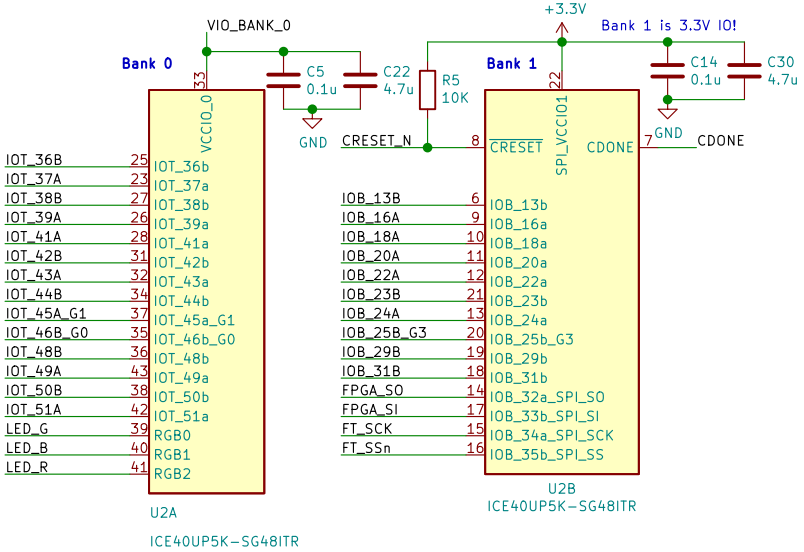
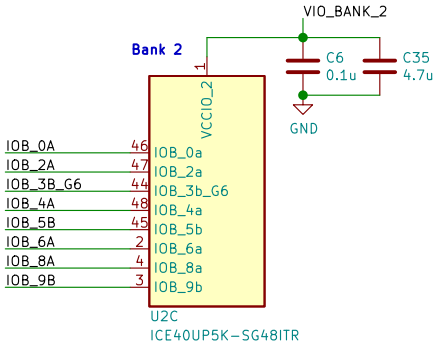
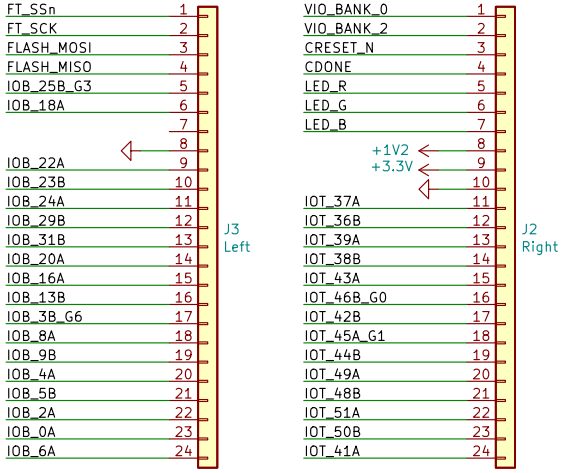
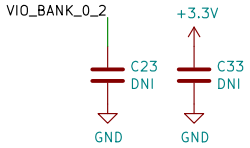
FPGA Banks



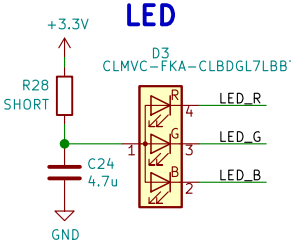


Board Connections

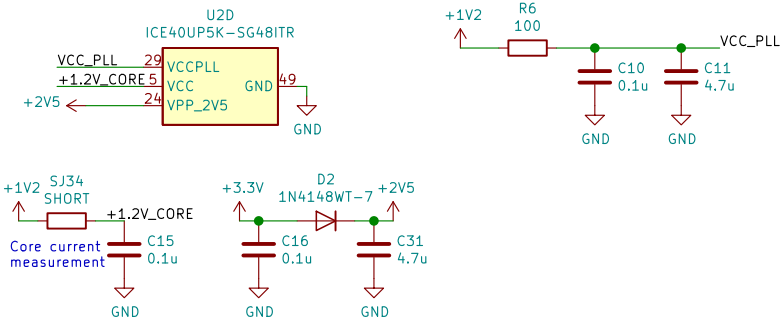




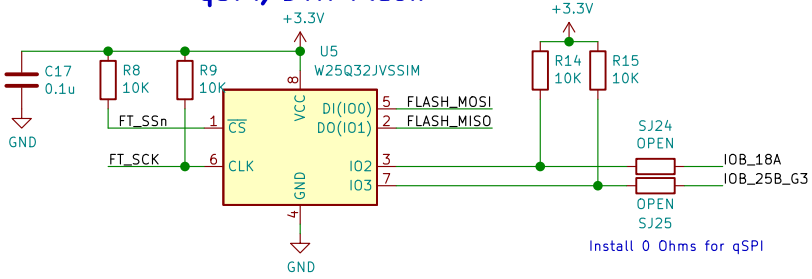
LED



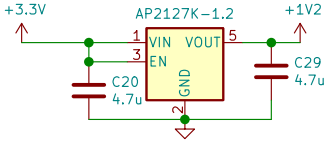
FPGA Power



qSPI/DTR Flash



1.2V



TBD:
- What if the flash is at 1.8V? Do we need a pad for the LDO?
- Edge connection pinout is TBD

FID1 Fiducial FID3 Fiducial FID5 Fiducial FID2 Fiducial FID4 Fiducial FID6 Fiducial

Sheet: / File: UPmicro.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1