Clock Signals for Altera DE-Series Boards

For Quartus II 13.0

1 Core Overview

The peripherals on the Altera® DE-series boards require clock signals for their operation. Some of these peripherals, the SDRAM, Audio Codec and VGA DAC chips, require the clock to have specific frequencies. The Clock Signals IP core generates those peripherals.

2 Functional Description

The Clock Signals IP Core can provide the necessary clocks for the VGA and Audio Cores and the SDRAM Controller for the DE-series boards. The block diagram of the core is shown in Figure 1.

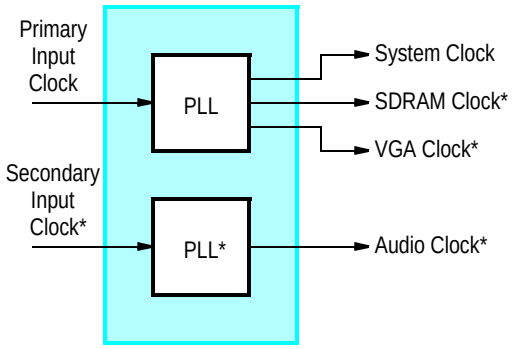

Figure 1. High-level block diagram of the Clock Signals IP core.

The core requires one or two input clocks and generates up to four output clocks. The signals in the figure marked by the asterisk are optional. The following subsections describe the purpose of each signal shown in Figure 1.

2.1 Primary Input Clock

The primary input clock is used to derive the system, VGA and SDRAM clocks. It is called `CLK_IN_PRIMARY` in Qsys. This clock must have a frequency of 50 MHz, which is the default frequency in Qsys and the main external clock frequency on the DE series boards.

2.2 Secondary Input Clock

The secondary input clock is used to derive the audio clock. It is called `CLK_IN_SECONDARY` in Qsys. This input is optional, and should be driven by a 27 MHz clock.

2.3 System Clock

The System Clock output is a 50 MHz clock signal. It is called `sys_clk` in Qsys. It should be used as the clock for all cores in Qsys, except for the Clock Signals IP and VGA Controller cores.

2.4 VGA Clock

The VGA Clock output is a 25 MHz clock signal required by the VGA Controller IP core (see Video IP cores' documentation for more details). The VGA Clock output from the Clock Signals IP core is called `vga_clk` in Qsys. This clock should be used for on-chip VGA components only. The clock pin of the VGA DAC on the DE-seried boards and the LCD daughter card, should be connected to the `VGA_CLK` signal which is output from the VGA Controller IP core. If the selected DE-Series Board is the tPad, then a secondary VGA clock signal, with a frequency of 40 MHz, is included. This secondary VGA clock signal should be used to drive the VGA controller for the 8 inch LCD screen.

2.5 SDRAM Clock

The SDRAM Clock output, named `sdram_clk`, is a clock signal with a −3ns phase shift to the 50 MHz system clock to ensure the correct timing for the SDRAM chip on the DE-series boards. The SDRAM clock should only be used to clock the SDRAM chip on the DE series boards. A `sdram_clk` signal will be available at the top level HDL module, which is generated for the Qsys system that includes the Clock Signals IP core. This signal should be connected to the `DRAM_CLK` pin on the DE series boards. Note that the `sdram_clk` signal must be exported, as shown in Figure 4, otherwise it will not be available at the top level HDL module.

2.6 Audio Clock

The Audio Clock output, named `audio_clk`, is a clock signal required by the audio CODEC chip. The frequency of this clock can be one of 11.2896, 12.0, 12.288, 16.9344 and 18.432 MHz. These frequencies are required by the audio CODEC chip for different sampling rates. See the audio chip's datasheet (pages 38 - 42) for more information regarding sampling rates and their associated clock frequencies. Users can find this signal in the clock list in Qsys. The audio clock should only be used to clock the audio chip on the DE series boards. An `audio_clk` signal will be available at the top level HDL module, which is generated for the Qsys system that includes the Clock Signals IP core. This signal should be connected to the `AUD_XCK` pin on the DE series boards. Note that the `audio_clk` signal must be exported, as shown in Figure 4, otherwise it will not be available at the top level HDL module.

3 Instantiating the Core in Qsys or Megawizard

Designers should use the Clock Signals IP core's configuration wizard in Qsys or Megawizard to specify its settings. The following configurations are available and shown in Figure 2:

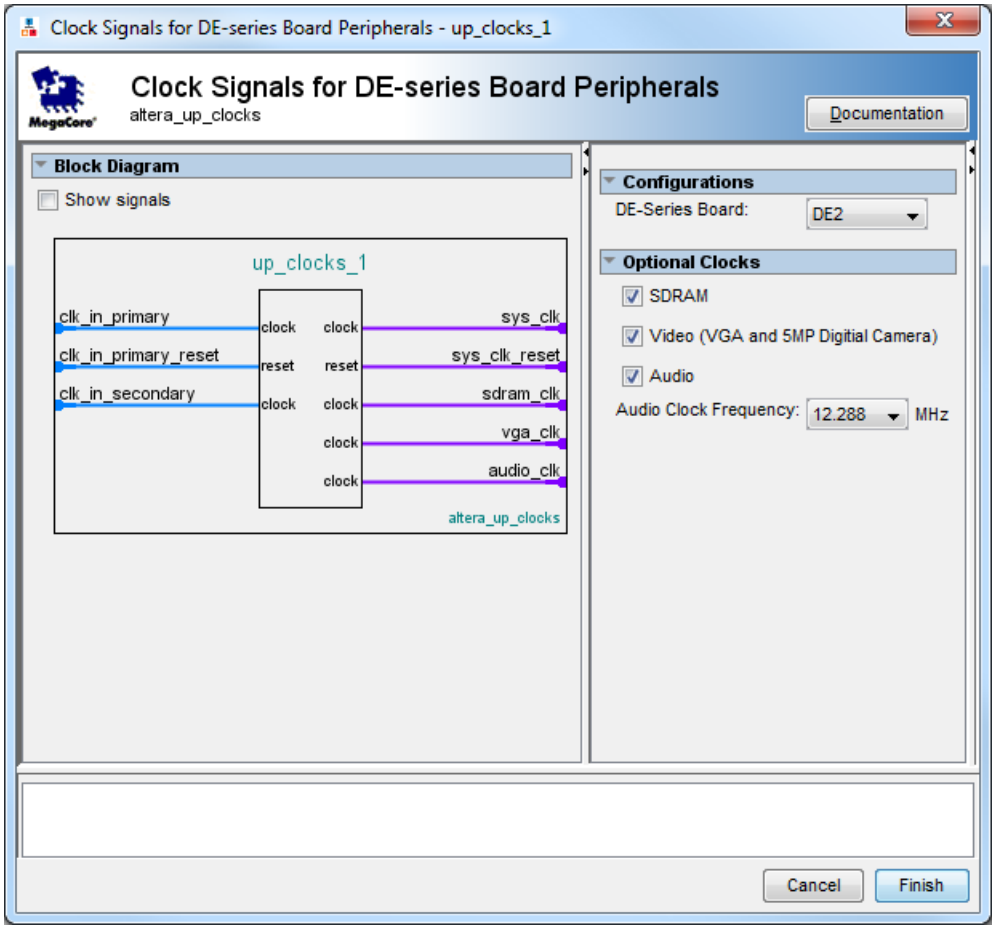

Figure 2. Clock Signals' Qsys wizard.

- **DE-Series Board** — allows users to specify the target board.
- **Optional Clocks** — allows users to select the components (VGA, SDRAM, Audio), which are used in the system and that require their own clocks. Checking the box next to a component will generate the appropriate clock for it.
- **Audio Clock Frequency** — allows users to select the clock frequency for the audio chip.

If the audio clock is selected, then the secondary input clock must be manually added to the clock list in Qsys. To manually add a clock, click the add button, which is to the right of the clock settings window. Edit the freguency value to 27 MHz. Also, you may rename the clock for your convenience.

Assuming that you have selected all the optional clocks, Figure 3 shows the contents of the clock settings window in Qsys. All cores, except for the Clock Signals and VGA Controller cores, should now be assigned to the system clock as shown in Figure 4. Also, the figure shows how to connect the primary and secondary input clocks to the Clock Signals IP core and the VGA clock to the VGA Controller and Dual-Clock Buffer IP cores.

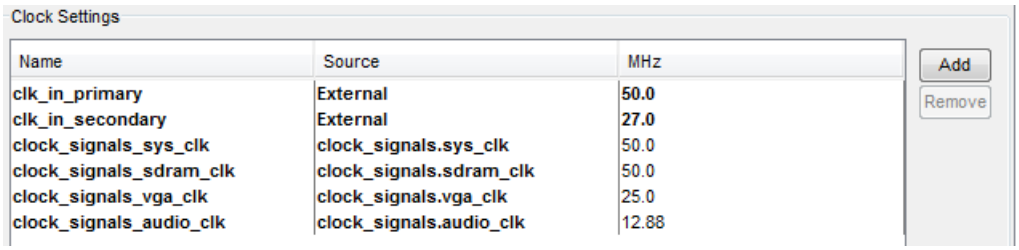

Figure 3. Qsys's clock settings window.

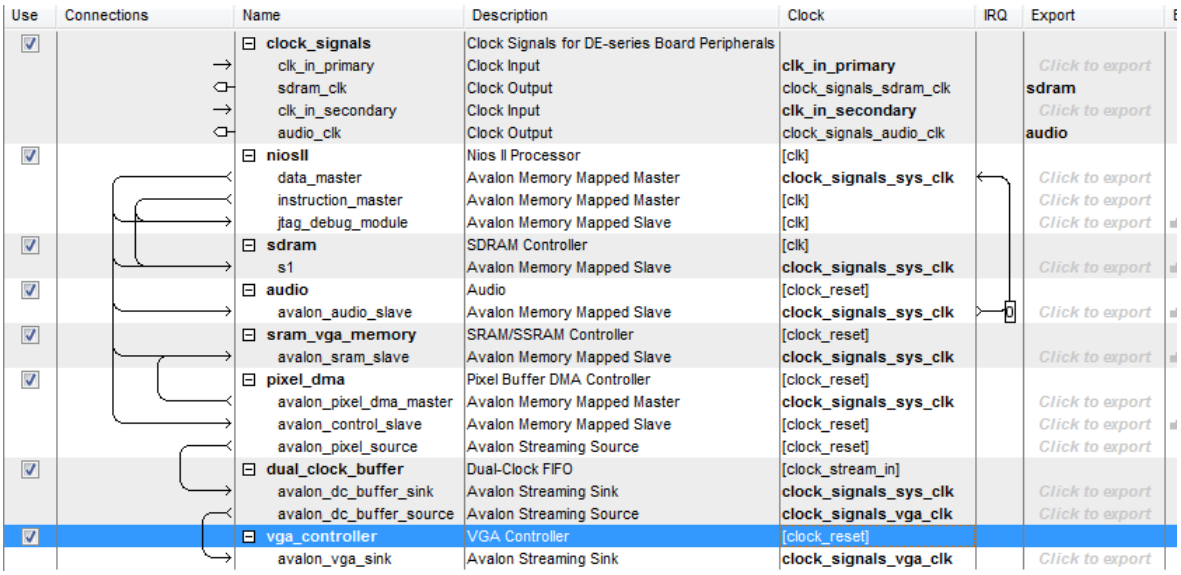

Figure 4. Qsys's clock connections.

Figures 5 and 6 shows an example of the clock ports on a top-level Qsys system for the DE-series boards, for both Verilog and VHDL, respectively. Note that `sys_clk` and `vga_clk` signals are not connected since they are for internal use only.

```
qsys_system the_system (
    .clk_in_primary      (CLOCK_50),
    .clk_in_secondary    (CLOCK_27),
    .reset_n             (KEY[0]),
    .audio_clk           (AUD_XCK),
    .sdram_clk           (DRAM_CLK),
    .sys_clk             (),
    .vga_clk             (),
    ...
);
```

Figure 5. External clock connections from Qsys example for verilog.

```
the_system : qsys_system
  port map (
    clk_in_primary      => CLOCK_50,
    clk_in_secondary    => CLOCK_27,
    reset_n             => KEY(0),
    audio_clk           => AUD_XCK,
    sdram_clk           => DRAM_CLK,
    ...
  );
```

Figure 6. External clock connections from Qsys example for VHDL.

Figures 7 and 8 shows an example of the clock ports on the module generated by the Megawizard for the DE-series boards, for both Verilog and VHDL, respectively. Note that `sys_clk` and `VGA_CLK` signals are connected. The `sys_clk` should be use as your system clock. The `VGA_CLK` should be used to drive the VGA subsystem, if used in your design.

```
up_clocks the_inst (
    .CLOCK_50      (CLOCK_50),
    .CLOCK_27      (CLOCK_27),
    .reset         (!KEY[0]),
    .AUD_CLK       (AUD_XCK),
    .SDRAM_CLK     (DRAM_CLK),
    .sys_clk       (sys_clk),
    .VGA_CLK       (VGA_CLK),
);
```

Figure 7. External clock connections from Megawizard example for verilog.

```
the_inst : up_clocks
  port map (
    CLOCK_50          => CLOCK_50,
    CLOCK_27          => CLOCK_27,
    reset             => !KEY(0),
    AUD_CLK           => AUD_XCK,
    SDRAM_CLK         => DRAM_CLK,
  );
```

Figure 8. External clock connections from Megawizard example for VHDL.