Altera University Program Flash Memory IP Core

Qsys and Standalone IP Core

1 Core Overview

A Flash Memory is a non-volatile type of memory that can be electrically erased and reprogrammed. It is similar to volatile types of memory, such as SRAM and DRAM, in that it can be written to and read; however, it is different in that it retains its data even when the memory device is powered down. The ability to retain its data makes it useful in applications such as Secure Data cards and USB memory sticks for the purposes of storing and transporting data.

While flash memory is versatile it has its limitations. Unlike volatile memory, to change the memory contents the data present in the memory must first be erased and only then can new data be written. The underlying technology also places a limitation on the number of times data can be written reliably to any particular location of the flash memory. Typically, flash memory devices allow each memory location to be written in the order of 10000 times, and up to 100000 in high-end parts.

The Altera University Program (UP) Flash Memory IP Core is a hardware component that facilitates the use of flash memory devices present on the Altera DE1 and DE2 boards. We provide this core for general use, however we advise that the flash memory not be used for temporary data storage, as doing so may significantly reduce the lifetime of the flash memory chips.

This document describes how to instantiate the Altera UP Flash Memory IP Core in a Qsys based design as well as a standalone module in user designs.

2 Functional Description

The Altera UP Flash Memory IP Core is supplied with two interfaces: a standalone interface, and Avalon Interconnect Interface. The standalone interface is intended for use in designs where an Avalon Interconnect is not used. The Avalon Interconnect Interface should be used in Qsys based systems, where the core will become a memory mapped I/O slave attached to the Avalon Interconnect. We describe the functionality of both versions of the core in the following subsections.

2.1 Standalone Version

The standalone interface diagram of the Altera UP Flash Memory IP Core is shown in Figure 1. It consists of user interface signals on the left-hand side, and a flash memory chip signals on the right-hand side. The signals on the left-hand side are all single bit wires, with the exception of *i_data*, *o_data*, and *i_address*. The data ports are both 8 bit wide, while the input address is defined by a *FLASH_MEMORY_ADDRESS_WIDTH* parameter. By default, the flash memory address width parameter is set to 22, indicating that 22 address bits are necessary to address each byte in a 4MB flash memory device. The remaining signals on the left-hand side are control signals that allow the flash

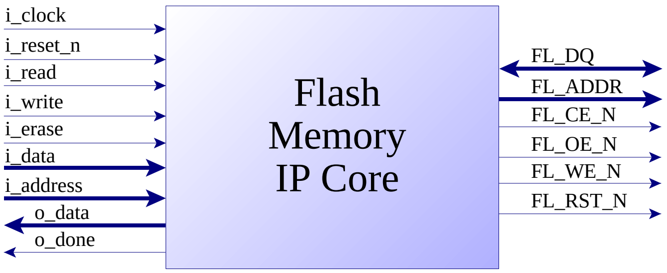

Figure 1. Standalone Flash Memory IP Core Interface.

memory to be read, written and erased.

The flash memory chip signals shown on the right hand side connect to the flash memory device on a DE board. Port *FL_DQ* is an 8-bit bidirectional bus that carries the data to and from the flash memory device. The address in the memory to be accessed is specified by the *FL_ADDR* output port. Its width matches that specified by *FLASH_MEMORY_ADDRESS_WIDTH* parameter. The other output signals are 1-bit wide each, and control data transfer between the Flash Memory IP Core and the flash memory device.

In the following subsections we describe how each set of signals operates.

2.1.1 User Interface

In addition to data and address lines described earlier, the user interface inputs include an *active-low* asynchronous reset, *i_reset_n*, a clock input called *i_clock*, as well as control signals *i_read*, *i_write*, *i_erase*, and *o_done*. The asynchronous reset signal will reset the internal FSM to an initial state, where the circuit will reset the flash memory device and prepare it for data exchange. The clock signal should connect to a 50MHz clock signal.

To transfer data between to and from the flash memory, several control signals are provided. The *i_read* signal causes the circuit to read a byte of data specified by the *i_address* input and produce it at the *o_data* output. Please note that the output will only be valid when the *o_done* signal is raised. Thus, the *i_read* signal should remain high until *o_done* is raised, before the data from the *o_data* lines is read. The *i_write* signal functions in a similar manner. When high, the *i_write* signal causes data at input *i_data* to be written at the address specified by *i_address*. The operation completes when *o_done* is raised. Please note that no other operation can be performed while a read/write operation is ongoing.

The *i_erase* signal functions differently. When *i_erase* is raised high, it causes a sector of memory to be erased. The sector that will be erased is the one which contains the byte at address specified by the *i_address* input. The only exception is when the *i_address* input consists of all 1s. In such a case, the entire flash memory device will be erased. It is important to note that the erase operation is critical to the proper operation of the flash memory. To write new data to an occupied memory location, it is necessary to erase the specified memory location first. This results in a hexadecimal value **FF** to be stored in the erased memory locations. Once the memory, either a sector of 8k/64k bytes or the entire chip, has been erased, the *o_done* signal will be raised. Please note that no other operations can be performed while an erase operation is ongoing.

Most flash memory interfaces allow data writes to previously written locations without forcing an erase operation to be executed first. Doing so is inadvisable, because the new data cannot be guaranteed to be stored correctly. More specifically, any bit that has been set to 0 cannot be changed to a 1 without using the memory location first. To protect the flash memory devices from accidental misuse, the Altera UP Flash Memory IP Core includes a protection mechanism that prevents writing data to non-empty memory locations. Any attempt to do so will result in the circuit behaving as though the operation succeeded. However, no data will actually be written to the specified memory location. A subsequent read operation will show that the memory contents remain unchanged.

2.1.2 Flash Memory Chip Interface

The signal connected to the flash memory device directly include *FL_DQ*, *FL_ADDR*, *FL_OE_N*, *FL_WE_N*, *FL_CE_N*, and *FL_RST_N*. The *FL_DQ* is a set of 8 bidirectional wires used to transfer data between the IP Core and the flash memory chip. The address of the data to be accessed is specified by the *FL_ADDR* lines. The remaining ports are control signals that ensure the transfer of data is completed correctly. The detailed behaviour of these signals is beyond the scope of this document. Further details on this topic can be found in the datasheet for the given flash memory device.

2.2 Qsys Version

The Qsys version of the flash memory IP core is shown in Figure 2.

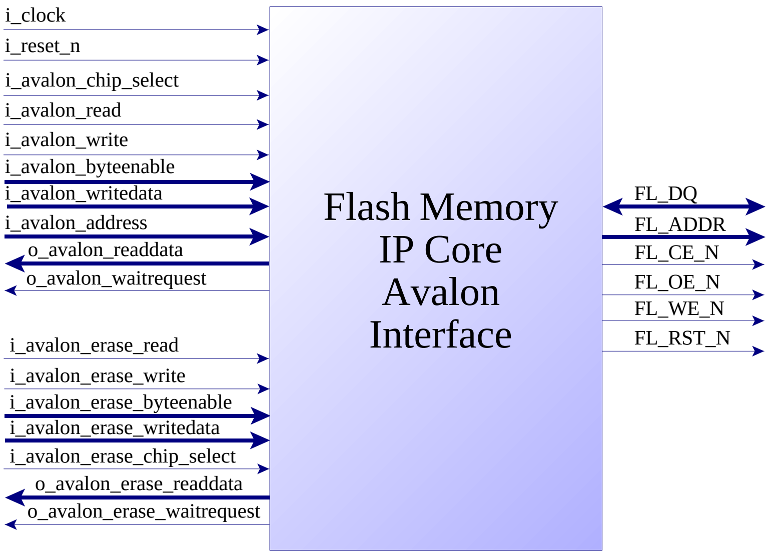

Figure 2. Qsys Flash Memory IP Core with Avalon Interconnect Interface.

This module is similar to the standalone version of the core, except in how it interfaces with a user circuit. In this case, the interface is facilitated by the Avalon Interconnect fabric. The Avalon Interconnect fabric allows components to be attached to a system and assigns an address range for each device on the interconnect. Thus, a Nios II soft-core processor that connects to peripheral devices by the means of this interconnect, can access each device as a memory mapped slave, simply by providing the appropriate address to the Avalon Interconnect.

The Altera UP Flash Memory IP Core has two memory-mapped slave ports that connect to the Avalon Interconnect.

One set, allows data to be transferred to and from flash memory. This allows the flash memory to appear as though it is a regular memory with read and write capability. The other set, labeled **_avalon_erase_** is a set of ports that provides access to an erase-control register.

The erase-control register is a 32-bit register used to control the erasing operation of flash memory device. Writing an address to this register causes the core to erase a sector containing the specified address. In a special case, when the address is (-1), the entire flash memory device will be erased. Please note that while the erase operation is in progress, the avalon interconnect will wait for the operation to complete. This means that another request to the flash memory device cannot be issued during that time.

3 Instantiating the Flash Memory IP Core

To use the Altera UP Flash Memory IP Core, the core needs to be instantiated in a design. This can be done in two ways: as a standalone module that functions in a manner similar to regular memory, or as a Qsys component connected to the Avalon Interconnect. Both methods of instantiating the core are described below.

3.1 Instantiating a Standalone Version of the Core

The Altera UP Flash Memory IP Core can be used as a standalone module that interfaces with a flash memory chip on DE boards. Users should instantiate a module called *Altera_UP_Flash_Memory_IP_Core_Standalone* to use the flash memory core in a standalone version. The input and output ports for the standalone Altera UP Flash Memory IP Core are shown in Figure 1, and described in detail in Section 2.

3.2 Instantiating a Qsys Version of the Core

To include the Altera UP Flash Memory IP Core in an Qsys-based design, users need to instantiate the core using the Qsys tool. To do this, locate the core in the list of modules under University Program > Memory, and click on Altera UP Flash Memory IP Core. This will bring up a dialog box, where users will be able to specify the memory size by defining a *FLASH_MEMORY_ADDRESS_WIDTH* parameter. By default, this parameter is set to 22, which indicates the flash memory is 4MB in size. Adjust the bitwidth according to the size of the flash memory device on your board and click Finish.

Once the core is instantiated, it is only necessary to assign an address range for the core to use. The flash memory core has two memory mapped slave ports, each with a separate address ranges. The first port, called *flash_data*, is a port that allows reading from and writing to the flash memory. The address range for this port matches the memory size of the flash memory chip. The second port, called *flash_erase_control* has an address range of 4 bytes. It facilitates access to the erase-control register. Both ports should be connected to the data master on the Avalon Interconnect.

Both of the address ranges mentioned above need to be assigned. They should be assigned such that they do not overlap with any existing devices connected to the Avalon Interconnect fabric. Once your system is configured to include the Altera UP Flash Memory IP Core, the generated system will contain I/O ports that need to be connected to specific pins on the Altera DE1 or DE2 board to access the flash memory chip properly. Please refer to the specific board manual for correct pin assignments.

3.3 Timing Constraints

When instantiating a Flash Memory IP core in a design it is important to set output constraints for pins that connect to the Flash Memory chip. This is important because without such constraints signals generated by the core may arrive at the Flash Memory chip out-of-order, thereby making the Flash Memory device appear to malfunction. For the Altera UP Flash Memory IP Core, both the standalone and the Qsys versions, the timing constraints for the FL_* signals should be set as follows:

1. *Fast Output Register* flag should be turned ON
2. T_{co} requirement should be set to no more than 10ns, and
3. T_{su} requirement should be set to no more than 10ns.

4 Software Programming Model

The Altera UP Flash Memory IP Core has a simple interface. The memory can be accessed by reading and writing data to the address range occupied by the Altera UP Flash Memory IP Core. This address range it occupies is specified within the Qsys software. In addition, an erase-control register that allows the flash memory to be erased is provided separately. It is a memory-mapped register, whose location in memory is specified in the Qsys based system.

The erase-control register provides a means to erase part, or all, contents of the flash memory device. To erase a portion of the memory, write an address to the erase-control register. The Altera UP Flash Memory IP Core will take this address and erase the sector in the flash memory that contains the specified memory location. Please note that a sector of flash memory can be 8 or 64 kbytes in size for a 4MB flash memory devices on DE1 and DE2 boards. To erase the contents of the entire flash memory device, write (-1) to the flash memory erase-control register.

5 Summary

This document described the Altera University Program Flash Memory IP Core for Altera DE1 and DE2 boards. A demonstration program of how this core can be used, called *Altera University Program Flash Memory Demo*, can be found on Altera University Program Website.