# Crystalfontz America, Inc.

CUSTOMER			
MODEL	CFAH1602B-TMC-JP		
APPROVAL	BY:	DATA:	

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

### **Crystalfontz America, Inc.**

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### 1. Module Classification Information

$$\begin{array}{ccccc} \underline{CFA} \ \underline{H} & \underline{1} \ \underline{6} \ \underline{0} \ \underline{2} & \underline{3} & \underline{B} - \underline{T} \ \underline{M} \ \underline{C} - & \underline{JP} \\ \hline \textcircled{\$} & \textcircled{\$} & \textcircled{\$} & \textcircled{\$} & \textcircled{\$} \end{array}$$

1	Brand: CRYSTALFONTZ AMERICA, INCORPORATED					
2	Display Type: <b>H→Character Type</b> , G→Graphic Type					
3	Display's logical dimen	sions: 16 columns by 02 lines				
4	Model serials no.	_				
(5)	Backlight Type:	N→Without backlight	Y→LED, Yellow Green			
		B→EL, Blue green	A→LED, Amber			
		D→EL, Green	R→LED, Red			
		W→EL, White	O→LED, Orange			
		F→CCFL, White	G→LED, Green			
		<b>T</b> → <b>LED</b> , White				
6	LCD Mode:	B→TN Positive, Gray	M→STN Negative, Blue			
		N→TN Negative,	F→FSTN Positive			
		G→STN Positive, Gray	T→FSTN Negative			
		Y→STN Positive, Yellow Green				
7	LCD Polarizer Type,	A→Reflective, N.T, 6:00	H→Transflective, W.T,6:00			
	Temperature range,	D→Reflective, N.T, 12:00	K→Transflective, W.T,12:00			
	Viewing direction:	G→Reflective, W. T, 6:00	C→Transmissive, N.T,6:00			
		J→Reflective, W. T, 12:00	F→Transmissive, N.T,12:00			
		B→Transflective, N.T,6:00	I→Transmissive, W. T, 6:00			
		E→Transflective, N.T.12:00	L→Transmissive, W.T,12:00			
8	Special Code:	JP→English and Japanese standar	rd font			

# 2. Precautions in use of LCD Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering:only to the I/O terminals.
- (7) Storage:please storage in anti-static electricity container and clean environment.

### 3. General Specification

ITEM	STANDARD VALUE	UNIT		
Number of Characters:	16 characters × 2 Lines			
Module dimension:	80.0×36.0×13.5(MAX)mm	mm		
View area:	66.0×16.0mm	mm		
Active area:	56.2×11.5mm	mm		
Character size:	$(L)2.95 \times (W)5.55$ mm	mm		
Character pitch:	$(L)3.55 \times (W)5.95$ mm	mm		
LCD type:	STN, Negative ,transmissive, B	Blue		
Duty:	1/16			
View direction:	6 o'clock			
Backlight:	LED White			

### 4. Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	$T_{OP}$	0	_	+50	$^{\circ}\!$
Storage Temperature	$T_{ST}$	-10	_	+60	$^{\circ}\!\mathbb{C}$
Input Voltage	V <sub>I</sub>	$V_{SS}$	_	$V_{DD}$	V
Supply Voltage For Logic	VDD-VSS	-0.3	_	7	V
Supply Voltage For LCD	$V_{DD}$ - $V_0$	-0.3	_	Vdd+0.3	V
Supply current FOR LED B/L	ILED	_	_	25	mA

### 5. Electrical Characteristics

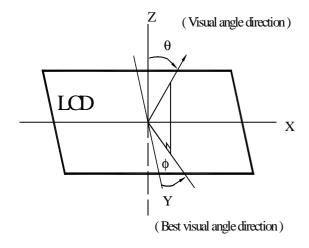
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	$V_{DD}$ - $V_{SS}$	_	4.5	_	5.5	V
		Ta=0°C	_		4.5	V
Supply Voltage For LCD	$V_{DD}$ - $V_0$	Ta=25°℃	_	4.2	_	V
		Ta=50°C	3.8		_	V
Input High Vol	$V_{\mathrm{IH}}$	_	2.2	_	$V_{\mathrm{DD}}$	V
Input Low Vol	$V_{\rm IL}$	_	_	_	0.6	V
Output High Vol	$V_{\mathrm{OH}}$	_	2.4	_	_	V
Output Low Vol.	$V_{OL}$	_	_	_	0.4	V
Supply Current	$I_{DD}$	V <sub>DD</sub> =5V	_	1.2	_	mA

### 6. Optical Characteristics

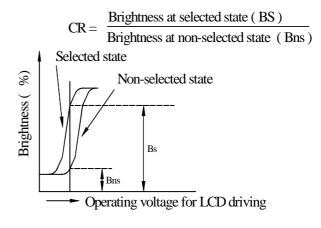
ITEM	SYMBAL	CONDITION	MIN.	TYP.	MAX.	UNIT
X7' A 1	(V) θ	CR≧3	10		105	deg
View Angle	(H) φ	CR≧3	-30		30	deg
Contrast Ratio	CR	_		5		_
	T rise	_		200	300	ms
Response Time	T fall	_		200	300	ms

### **6.1 Definitions**

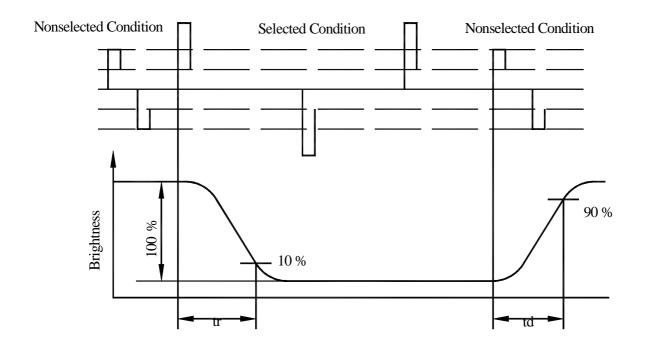
#### **View Angles**



#### **Contrast Ratio**



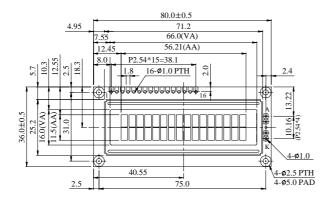
#### **Response Time**



# 7. Interface Pin Function

		ı	
Pin No.	Symbol	Level	Description
1	$V_{SS}$	0V	Ground
2	$V_{DD}$	5.0V	Supply Voltage for logic
3	VO	(Variable)	Operating voltage for LCD
4	RS	H/L	H:DATA, L:Instruction code
5	R/W	H/L	H:Read(MPU→Module)L:Write(MPU→Module)
6	Е	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	A	_	Power supply for LED backlight ( + )
16	K	_	Power supply for LED backlight ( - )

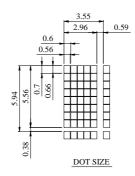
### 8. Counter drawing



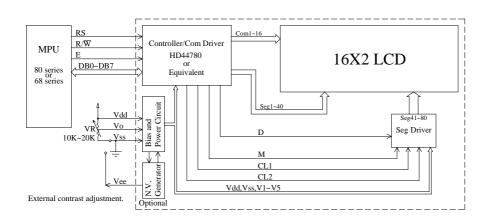


LED H/L B/L					
$\angle$	High				
Н1	13.2				
H2	8.6				

PIN NO.	SYMBOL
1	Vss
2	Vdd
3	Vo
4	RS
5	R/W
6	Е
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	A/Vee
16	K



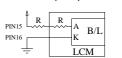
The non-specified tolerance of dimension is  $\pm 0.3 \text{mm}$ .



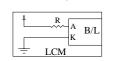
LED B/L Drive Method 1.Drive from A,K



2.Drive from pin15, pin16



(Will never get Vee output from pin15) 3.Drive from Vdd,Vss



(Contrast performance may go down.)

 $\begin{array}{l} Recommanded\ Value \\ V_{\text{LED}} = 3.3V,\ \underline{I}_{\text{LED}} = 25\text{mA} \end{array}$ 

Character located DDRAM address DDRAM address 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F

# 9. Backlight Information

9.1 Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED		25		mA	V=3.3V
Supply Voltage	V	_	3.3	3.6	V	
Reverse Voltage	VR	_	_	8	V	
Luminous Intensity	IV	20	_	_	CD/M <sup>2</sup>	ILED=25mA
Wave Length	λρ				nm	ILED=25mA
Life Time		_	100000	_	Hr.	V≤3.6V
Color					White	

### 10. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

### Busy Flag (BF)

When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

#### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

#### Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is  $80\times8$  bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.

High bits Low bits AC6 AC5 AC4 AC3 AC2 AC1 AC0 (hexadecimal)

Example:DDRAM addresses 4E 1 0 0 1 1 1 0

#### **DDRAM Address**

#### Display position DDRAM address

AC

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

2-Line by 16-Character Display

#### **Character Generator ROM (CGROM)**

The CGROM generate  $5 \times 8$  dot or  $5 \times 10$  dot character patterns from 8-bit character codes. See Table 2.

#### **Character Generator RAM (CGRAM)**

In CGRAM, the user can rewrite character by program. For  $5 \times 8$  dots, eight character patterns can be written, and for  $5 \times 10$  dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

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# Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)

Table 1.

For 5 \* 8 dot character patterns

5 * 8 dot character pattern	S
Character Codes (DDRAM data)	CGRAM Address Character Patterns (CGRAM data)
7 6 5 4 3 2 1 0	5 4 3 2 1 0 7 6 5 4 3 2 1 0
High Low	High Low High Low
0 0 0 0 * 0 0 0	0 0 0 0   * * * *   0 0 0 0   Character pattern(1)   1 1 0   * * * *   0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1 1   * * * *   0 0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0   Cursor pattern   1 1 1 1   * * * *   0 0 0 0 0   Cursor pattern   1 1 1   * * *   0 0 0 0 0   Cursor pattern   1 1 1   * * * *   0 0 0 0   Curso
0 0 0 0 * 0 0 1	0 0 0 0
0 0 0 0 * 1 1 1	1 1 1 0 0 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1

For 5 \* 10 dot character patterns

5 * 10 dot character patte	rn s		
Character Codes (DDRAM data)	CGRAM Address	Character Patterns (CGRAM data)	
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0	
High Low	High Low	High Low	
	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	* * * * 0 0 0 0 0 * * * * 0 0 0 0 0 * * * *	
	0 0 1 1 0 0 1 0 0	* * * * 0 0 0	
0 0 0 0 * 0 0 0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	* * * * 0 0 0	Character
	0 1 1 0	* * * * 0 0 0 0	pattern
	1 0 0 0	* * * * 0 0 0 0	
		$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Cursor pattern
		<b>1</b>	
		* * *   * * * * *	

: " High "

# 11. Character Generator ROM Pattern

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#### Table.2

Upper																
4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LННН	HLLL	HLLH	HLHL	нгнн	HHLL	ннгн	HHHL	нннн
LLLL	CG RAM (1)					====	•••	<b>::::</b> -					-===	<b></b> .	:::::	<b> </b>
LLLH	(2)		i	1							<b></b>			··	-===	
LLHL	(3)		::	- :::			<u> </u>	<b>!</b> -			=	· ‡ · ·	! <u>!</u> !	.::: <sup>:</sup>		
LLHH	(4)				: <u>.</u>	::	<b>:</b> .						-::-	====	::::-	::-:=
LHLL	(5)						::::	·					i		<b></b>	====
LHLH	(6)		#				====	<b></b>			==				<b>::::</b>	II
LHHL	(7)			====		ii		<b>■</b> ■							<b> </b>	====
СННН	(8)		:=	:-::				<b>II</b>					::::			31
HLLL	(1)		<b>E</b>	::			<b>!</b> :	:-: <u>:</u>			<u>i</u> -	-:::		<b>!.!</b>	<b>!</b>	:-::
HLLH	(2)		_:	••		• • •	1	•				•	!		1	<u></u>
HLHL	(3)		:-[-:	::	<b>!</b>		:						· ·	<u></u>		====
нгнн	(4)		[	::			<b>!</b> ::	-			:::		<b></b>		:-:	
HHLL	(5)		:=	-:.	<b></b>			i				<b>∷.</b> :	:		-:[:-	
ннгн	(6)							:-				:		···	·i	:
нннг	(7)		::		<b>!!</b>	"	<b>!</b> -":							"-		
нннн	(8)			:			====	-=:			: :.:	٠!	:		ı <u></u> ı	

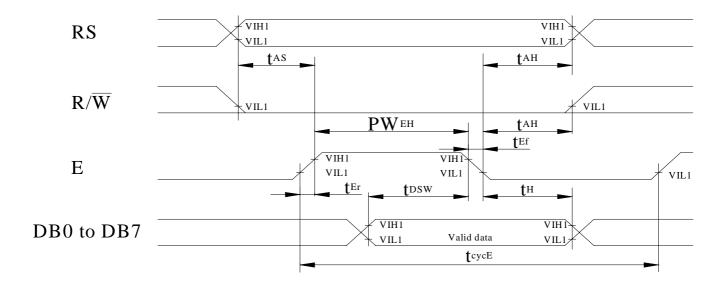
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### 12. Instruction Table

Instruction				Ins	structi	ion Co	ode				Description	Evacution time (face_270V bg)	
Thisti uction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution time (fosc=270Khz)	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms	
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms	
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μ s	
Display ON/OFF Control	0	0	0	0	0	0	1	D	С	В	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μ s	
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	_	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μ s	
Function Set	0	0	0	0	1	DL	N	F	_	1	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39 μ s	
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μ s	
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μ s	
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μ s	
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μ s	
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μ s	

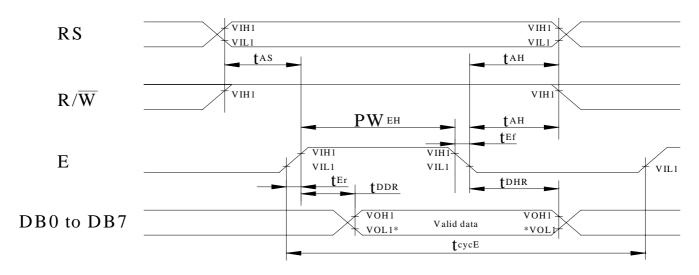
### 13. Timing Characteristics

### 13.1 Write Operation



Item	Symbol	Min	Тур	Max	Unit
Enable cycle time	t <sub>cycE</sub>	500	_	_	ns
Enable pulse width (high level)	PW <sub>EH</sub>	230	_	_	ns
Enable rise/fall time	$t_{\rm Er}, t_{\rm Ef}$	_	_	20	ns
Address set-up time (RS, R/W to E)	t <sub>AS</sub>	40	_	_	ns
Address hold time	t <sub>AH</sub>	10	_	_	ns
Data set-up time	$t_{ m DSW}$	80	_	_	ns
Data hold time	t <sub>H</sub>	10	_	_	ns

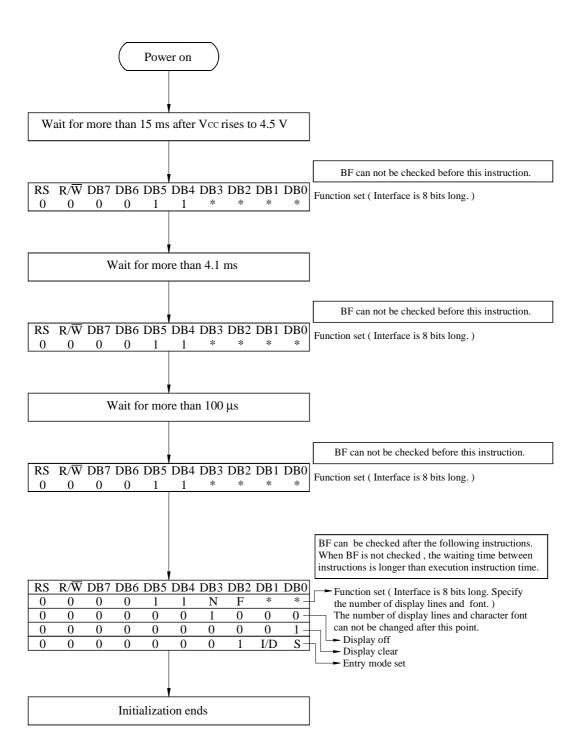
### 13.2 Read Operation



NOTE: \*VOL1 is assumed to be 0.8V at 2 MHZ operation.

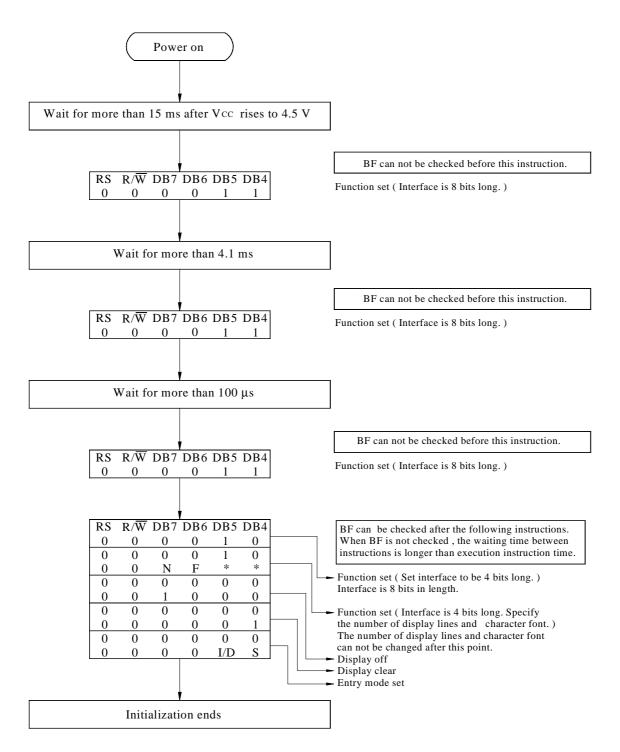
ITEM	Symbol	Min	Тур	Max	Unit
Enable cycle time	t <sub>cycE</sub>	500	_	_	ns
Enable pulse width (high level)	$PW_{EH}$	230	_		ns
Enable rise/fall time	$t_{\rm Er}, t_{\rm Ef}$	_	_	20	ns
Address set-up time (RS, R/W to E)	t <sub>AS</sub>	40	_	<del>-</del>	ns
Address hold time	t <sub>AH</sub>	10	_	_	ns
Data delay time	t <sub>DDR</sub>	_	_	160	ns
Data hold time	t <sub>DHR</sub>	5	_	_	ns

### 14. Initializing of LCM



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8-Bit Ineterface



4-Bit Ineterface

# 15. Quality Assurance

#### **♦** Screen Cosmetic Criteria

	Screen Cosin			
No.	Defect	Judgement Criterion	Partition	
		A)Clear		
		Size:d mm Acceptable Qty in active area		
		$d \leq 0.1$ Disregard		
		$0.1 < d \le 0.2$		
		$0.2 < d \le 0.3$		
		0.3 <d 0<="" td=""><td></td></d>		
1	Spots	Note:Including pin holes and defective dots which must be within one pixel size.	Minor	
		B)Unclear		
		Size:d mm Acceptable Qty in active area		
		$d \leq 0.2$ Disregard		
		$0.2 < d \le 0.5$		
		$0.5 < d \le 0.7$		
		0.7 <d 0<="" td=""><td></td></d>		
		Size:d mm Acceptable Qty in active area		
		$d \leq 0.3$ Disregard		
2	Bubbles in Polarizer	$0.3 < d \le 1.0$ 3	Minor	
		$1.0 < d \le 1.5$		
		1.5 <d 0<="" td=""><td></td></d>		
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel	Minor	
	Doruccii	surface, the scratches are not to be remarkable.	1,111101	
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor	
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels.	Minor	
,	Coloration	Back-light type should be judged with back-light on state only.	IVIIIIOI	

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### 16. RELIABILITY

### **Content of Reliability Test**

	Environmental Test											
No.	Test Item	Content of Test	Test Condition	Applicable Standard								
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	60°ℂ 200hrs									
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-10°C 200hrs									
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50°C 200hrs									
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0°C 200hrs									
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60°C,90%RH 96hrs									
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	50°C,90%RH 96hrs									
7	Temperature Cycle	Endurance test applying the low and high temperature cycle.  -10°C 25°C 60°C  30min 5min 30min 1 cycle	-10°C /60°C 10 cycles									
		Mechanical T	est									
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs									
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction									
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs									
		Others		T								
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5k $\Omega$ CS=100pF 1 time									

<sup>\*\*\*</sup>Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at  $25^{\circ}$ C