# IS61VPS102436A IS61LPS102436A IS61VPS204818A IS61LPS204818A



# 1Mb x 36, 2Mb x 18 36Mb SYNCHRONOUS PIPELINED, SINGLE CYCLE DESELECT STATIC RAM

**JUNE 2010** 

#### **FEATURES**

- · Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- · Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- Power Supply

LPS: VDD  $3.3V \pm 5\%$ , VDDQ  $3.3V/2.5V \pm 5\%$ VPS: VDD  $2.5V \pm 5\%$ , VDDQ  $2.5V \pm 5\%$ 

- JEDEC 100-Pin TQFP and 165-ball PBGA packages
- Lead-free available

#### **DESCRIPTION**

The *ISSI* IS61LPS/VPS102436A and IS61LPS/VPS 204818A are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPS/VPS102436A is organized as 1,048,476 words by 36 bits. The IS61LPS/VPS204818A is organized as 2M-word by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable ( $\overline{BWE}$ ) input combined with one or more individual byte write signals ( $\overline{BWx}$ ). In addition, Global Write ( $\overline{GW}$ ) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either ADSP (Address Status Processor) or ADSC (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the ADV (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

#### **FAST ACCESS TIME**

Symbol	Parameter	200	166	Units
tkQ	Clock Access Time	3.1	3.5	ns
tĸc	Cycle Time	5	6	ns
	Frequency	200	166	MHz

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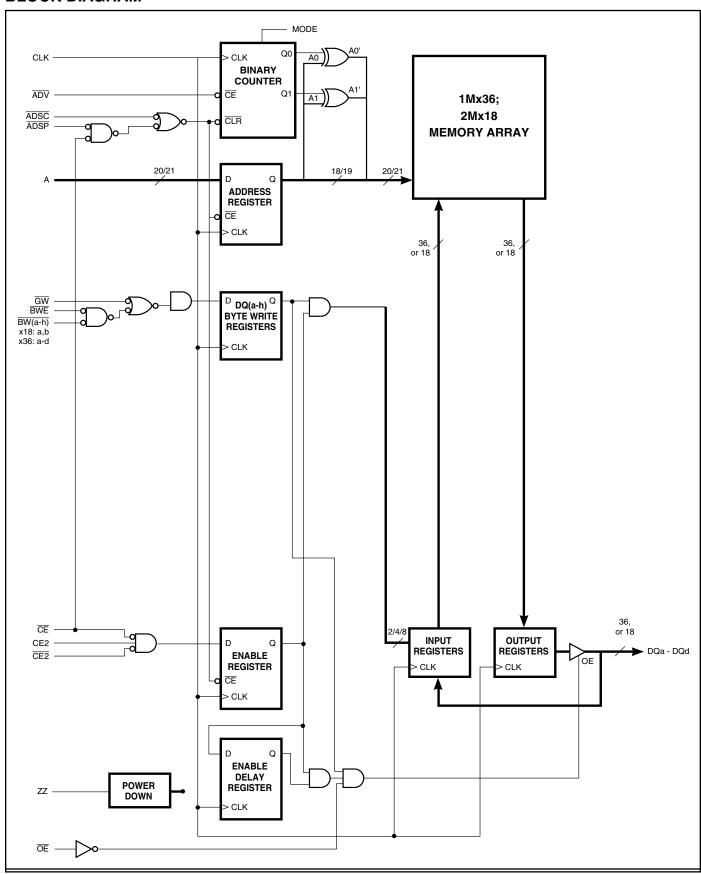
a.) the risk of injury or damage has been minimized;

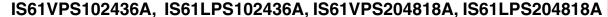
b.) the user assume all such risks; and

c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances



## **BLOCK DIAGRAM**

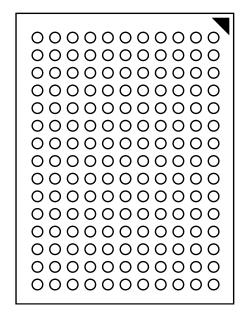






#### **165-PIN BGA**

165-Ball, 13x15 mm BGA 1mm Ball Pitch, 11x15 Ball Array



**BOTTOM VIEW** 





## 165 PBGA PACKAGE PIN CONFIGURATION

1M x 36 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
Α	NC	Α	CE	BWc	BWb	CE2	BWE	ADSC	ĀDV	Α	NC
В	NC	Α	CE2	BWd	BWa	CLK	GW	ŌĒ	ADSP	Α	NC
С	DQPc	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQb	DQb
Н	NC	NC	NC	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	NC	NC	ZZ
J	DQd	DQd	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	DQa
М	DQd	DQd	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	Vss	NC	Α	NC	Vss	VDDQ	NC	DQPa
Р	NC	NC	Α	Α	NC	A1*	NC	Α	Α	Α	Α
R	MODE	Α	Α	Α	NC	A0*	NC	Α	Α	Α	Α

Note: \* Ao and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

Symbol	Pin Name
Α	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance
ADSP	Address Status Processor
ADSC	Address Status Controller
GW	Global Write Enable
CLK	Synchronous Clock
CE, CE2, CE2	Synchronous Chip Select
BWx (x=a,b,c,d)	Synchronous Byte Write Controls

Symbol	Pin Name
BWE	Byte Write Enable
ŌĒ	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
VDD	3.3V/2.5V Power Supply
VDDQ	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground





## 165 PBGA PACKAGE PIN CONFIGURATION

2M x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
Α	NC	Α	CE	BWb	NC	CE2	BWE	ADSC	ĀDV	Α	Α
В	NC	Α	CE2	NC	BWa	CLK	GW	ŌĒ	ADSP	Α	NC
С	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
E	NC	DQb	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
F	NC	DQb	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
G	NC	DQb	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
Н	NC	NC	NC	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	NC	NC	ZZ
J	DQb	NC	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
K	DQb	NC	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
L	DQb	NC	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
М	DQb	NC	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	Vss	NC	Α	NC	Vss	VDDQ	NC	NC
Р	NC	NC	Α	Α	NC	A1*	NC	Α	Α	Α	Α
R	MODE	Α	А	Α	NC	A0*	NC	А	Α	Α	Α

Note: \* Ao and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

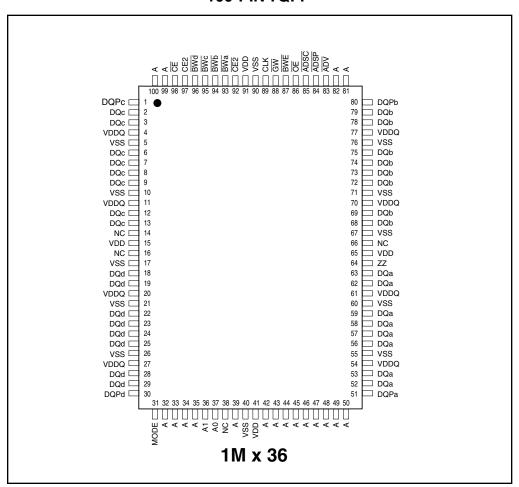
Symbol	Pin Name
Α	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance
ADSP	Address Status Processor
ADSC	Address Status Controller
GW	Global Write Enable
CLK	Synchronous Clock
CE, CE2, CE2	Synchronous Chip Select
BWx (x=a,b)	Synchronous Byte Write Controls

Symbol	Pin Name
BWE	Byte Write Enable
ŌĒ	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
VDD	3.3V/2.5V Power Supply
VDDQ	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground



#### **PIN CONFIGURATION**

#### 100-PIN TQFP



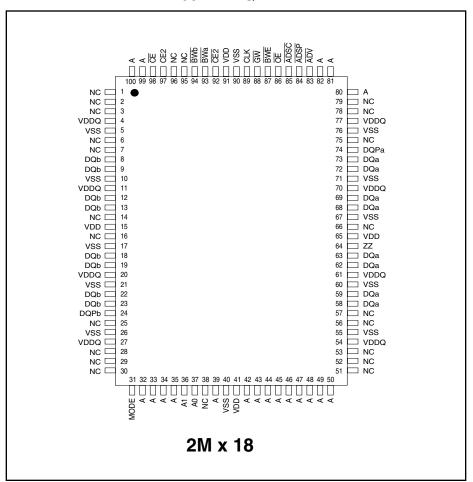
A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
Α	Synchronous Address Inputs
ADSC	Synchronous Controller Address Status
ADSP	Synchronous Processor Address Status
ADV	Synchronous Burst Address Advance
BWa-BWd	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable
CE, CE2, CE2	Synchronous Chip Enable
CLK	Synchronous Clock

DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data Input/Output
GW	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
ŌĒ	Output Enable
V <sub>DD</sub>	3.3V/2.5V Power Supply
VDDQ	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable



## **PIN CONFIGURATION**

#### 100-PIN TQFP



A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
Α	Synchronous Address Inputs
ADSC	Synchronous Controller Address Status
ADSP	Synchronous Processor Address Status
ADV	Synchronous Burst Address Advance
BWa-BWb	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable
$\overline{\text{CE}}$ , CE2, $\overline{\text{CE2}}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQb	Synchronous Data Input/Output

DQPa-DQPb	Parity Data I/O; DQPa is parity for DQa1-8; DQPb is parity for DQb1-8
GW	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
ŌĒ	Output Enable
V <sub>DD</sub>	3.3V/2.5V Power Supply
VDDQ	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable





## **TRUTH TABLE**(1-8) (3CE option)

OPERATION	ADDRESS	CE	CE2	CE2	ZZ	ADSP	ADSC	ADV	WRITE	ŌĒ	CLK	DQ
Deselect Cycle, Power-Down	None	Н	Х	Х	L	Χ	L	Χ	Х	Х	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Χ	L	L	L	Χ	Χ	Χ	Χ	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Н	Χ	L	L	Χ	Χ	Χ	Χ	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Χ	L	L	Н	L	Χ	Χ	Χ	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Н	Χ	L	Н	L	Χ	Χ	Χ	L-H	High-Z
Snooze Mode, Power-Down	None	Χ	Χ	Χ	Н	Χ	Χ	Χ	Χ	Χ	Χ	High-Z
Read Cycle, Begin Burst	External	L	L	Н	L	L	Χ	Χ	Χ	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	Н	L	L	Χ	Χ	Χ	Н	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	Н	L	Н	L	Χ	L	Χ	L-H	D
Read Cycle, Begin Burst	External	L	L	Н	L	Н	L	Χ	Н	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	Н	L	Н	L	Χ	Н	Н	L-H	High-Z
Read Cycle, Continue Burst	Next	Χ	Χ	Χ	L	Н	Н	L	Н	L	L-H	Q
Read Cycle, Continue Burst	Next	Χ	Χ	Χ	L	Н	Н	L	Н	Н	L-H	High-Z
Read Cycle, Continue Burst	Next	Н	Χ	Χ	L	Χ	Н	L	Н	L	L-H	Q
Read Cycle, Continue Burst	Next	Н	Χ	Χ	L	Χ	Н	L	Н	Н	L-H	High-Z
Write Cycle, Continue Burst	Next	Χ	Χ	Χ	L	Н	Н	L	L	Χ	L-H	D
Write Cycle, Continue Burst	Next	Н	Χ	Χ	L	Χ	Н	L	L	Χ	L-H	D
Read Cycle, Suspend Burst	Current	Χ	Χ	Χ	L	Н	Н	Н	Н	L	L-H	Q
Read Cycle, Suspend Burst	Current	Χ	Χ	Χ	L	Н	Н	Н	Н	Н	L-H	High-Z
Read Cycle, Suspend Burst	Current	Н	Χ	Χ	L	Χ	Н	Н	Н	L	L-H	Q
Read Cycle, Suspend Burst	Current	Н	Χ	Χ	L	Χ	Н	Н	Н	Н	L-H	High-Z
Write Cycle, Suspend Burst	Current	Χ	Χ	Χ	L	Н	Н	Н	L	Χ	L-H	D
Write Cycle, Suspend Burst	Current	Н	Χ	Χ	L	Χ	Н	Н	L	Χ	L-H	D

#### NOTE:

- 1. X means "Don't Care." H means logic HIGH. L means logic LOW.
- 2. For WRITE, L means one or more byte write enable signals (BWa-h) and BWE are LOW or GW is LOW. WRITE = H for all BWx, BWE, GW HIGH.
- 3. BWa enables WRITEs to DQa's and DQPa. BWb enables WRITEs to DQb's and DQPb. BWc enables WRITEs to DQc's and DQPc. BWd enables WRITEs to DQd's and DQPd. DQPa-DQPd are available on the x36 version.
- 4. All inputs except OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
- 5. Wait states are inserted by suspending burst.
- 6. For a WRITE operation following a READ operation,  $\overline{\text{OE}}$  must be HIGH before the input data setup time and held HIGH during the input data hold time.
- 7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
- 8. ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE LOW or GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

## IS61VPS102436A, IS61LPS102436A, IS61VPS204818A, IS61LPS204818A



## TRUTH TABLE(1-8) (1CE option)

NEXT CYCLE	ADDRESS	CE	ADSP	ADSC	ADV	WRITE	ŌĒ	DQ
Deselected	None	Н	Χ	L	Χ	Х	Х	High-Z
Read, Begin Burst	External	L	L	Χ	Χ	Χ	L	Q
Read, Begin Burst	External	L	L	Χ	Χ	Χ	Н	High-Z
Write, Begin Burst	External	L	Н	L	Χ	L	Χ	D
Read, Begin Burst	External	L	Н	L	Χ	Н	L	Q
Read, Begin Burst	External	L	Н	L	Χ	Н	Н	High-Z
Read, Continue Burst	Next	Χ	Н	Н	L	Н	L	Q
Read, Continue Burst	Next	Χ	Н	Н	L	Н	Н	High-Z
Read, Continue Burst	Next	Н	Χ	Н	L	Н	L	Q
Read, Continue Burst	Next	Н	Χ	Н	L	Н	Н	High-Z
Write, Continue Burst	Next	Χ	Н	Н	L	L	Χ	D
Write, Continue Burst	Next	Н	Χ	Н	L	L	Χ	D
Read, Suspend Burst	Current	Χ	Н	Н	Н	Н	L	Q
Read, Suspend Burst	Current	Χ	Н	Н	Н	Н	Н	High-Z
Read, Suspend Burst	Current	Н	Χ	Н	Н	Н	L	Q
Read, Suspend Burst	Current	Н	Х	Н	Н	Н	Н	High-Z
Write, Suspend Burst	Current	Χ	Н	Н	Н	L	Х	D
Write, Suspend Burst	Current	Н	Х	Н	Н	L	Χ	D

#### NOTE:

- 1. X means "Don't Care." H means logic HIGH. L means logic LOW.
- 2. For WRITE, L means one or more byte write enable signals (BWa-h) and BWE are LOW or GW is LOW. WRITE = H for all BWx, BWE, GW HIGH.
- 3. BWa enables WRITEs to DQa's and DQPa. BWb enables WRITEs to DQb's and DQPb. BWc enables WRITEs to DQc's and DQPc. BWd enables WRITEs to DQd's and DQPd. DQPa-DQPd are available on the x36 version.
- 4. All inputs except OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
- 5. Wait states are inserted by suspending burst.
- 6. For a WRITE operation following a READ operation,  $\overline{\text{OE}}$  must be HIGH before the input data setup time and held HIGH during the input data hold time.
- 7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
- 8. ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE LOW or GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

#### PARTIAL TRUTH TABLE

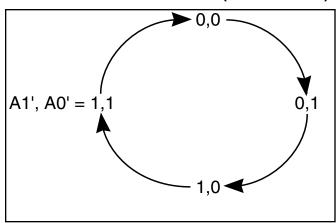
Function	GW	BWE	BWa	BWb	BWc	BWd
Read	Н	Н	Х	Х	Х	Х
Read	Н	L	Н	Н	Н	Н
Write Byte 1	Н	L	L	Н	Н	Н
Write All Bytes	Н	L	L	L	L	L
Write All Bytes	L	Х	Х	Х	Х	Х



#### **INTERLEAVED BURST ADDRESS TABLE (MODE = VDD or No Connect)**

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

## LINEAR BURST ADDRESS TABLE (MODE = VSS)

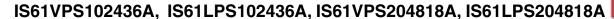


## **ABSOLUTE MAXIMUM RATINGS(1)**

Symbol	Parameter	Value	Unit
Тѕтс	Storage Temperature	-55 to +150	°C
PD	Power Dissipation	1.6	W
Іоит	Output Current (per I/O)	100	mA
VIN, VOUT	Voltage Relative to Vss for I/O Pins	-0.5 to V <sub>DDQ</sub> + 0.5	V
VIN	Voltage Relative to Vss for for Address and Control Inputs	-0.5 to V <sub>DD</sub> + 0.5	V
VDD	Voltage on VDD Supply Relative to Vss	-0.5 to 4.6	V

#### Notes:

- Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
- 3. This device contains circuitry that will ensure the output devices are in High-Z at power up.





**OPERATING RANGE (IS61LPSXXXXX)** 

Range	Ambient Temperature	<b>V</b> DD	VDDQ
Commercial	0°C to +70°C	3.3V <u>+</u> 5%	3.3V / 2.5V <u>+</u> 5%
Industrial	–40°C to +85°C	3.3V <u>+</u> 5%	3.3V / 2.5V <u>+</u> 5%

**OPERATING RANGE (IS61VPSXXXXX)** 

Range	Ambient Temperature	<b>V</b> DD	<b>V</b> DDQ
Commercial	0°C to +70°C	2.5V <u>+</u> 5%	2.5V <u>+</u> 5%
Industrial	–40°C to +85°C	2.5V <u>+</u> 5%	2.5V <u>+</u> 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			3.3V		2.5V			
Symbol	Parameter	<b>Test Conditions</b>	Min.	Max.	Min.	Max.	Unit	
Vон	Output HIGH Voltage	IOH = -4.0  mA  (3.3V) IOH = -1.0  mA  (2.5V)	2.4	_	2.0	_	V	
Vol	Output LOW Voltage	IoL = 8.0 mA (3.3V) IoL = 1.0 mA (2.5V)	_	0.4	_	0.4	V	
VIH	Input HIGH Voltage		2.0	VDD + 0.3	1.7	VDD + 0.3	V	
VIL	Input LOW Voltage		-0.3	8.0	-0.3	0.7	V	
lu	Input Leakage Current	$Vss \leq V_{IN} \leq V_{DD}{}^{(1)}$	-5	5	-5	5	μΑ	
ILO	Output Leakage Current	$\frac{Vss \le V_{OUT} \le V_{DDQ}}{OE} = V_{IH}$	-5	5	-5	5	μΑ	

# POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

					200 IAX	-1( M <i>A</i>		
Symbol	Parameter	Test Conditions	Temp. range	x18	x36	x18	x36	Unit
СС	AC Operating	Device Selected,	Com.	450	450	400	400 mA	
	Supply Current	$\overline{OE} = V_{IH}, ZZ \leq V_{IL},$	Ind.	475	475	450	450	
		All Inputs $\leq 0.2 V$ or $\geq V_{DD} - 0.2 V$ , Cycle Time $\geq$ txc min.	typ. <sup>(2)</sup>	3	90	3	40	
İsb	Standby Current	Device Deselected,	Com.	150	150	140	140	mA
	TTL Input	$V_{DD} = Max.,$ All Inputs $\leq V_{IL}$ or $\geq V_{IH},$ $ZZ \leq V_{IL}, f = Max.$	Ind.	160	160	150	150	
İsbi	Standby Current	Device Deselected,	Com.	110	110	110	110	mA
•	CMOS Input	$V_{DD} = Max.,$	Ind.	140	140	140	140	
	·	$\begin{aligned} &V\text{IN} \leq V\text{SS} + 0.2V \text{ or } \geq &V\text{DD} - 0.2V \\ &f = 0 \end{aligned}$	typ. <sup>(2)</sup>	7	5	7	5	

#### Note:

<sup>1.</sup> MODE pin has an internal pullup and should be tied to VDD or Vss. It exhibits ±100µA maximum leakage current when tied to ≤ Vss + 0.2V or  $\geq$  VDD - 0.2V.

<sup>2.</sup> Typical values are measured at Vcc = 3.3V, TA = 25°C and not 100% tested.



# CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
Cin	Input Capacitance	VIN = 0V	6	pF
Соит	Input/Output Capacitance	Vout = 0V	8	pF

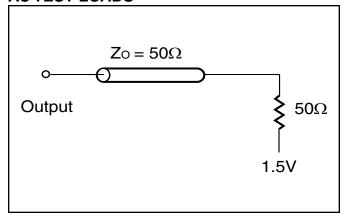
#### Notes:

- 1. Tested initially and after any design or process changes that may affect these parameters.
- 2. Test conditions:  $T_A = 25^{\circ}C$ , f = 1 MHz,  $V_{DD} = 3.3V$ .

## 3.3V I/O ACTEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing	1.5V
and Reference Level	
Output Load	See Figures 1 and 2

## **ACTEST LOADS**



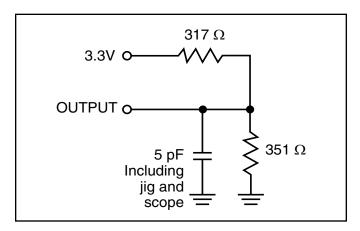


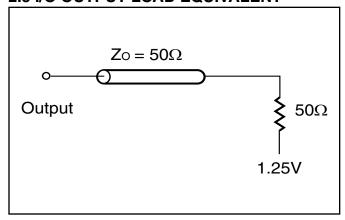
Figure 1 Figure 2



# 2.5V I/O ACTEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing	1.25V
and Reference Level	
Output Load	See Figures 3 and 4

# 2.5 I/O OUTPUT LOAD EQUIVALENT



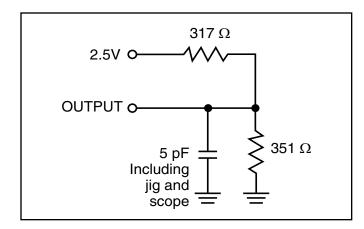
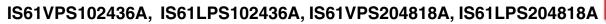


Figure 3 Figure 4





# READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-20	00	-166	-166		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	
fmax	Clock Frequency	_	200	_	166	MHz	
tĸc	Cycle Time	5	_	6	_	ns	
tкн	Clock High Time	2	_	2.4	_	ns	
tĸL	Clock Low Time	2	_	2.4	_	ns	
tkQ	Clock Access Time	_	3.1	_	3.5	ns	
tkqx <sup>(2)</sup>	Clock High to Output Invalid	1.5	_	1.5	_	ns	
tkqlz <sup>(2,3)</sup>	Clock High to Output Low-Z	1	_	1	_	ns	
tkqhz <sup>(2,3)</sup>	Clock High to Output High-Z	_	3.0	_	3.4	ns	
toeq	Output Enable to Output Valid	_	3.1	_	3.5	ns	
toeqx(2)	Output Disable to Output Invalid	0	_	0	_	ns	
toelz(2,3)	Output Enable to Output Low-Z	0	_	0	_	ns	
toehz <sup>(2,3)</sup>	Output Disable to Output High-Z	_	3.0	_	3.4	ns	
tas	Address Setup Time	1.4	_	1.5	_	ns	
tss	Address Status Setup Time	1.4	_	1.5	_	ns	
tws	Read/Write Setup Time	1.4	_	1.5	_	ns	
tces	Chip Enable Setup Time	1.4	_	1.5	_	ns	
tavs	Address Advance Setup Time	1.4	_	1.5	_	ns	
tos	Data Setup Time	1.4	_	1.5	_	ns	
tah	Address Hold Time	0.4	_	0.5	_	ns	
tsн	Address Status Hold Time	0.4	_	0.3	_	ns	
twн	Write Hold Time	0.4	_	0.5	_	ns	
tсен	Chip Enable Hold Time	0.4	_	0.5	_	ns	
tavh	Address Advance Hold Time	0.4	_	0.5	_	ns	
tон	Data Hold Time	0.4	_	0.5	_	ns	
tpds	ZZ High to Power Down	_	2	_	2	сус	
tpus	ZZ Low to Power Down	_	2	_	2	сус	

#### Note:

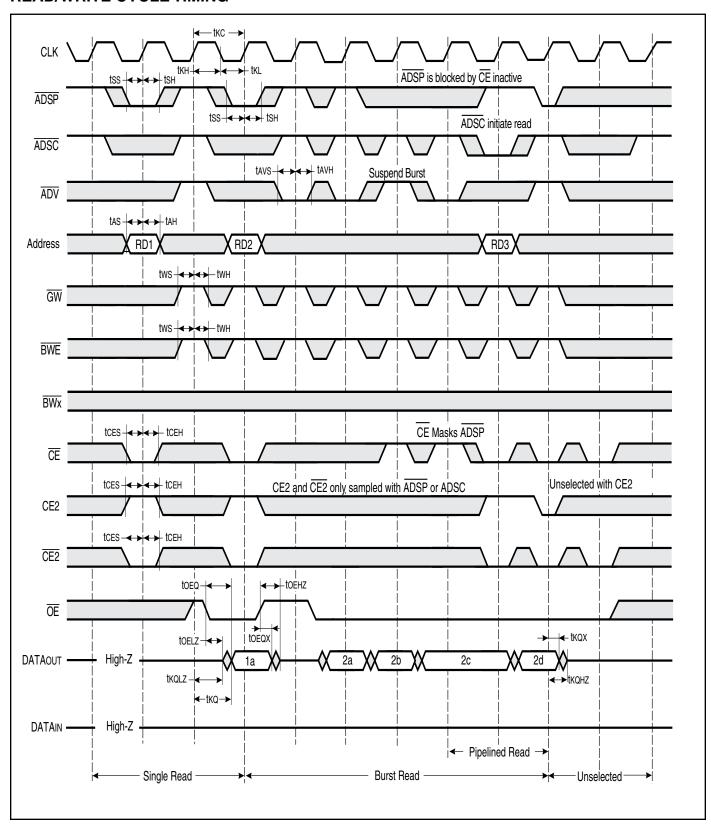
<sup>1.</sup> Configuration signal MODE is static and must not change during normal operation.

<sup>2.</sup> Guaranteed but not 100% tested. This parameter is periodically sampled.

<sup>3.</sup> Tested with load in Figure 2.

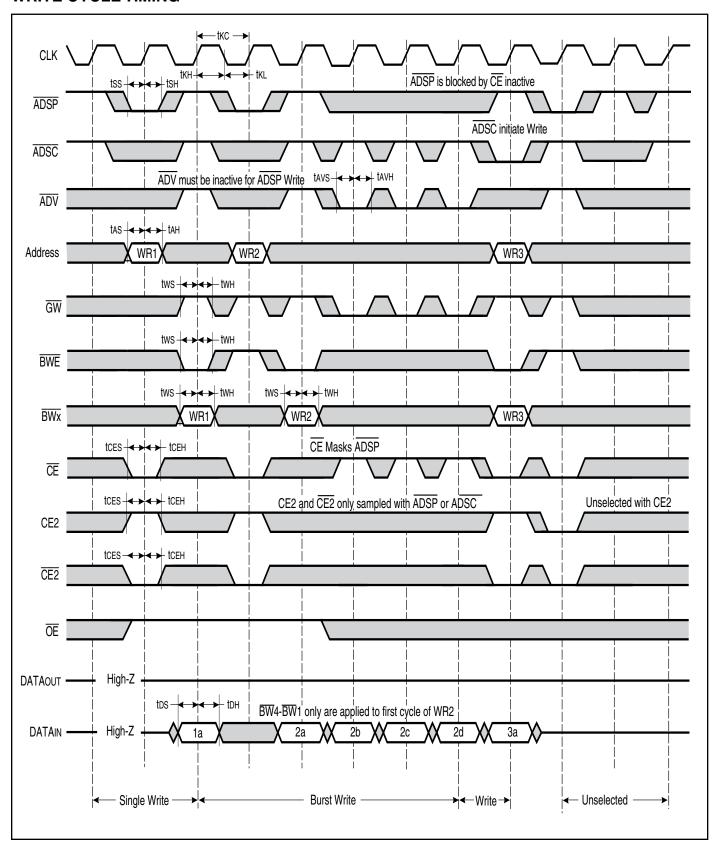


#### **READ/WRITE CYCLE TIMING**





#### WRITE CYCLE TIMING

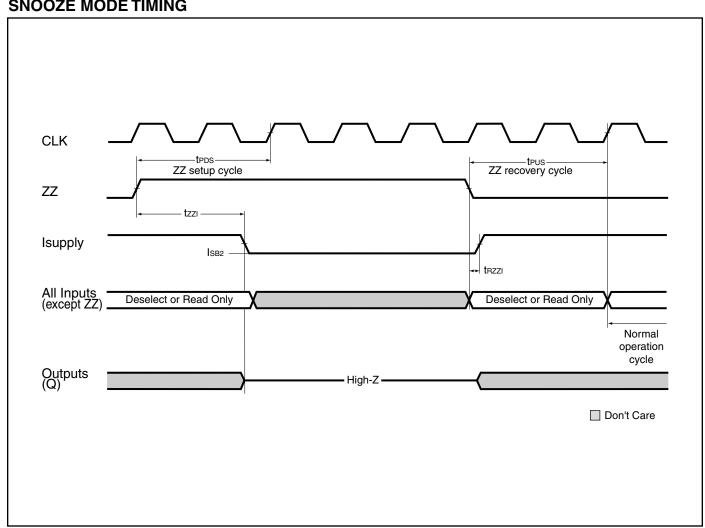




# **SNOOZE MODE ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Temperature	Conditions	Min.	Max.	Unit
ISB2	Current during SNOOZE MODE	Com.	$ZZ \ge Vih$	_	60	mA
		Ind.		_	90	
tpds	ZZ active to input ignored			_	2	cycle
tpus	ZZ inactive to input sampled			2	_	cycle
tzzı	ZZ active to SNOOZE current			_	2	cycle
trzzi	ZZ inactive to exit SNOOZE current			0	_	ns

## **SNOOZE MODE TIMING**







# ORDERING INFORMATION (3.3V core/2.5V-3.3V I/O)

Commercial Range: 0°C to +70°C

Configuration	Frequency	Order Part Number	Package	
1Mx36				_
	166	IS61LPS102436A-166TQ IS61LPS102436A-166TQL	100 TQFP 100 TQFP, Lead-free	
		IS61LPS102436A-166B3	165 PBGA	
2Mx18				
	166	IS61LPS204818A-166TQ IS61LPS204818A-166TQL	100 TQFP 100 TQFP, Lead-free	
		IS61LPS204818A-166B3	165 PBGA	

# Industrial Range: -40°C to +85°C

Configuration	Frequency	Order Part Number	Package	
1Mx36				
	166	IS61LPS102436A-166TQI IS61LPS102436A-166TQLI	100 TQFP 100 TQFP, Lead-free	
		IS61LPS102436A-166B3I IS61LPS102436A-166B3LI	165 PBGA 165 PBGA, Lead-free	
2Mx18				
	166	IS61LPS204818A-166TQI	100 TQFP	
		IS61LPS204818A-166B3I	165 PBGA	





# ORDERING INFORMATION (2.5V core/2.5V I/O)

Commercial Range: 0°C to +70°C

Configuration	Frequency	Order Part Number	Package
1Mx36			
	166	IS61VPS102436A-166TQ IS61VPS102436A-166TQL	100 TQFP 100 TQFP, Lead-free
		IS61VPS102436A-166B3	165 PBGA
2Mx18			
	166	IS61VPS204818A-166TQ IS61VPS204818A-166TQL	100 TQFP 100 TQFP, Lead-free
		IS61VPS204818A-166B3	165 PBGA

Industrial Range: -40°C to +85°C

Configuration	Frequency	Order Part Number	Package	
2Mx18				
	166	IS61VPS204818A-166TQI	100 TQFP	
		IS61VPS204818A-166B3I	165 PBGA	



