SSRAM Controller for Altera DE-Series Boards

For Quartus Prime 16.0

1 Core Overview

The SSRAM Controller communicates with the 1M × 36 synchronous CMOS static RAM (SSRAM) chip on Altera's DE2i-150 Board. It provides a convenient byte-addressable interface for using the SSRAM chip on the DE2i-150 board.

2 Functional Description

By mapping Avalon® Switch Fabric signals to the SSRAM chip, the SSRAM Controller enables users to read or write the SSRAM from a master device (such as the Nios® II processor) as a normal memory operation. The Avalon Switch Fabric handles addressing automatically and 8, 16 and 32-bit read/write transfers are supported. A write operation takes 13 cycles, and a read operation takes 10 cycles.

The SRAM Controller supports a clock frequency of 50 MHz, which is readily available on the DE2i-150 Board.

3 Instantiating the Core

The SSRAM Controller can be instantiated in a system using Qsys. There is no need to configure the controller. Once instantiated the user can use the SSRAM in the same way as using an On-Chip Memory. Any read or write operation to an address within the SSRAM Controller's address range will be read or written to the SSRAM on the DE2i-150 boards. Note that the SSRAM Controller has a longer read/write latency than the On-Chip Memory and needs two transfers for 32-bit data, hence it is not recommended for designs that require fast memory response.