EXPERIMENT – 1

Observation of Constellation Diagram and Study of Bandwidth efficiency of QAM

Objective:

a. To study the Constellation Diagram of QAM
b. Study of Bandwidth Efficiency in Quadrature Amplitude Modulation techniques

Equipment's:

- Experimental kit DCL-QAM
- Connecting chords
- Power supply
- 20MHz Dual trace Oscilloscope

THEORY:

The constellation diagram or geometrical representation is as shown in fig 3.2 below. The point in signal space corresponding to each of the eight possible transmitted signals is indicated by dots. For each such signal we can recover three bits rather than one. The distance of a signal point from the origin is √(Es)which is the square root of the signal energy associated with the symbol, that is Es=Ps * Ts = Ps(2Tb). As we know the ability to determine a bit without error is measured by the distance in signal space between points corresponding to the different values of the bit.

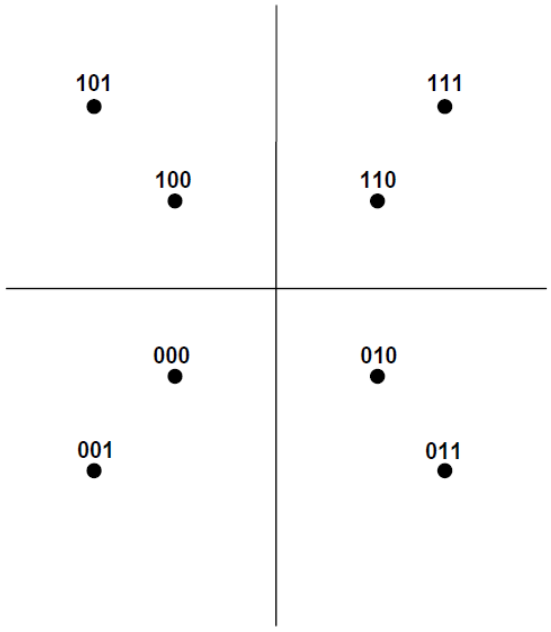


FIG 3.2 CONSTELLATION DIAGRAM

We note from fig. that points which differ in a single bit are separated by the distance d = 2√Ps Tb = 2√Eb where Eb is the energy contained in a bit transmitted for a time Tb. This distance for QPSK is the same as for BPSK. Hence, altogether, we have the important result that, in spite of the reduction by a factor of two in the bandwidth required by QPSK in comparison with BPSK, the noise immunity of the two systems are the same.

The number of dot points appearing in the constellation diagram depends on the number of symbol generated due to EVEN, ODD and C bit. The position of dot points in the quadrant of the constellation diagram is also depends on the symbol Generated due to the EVEN, ODD and C bit as shown above. The fig below shows examples of constellation diagram.

In fig 3.3 the data pattern used is 111001010011100101110000. If we plot the expected data pattern of EVEN, ODD and C bit as shown in fig, then there are 8symbols generated as 000, 001, 010, 011, 100, 101, 110, 111 thus there are 8dots appearing in the constellation diagram in all four quadrants.

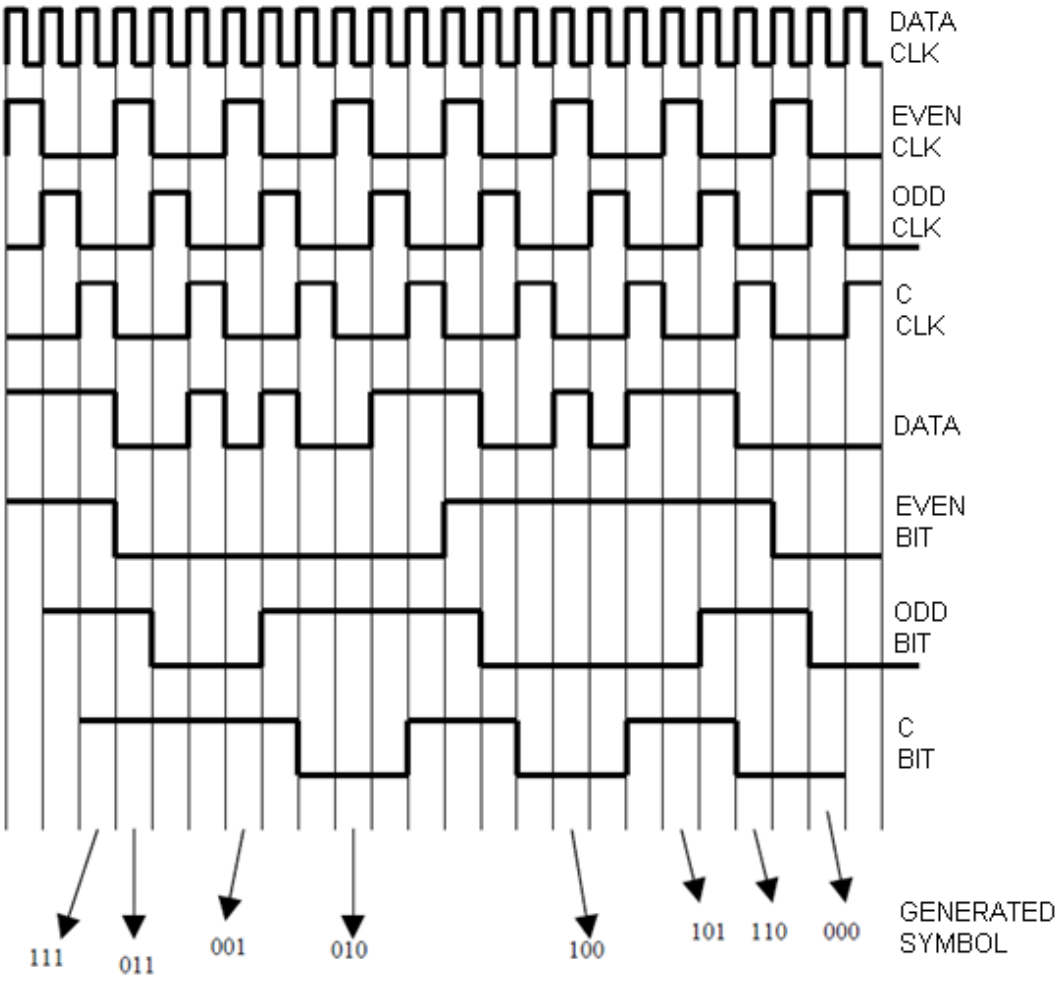


Fig 3.3

Bandwidth efficiency of QAM is defined by the ratio of bit transmission speed in QAM to Bandwidth of QAM signal. It is given by **Bandwidth Efficiency = Fb / Bw**

Where Fb is Bit transmission speed and Bw is the bandwidth of signal transmitted.

The more the bandwidth efficiency more is the data transfer within the same bandwidth of signal transmission.

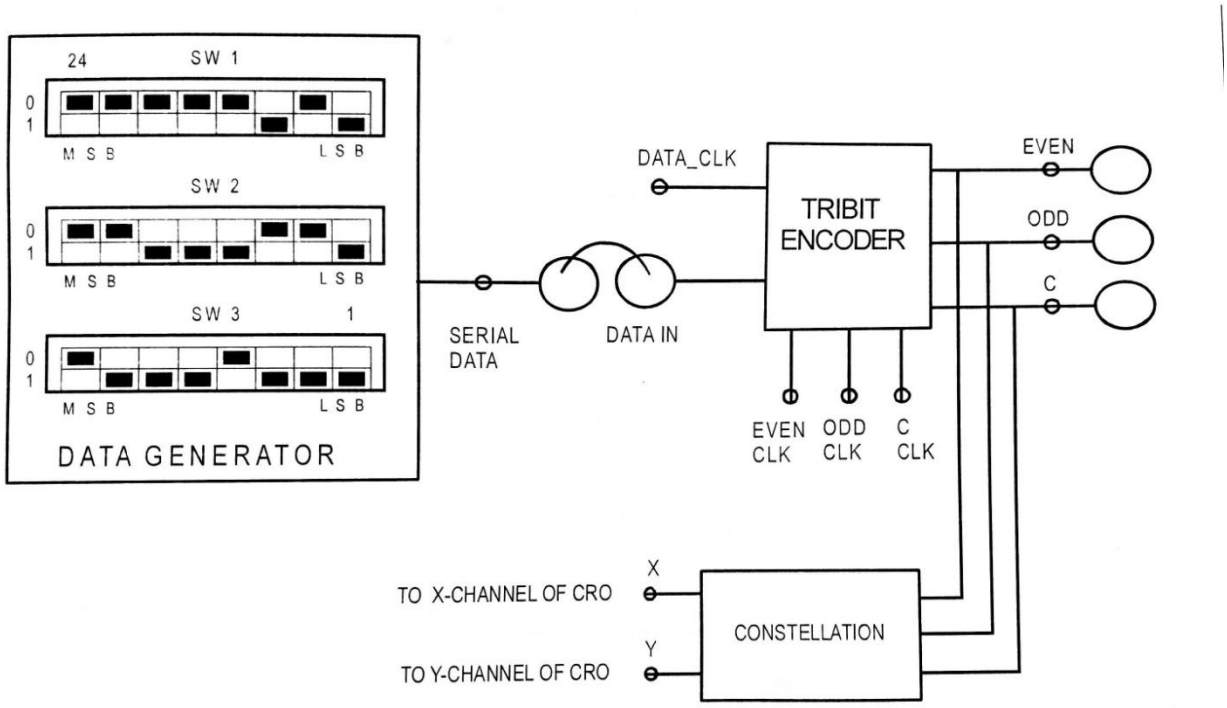


FIG 3.1 BLOCK DIAGRAM FOR OBSERVATION OF CONSTELLATION DIAGRAM

Procedure:

Study of Constellation Diagram

1. Carry out the connections and switch settings as in Block Diagram
2. Connect power supply in proper polarity to the kit DCL-QAM and switch it on.
3. Select Data pattern of simulated data using switch SW1, SW2, SW3
4. Connect SERIAL DATA generated to DATA IN of the TRIBIT ENCODER
5. Now connect X & Y port of CONSTELLATION BLOCK to X-channel and Y-channel of CRO respectively
6. Observe the waveforms.

Bandwidth efficiency of QAM technique

1. Measure the transmission clock at DATA_CLOCK post i.e. 256KHz

2. Divide this clock by the number of bits transmitted simultaneously, i.e. 3 bits in this case (EVEN, ODD, & C Bits)
3. Transmission clock is the bit transmission speed (256KHz) and Bandwidth of modulator is clock divide by the number of bits transmitted (i.e. 256KHz/3 = 85.33KHz)
4. From the above data, calculate bandwidth efficiency by substituting these values in the formula as follows;

Bandwidth Efficiency = Fb/Bw = 256K/85.33K = 3

CAPTURED WAVEFORM:

CH 1: DATA CLK (256 KHz) & CH 2: SERIAL DATA (000001010011100101110111)

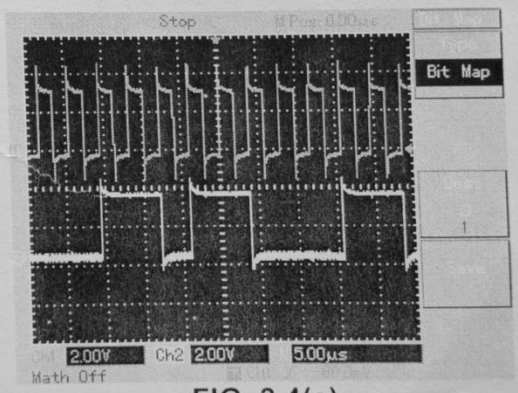


FIG. 3.4(a)

CH 1: EVEN CLK & CH 2: EVEN (TRIBIT ENCODER)

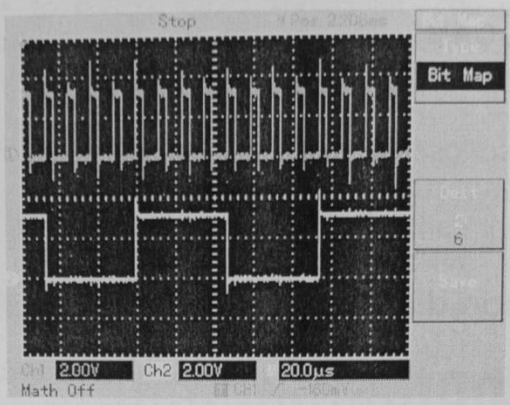


Fig.3.4(b)

CH 1: ODD CLK & CH 2: ODD (TRIBIT ENCODER)

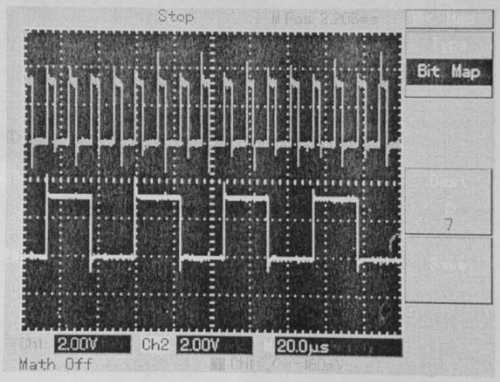


Fig.3.4(c)

CH 1: C CLK & CH 2: C (TRIBIT ENCODER)

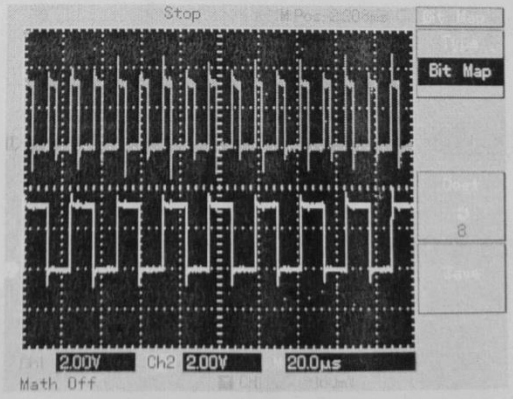


Fig.3.4(d)

SERIAL DATA: 000001010011100101110111
CH 1: X & CH 2: Y

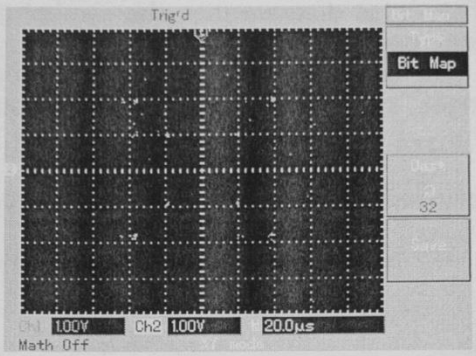


Fig. 3.4(e)

SERIAL DATA: 101010101010101010101010
CH 1: X & CH 2: Y

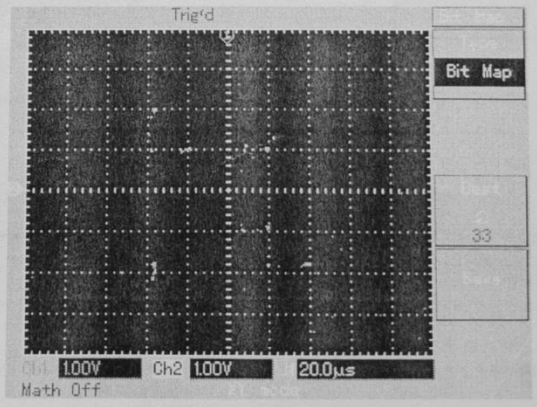
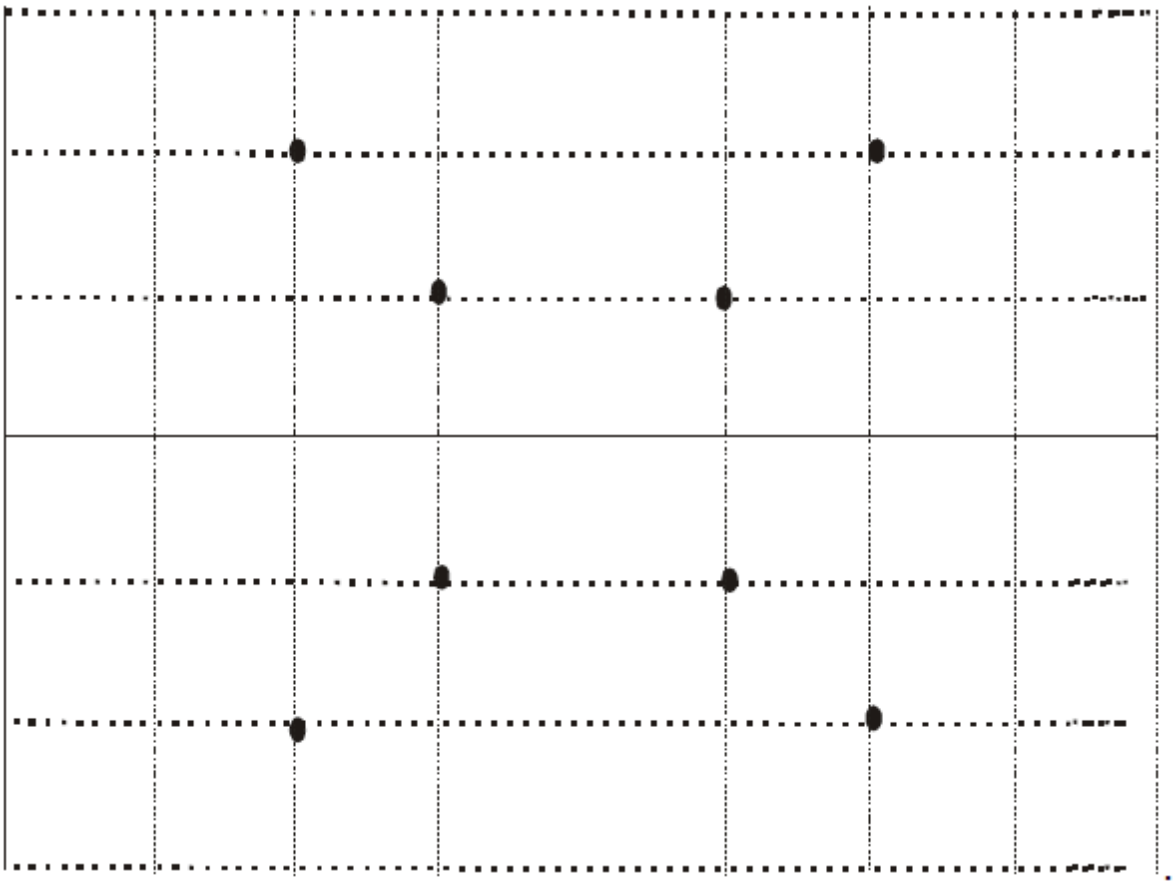


Fig. 3.4(f)



Conclusion:

EXPERIMENT NO: 2

NAME: QUADRATURE AMPLITUDE MODULATION TECHNIQUES

OBJECTIVE:

Study of Carrier Modulation Techniques by Quadrature Amplitude method

THEORY:

The QAM is a digital modulation where the information is contained into the phase as well as the amplitude of the transmitted carrier. In the 8-QAM the data are divided into the group of 3 bits (tribit), one of which will varies the amplitude of the carrier, the other two the phase. The modulated signal can take 4different phases and 2 different amplitudes, for a total of 8 different states. Similarly in the 16-QAM the data are divided into group of 4 bits (quad bit). The16 possible combinations change amplitude and phase of the carrier, which can take 16 different states.

A generator of 8-QAM signals for 3-bit symbol is shown in fig 4.2. For 8 QAM the main data source is divided into 3 bits called EVEN bit, ODD bit and C bit.

These three bits are called TRIBIT. These tribit together forms a symbol. We have 24 bit input data which gives 8 possible symbols. Among the 3 bits EVEN&ODD bit is responsible for phase modulation and the last bit (C bit) performs the amplitude modulation. The effect of each symbol on the final QAM signal is shown in the table below.

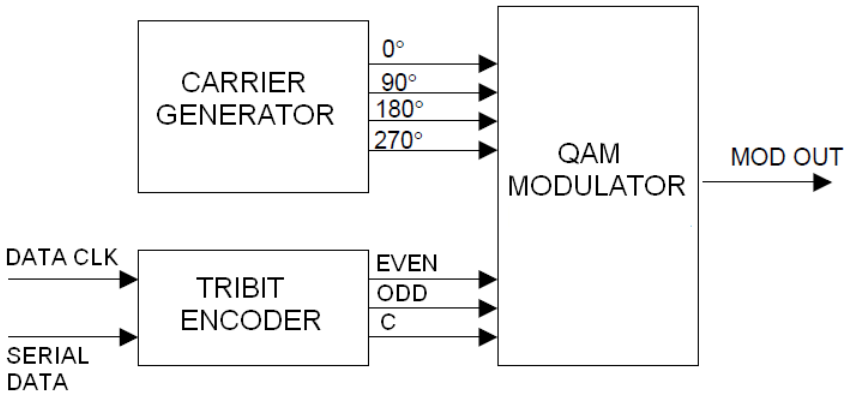


FIG 4.2 QAM MODULATOR

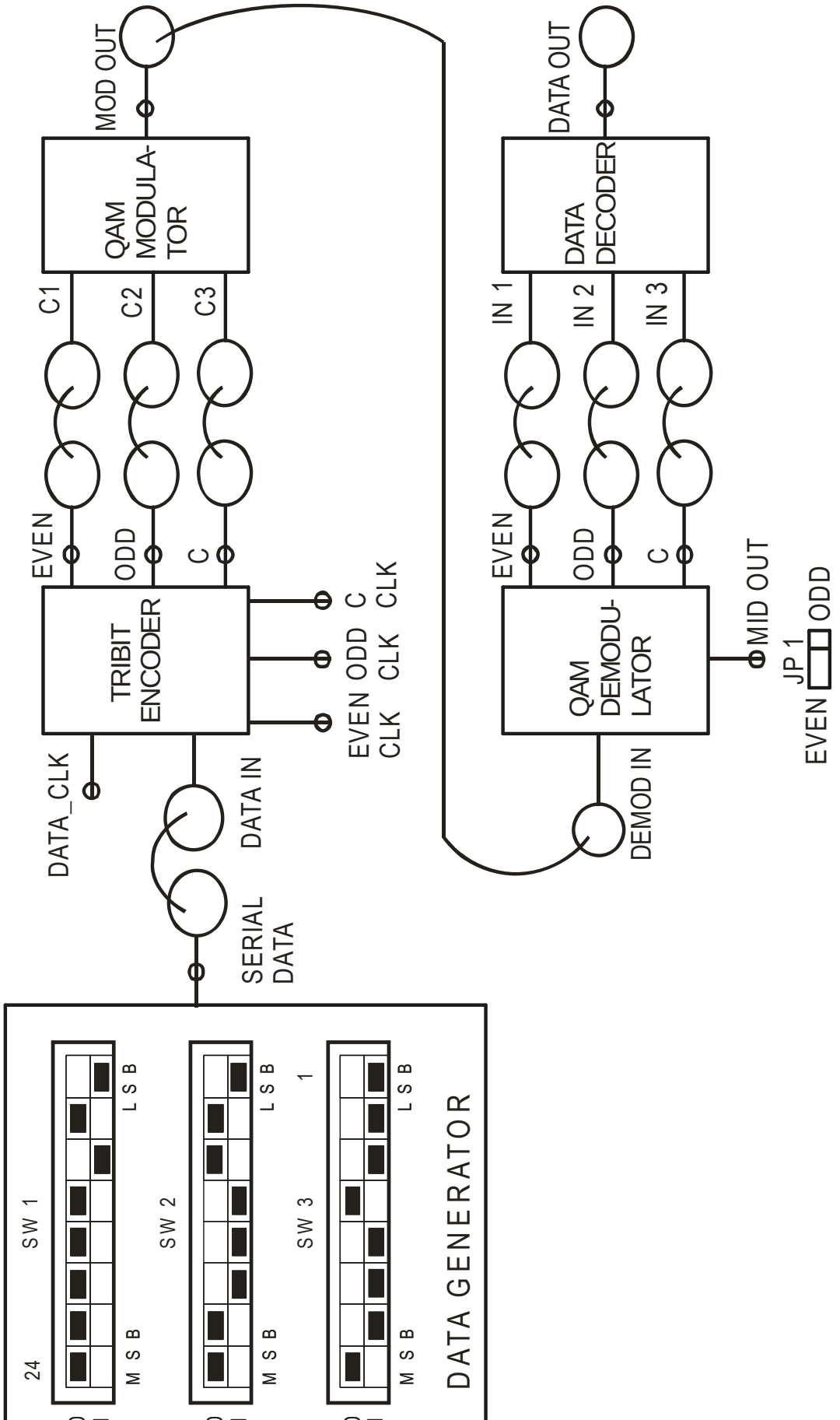


FIG 4.1 BLOCK DIAGRAM FOR QUADRATURE AMPLITUDE MODULATION TECHNIQUE

BINARY INPUT			QAM MOD OUT	
EVEN	ODD	C	AMPLITUDE	PHASE
0	0	0	1 V	180°
0	0	1	2 V	180°
0	1	0	1 V	90°
0	1	1	2 V	90°
1	0	0	1 V	270°
1	0	1	2 V	270°
1	1	0	1 V	0°
1	1	1	2 V	0°

The block diagram of the modulator used on the module is shown in the fig 4.1four 1MHz sine carriers, shifted between them of 90 deg, are applied to modulator. The data (signal EVEN, ODD and C) reach the modulator from the Tribit coder. The instantaneous value of EVEN, ODD and C data bit generates a symbol. Since EVEN, ODD and C can take either 0 or 1 value, maximum 8 possible symbols can be generated as shown in the above table. According to the symbol generated one of the four-sine carriers will be selected. The relation between the symbol generated and sine carrier is shown in table above.

A receiver for the QAM signal is shown in fig 4.1 Synchronous detection

is required and hence it is necessary to locally regenerate the carriers. The scheme for carrier regeneration is similar to BPSK. In that earlier case we used the multiplier and filter to recover the data.

The incoming signal is applied to the multipliers to remove the phase shift and to envelope detector for C bit recovery. The output of the multipliers can be seen at MID EVEN and MID OUT posts. The output of the multipliers is then given to filters, where we get the recovered EVEN and ODD data. These recovered EVEN&ODD bits having exactly same phase & frequency compared to transmitter EVEN&ODD bit. The C bit is recovered simply by passing the QAM modulated data through envelope detector. These recovered EVEN, ODD& C bits then applied to data decoder logic to recover the original NRZ-L data.

EQUIPMENTS:

- Experimental Kit **DCL-QAM**
- Connecting Chords.
- Power supply.
- 20MHz Dual Trace Oscilloscope.

PROCEDURE:

1. Refer to the block diagram (Fig 4.1) and carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-QAM** and switch it on.
3. Select Data pattern of simulated data using switch **SW1, SW2, SW3.**
4. Connect **SERIAL DATA** generated to **DATA IN** of the **TRIBIT ENCODER**.
5. Connect the tribit data **EVEN, ODD** &**C** to control input **C1, C2** and **C3** of **QAM MODULATOR** respectively.
6. Connect QAM modulated signal **MOD OUT** of the **QAM MODULATOR** to the **DEMOD IN** of the **QAM DEMODULATOR**.
7. Observe output of multipliers at **MID OUT** post of **QAM DEMODULATOR** by changing jumper (JP1) at **EVEN** and **ODD** position respectively.
8. Connect the demodulated data **EVEN, ODD&C of QAM DEMODULATOR** to IN1, IN2, and IN3of **DATA DECODER** respectively.
9. Observe the decoded data at **DATA OUT** post of **DATA DECODER**. Compare the decoded data with **SERIAL DATA**.
10. Observe various waveforms as mentioned below (Fig4.3).

OBSERVATION:

Observe the following waveforms on oscilloscope and plot it on the paper.

ON KIT **DCL-QAM**

1. Transmitter clock **DATA_CLK** with respect to NRZ-L coded data **SERIAL DATA** (Fig4.3(a))

2. **EVEN CLK** with respect to **ODD CLK.** (Fig4.3(b))
3. **EVEN CLK** with respect to **C CLK.** (Fig4.3(c))
4. **EVEN** data with respect to **EVEN CLK.** (Fig4.3(d))
5. **ODD** data with respect to **ODDCLK.** (Fig4.3(e))
6. **C** data with respect to **CCLK.** (Fig4.3(f))
7. Carrier signals **SIN 1,SIN 2, SIN 3**and **SIN 4.** (Fig4.3(g,h))
8. **QAM** modulated signal at **MOD OUT** of **QAMMODULATOR** with respect to **EVEN** of **TRIBITENCODER**. (Fig4.3(i))
9. **QAM** modulated signal at **MOD OUT** of **QAM MODULATOR** with respect to **C** of **TRIBIT ENCODER**. (Fig4.3(j))
10. Mid **EVEN** signal at **MID OUT** post of **QAM DEMODULATOR** with respect to **EVEN** of **TRIBITENCODER**. (Fig4.3(k))
11. Mid **ODD** signal at **MID OUT** post of **QAM DEMODULATOR** with respect to **ODD** of **TRIBIT ENCODER**. (Fig4.3(l))
12. **EVEN** of **QAM DEMODULATOR** with respect to **EVEN** of **TRIBIT ENCODER**. (Fig4.3(m))
13. **ODD** of **QAM DEMODULATOR** with respect to **ODD** of **TRIBIT ENCODER**. (Fig4.3(n))
14. **C** of **QAM DEMODULATOR** with respect to **C** of **TRIBIT ENCODER**. (Fig4.3(o))
15. **DATA OUT** with respect to **SERIAL DATA.** (Fig4.3(p))

CAPTURED WAVEFORM:

CH 1: DATA CLK (256 KHz) & CH 2: SERIAL DATA (000001010011100101110111)

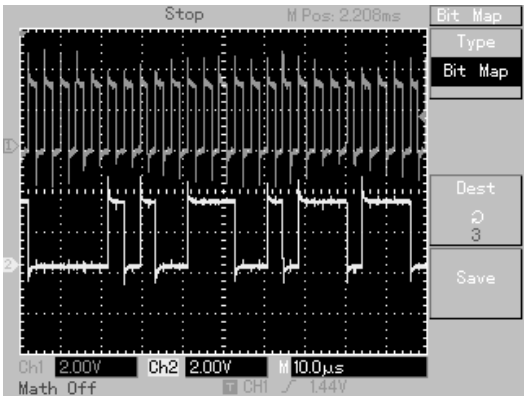


FIG. 4.3(a)

CH 1: EVEN CLK & CH 2: ODD CLK

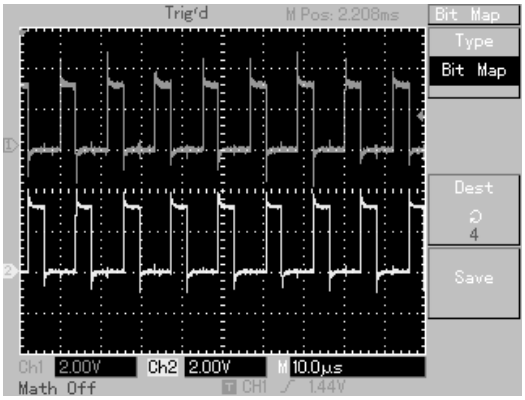


FIG. 4.3(b)

CH 1: EVEN CLK & CH 2: C CLK

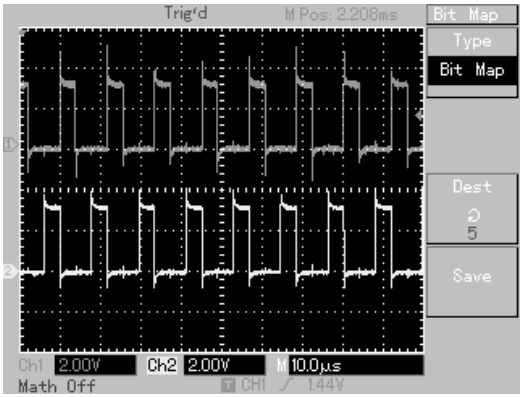


FIG. 4.3(c)

CH 1: EVEN CLK & CH 2: EVEN (TRIBIT ENCODER)

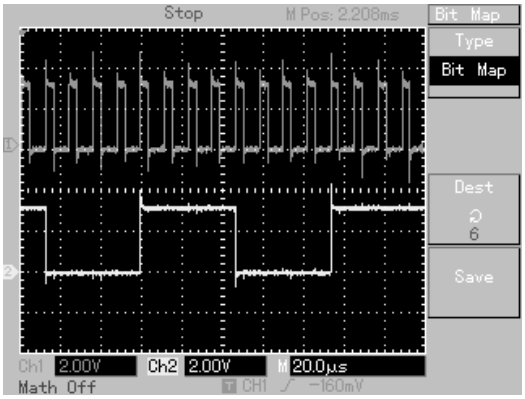


FIG. 4.3(d)

CH 1: ODD CLK & CH 2: ODD (TRIBIT ENCODER)

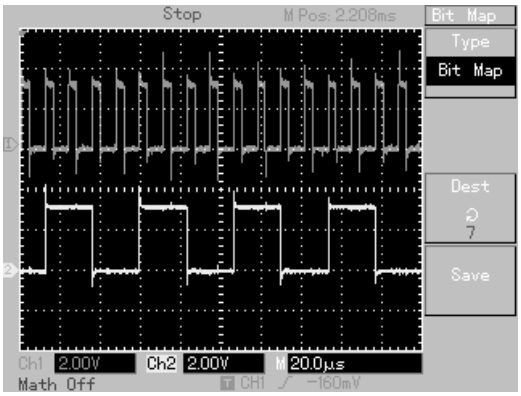


FIG. 4.3(e)

CH 1: C CLK & CH 2: C (TRIBIT ENCODER)

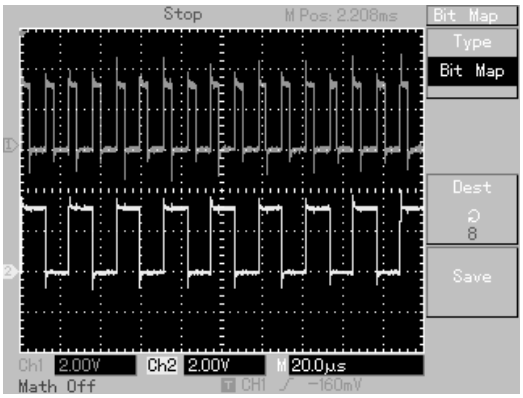


FIG. 4.3(f)

CH 1: SIN 1 (0º) & CH 2: SIN 2 (90º)

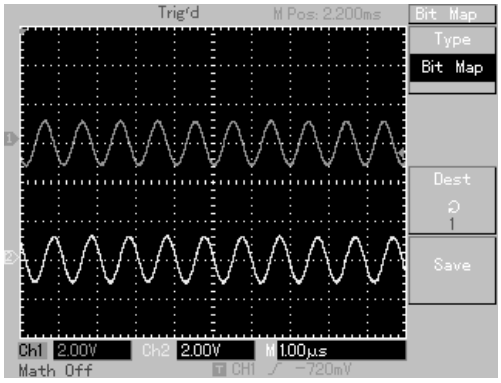


Fig.4.3 (g)

CH 1: SIN 3 (180º) & CH 2: SIN 4 (270º)

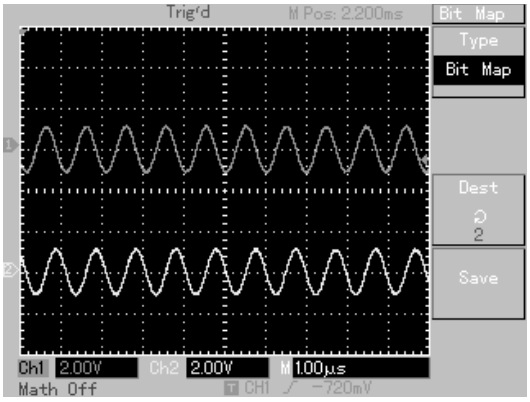


Fig.4.3 (h)

NOTE:

For **MOD OUT,** select a symbol using **EVEN** and **ODD** and then observe the **MOD OUT**. For waveform below a symbol is selected using **EVEN** and **ODD** and then **MOD OUT** is observed with respect to **EVEN.**

CH 1: EVEN (TRIBIT ENCODER) & CH 2: MOD OUT

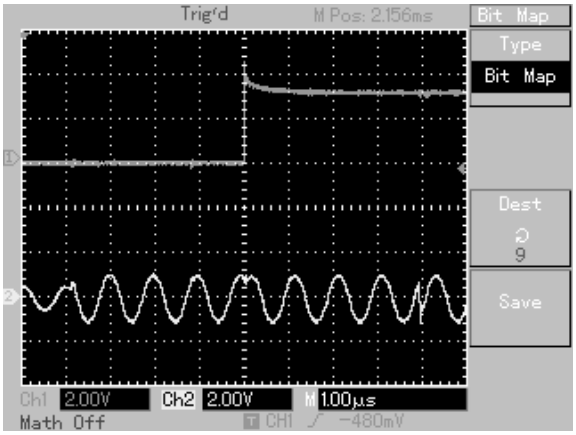


Fig.4.3(i)

CH 1: C(TRIBIT ENCODER) & CH 2: MOD OUT

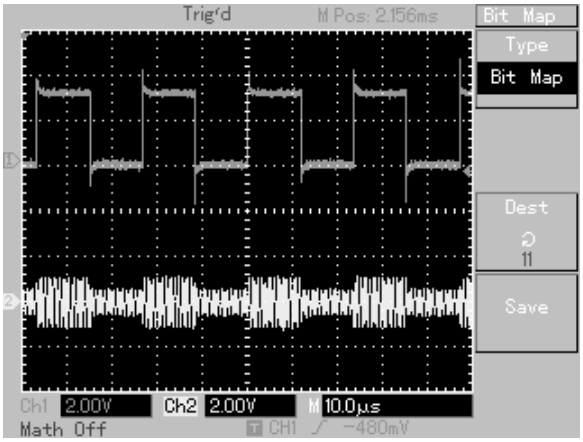


Fig.4.3(j)

CH 1: EVEN(TRIBIT ENCODER) & CH 2: MID OUT

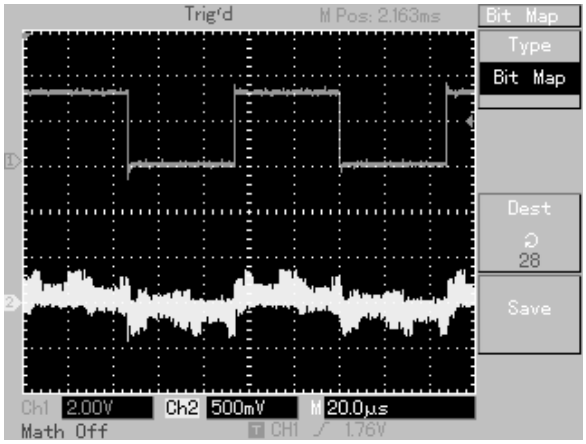


Fig.4.3(k)

CH 1: ODD (TRIBIT ENCODER) & CH 2: MID OUT

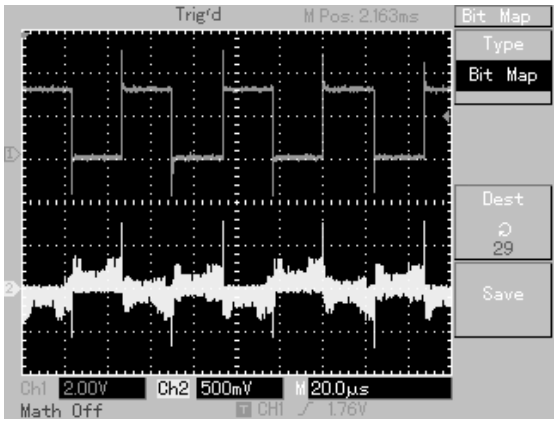


Fig.4.3(l)

CH 1: EVEN (TRIBIT ENCODER) & CH 2: EVEN(Demodulated)

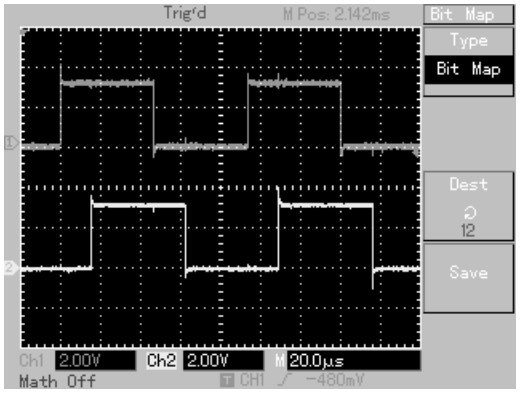


Fig.4.3(m)

CH 1: ODD(TRIBIT ENCODER) & CH 2: ODD(Demodulated)

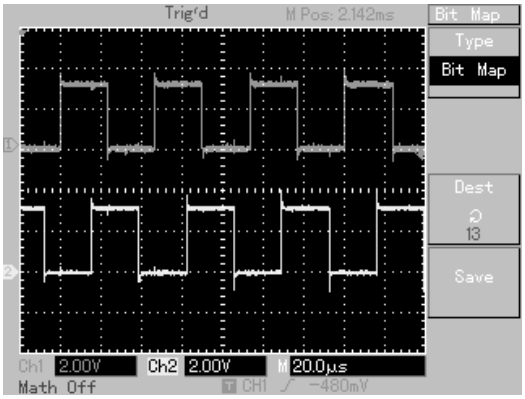


Fig.4.3(n)

CH 1: C(TRIBIT ENCODER) & CH 2: C(Demodulated)

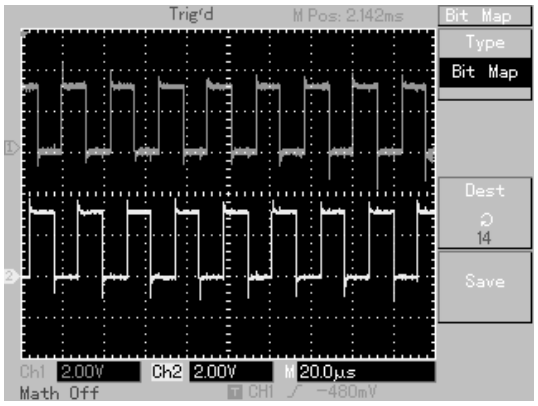


Fig.4.3(o)

CH 1: SERIAL DATA & CH 2: DATA OUT

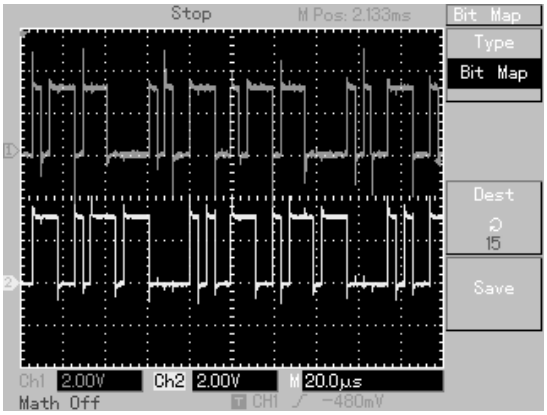


Fig.4.3(p)

CONCLUSION:

In BPSK we deal individually with each bit of duration Tb. In QAM we lump three bits together to form a SYMBOL. The symbol can have any one of eight possible values corresponding to three-bit sequence. We therefore arrange to make available for transmission eight distinct signals. At the receiver each signal represents one symbol and, correspondingly, three bits. When bits are transmitted, as in BPSK, the signal changes occur at the bit rate. When symbols are transmitted the changes occur at the symbol rate, which is one-third the bit rate. Thus the symbol time is Ts = 3Tb.

Experiment - 3

Study of GFSK Modulation and Demodulation

Objective: Study of GFSK Modulation and Demodulation

Equipments:

- Experimenter kit DCL-GFSK
- Connecting/Patch chords
- Power supply
- 20MHz Dual trace Oscilloscope

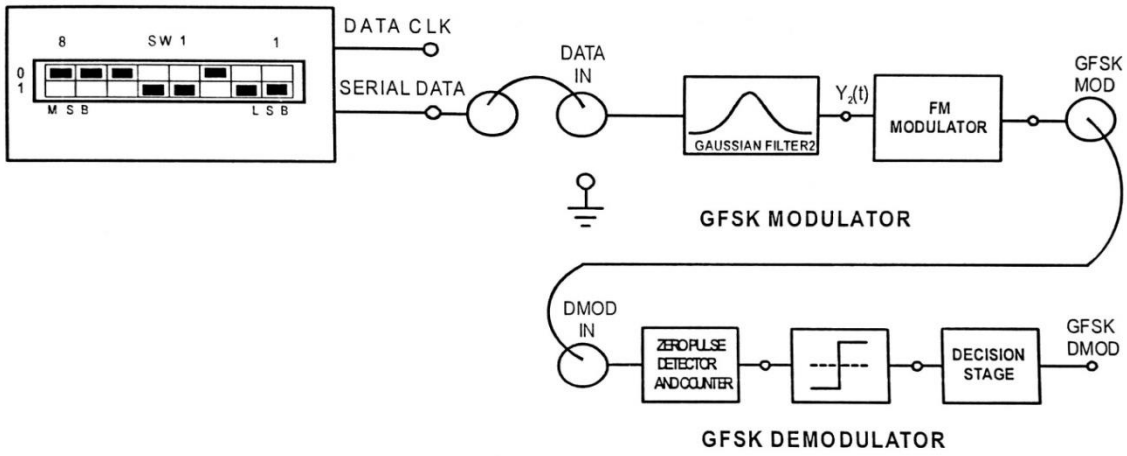


FIG 1.1 BLOCK DIAGRAM FOR GFSK MODULATION AND DEMODULATION

Procedure:

1. Carry out the connections and switch settings as in Block Diagram
2. Connect power supply in proper polarity to the kit DCL-GMSK and switch it on.
3. Select a Data pattern using switch SW1 of DATA GENERATOR BLOCK
4. Connect SERIAL DATA generated on board to DATA IN of GAUSSIAN FILTER2 of GFSK MODULATOR section
5. Observe GAUSSIAN shaped pulse at output of GAUSSIAN FILTER2 section and Modulated signal at output of GFSK MODULATOR section
6. For GFSK demodulation, connect GFSK MOD post to DMOD IN post of GFSK DEMODULATOR block and observe demodulated output.
7. Observe various waveforms at respective test points.

Filter's -3 dB cutoff = BT product x Bit rate
= 0.5 x 256 e3
= 128 e3
= 128 kHz

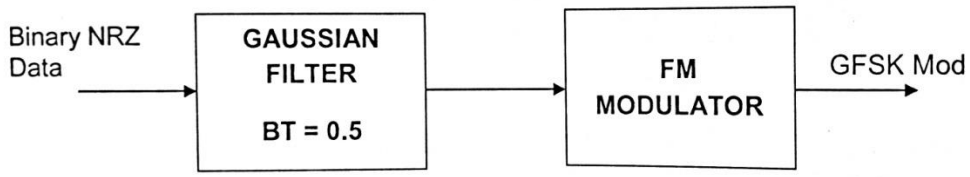


FIG. 1.2 GFSK MODULATOR

In DCL-GMSK, for GFSK modulation techniques, the modulated output shifts between frequencies as per table given.

$Y_2(t)$	GFSK MOD
0	2MHz
1	4MHz
0 to 1 OR 1 to 0 transition	In between 2 and 4 MHz

GFSK DEMODULATION:

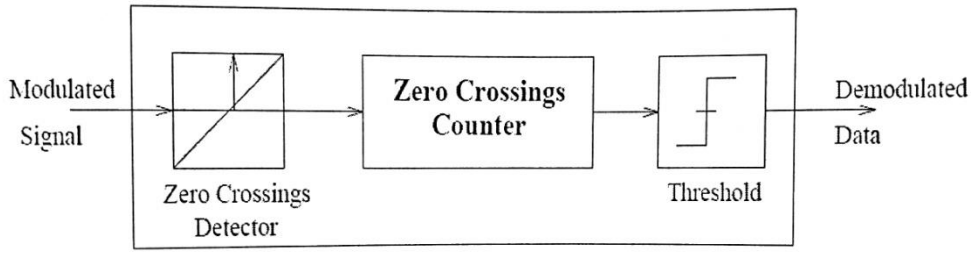


FIG. 1.3 GFSK DEMODULATOR

CAPTURED WAVEFORM

CH 1: DATA CLK (256 KHz) & CH 2: SERIAL DATA (00011011)

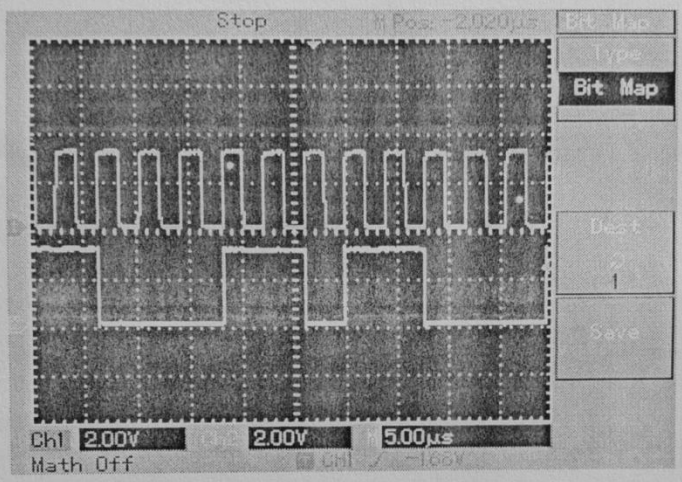


FIG. 1.4 (a)

CH 1: DATA IN & CH 2: Y_2 (t)

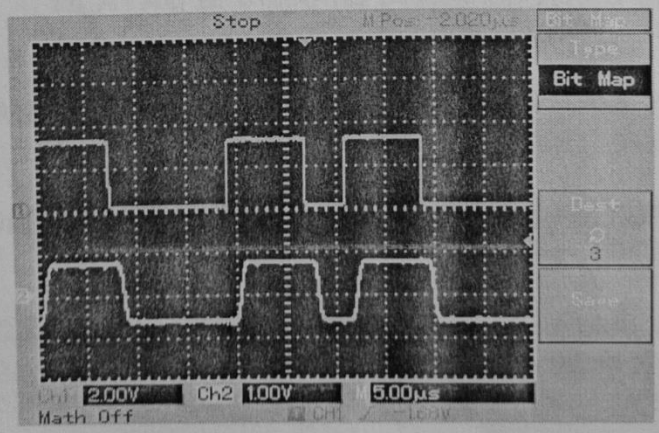


FIG. 1.4 (b)

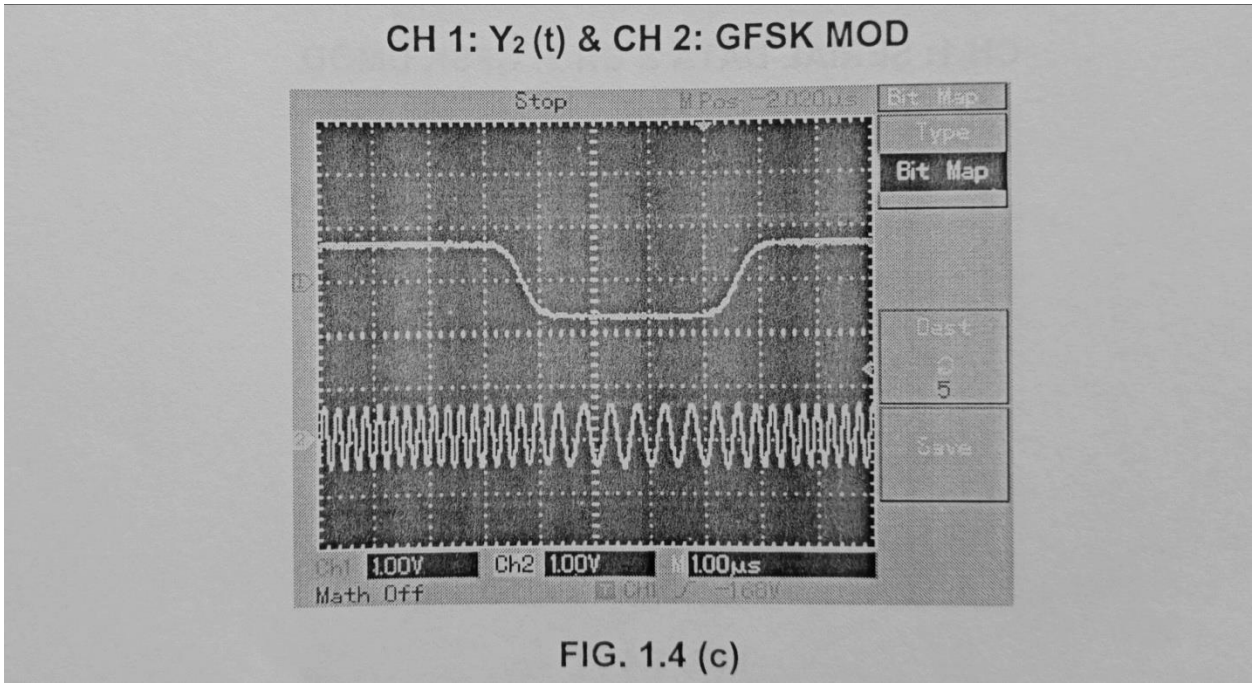


FIG. 1.4 (c)

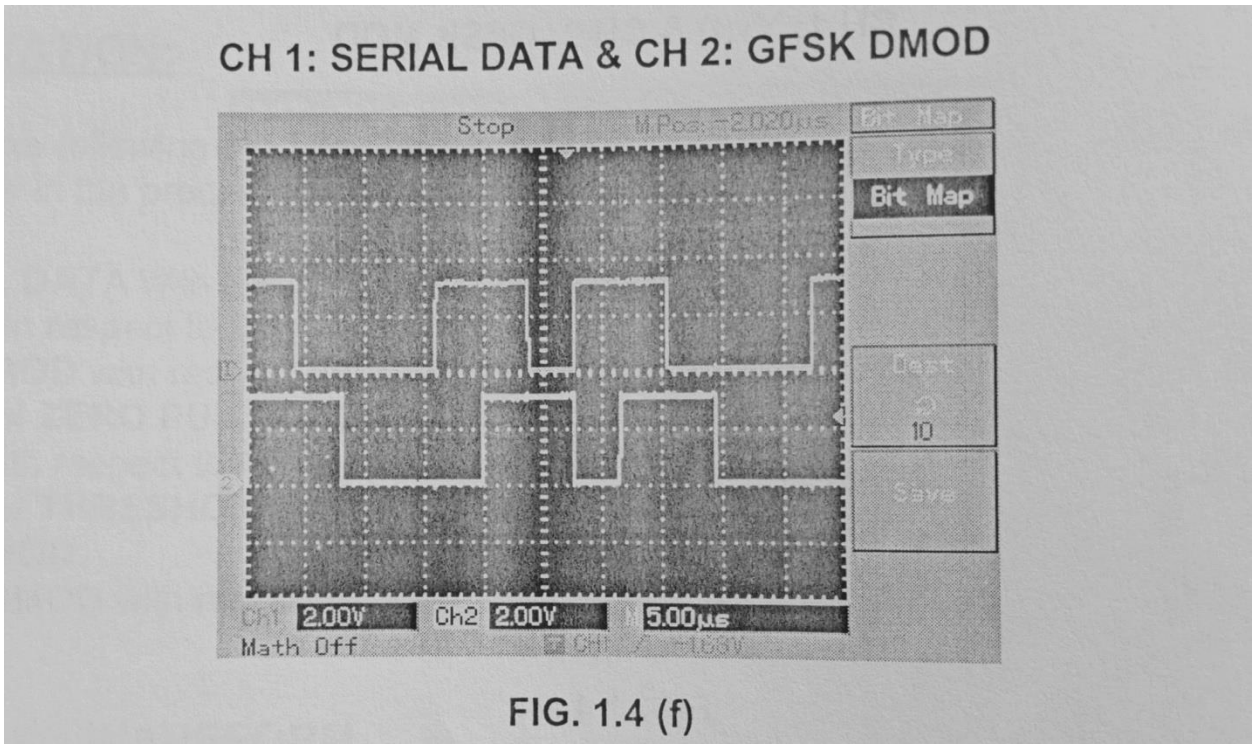


FIG. 1.4 (f)

Conclusion:

EXPERIMENT- 4

Study of GMSK Modulation and Demodulation

Objective: Study of GMSK Modulation and Demodulation

Equipments:

- Experimenter kit DCL-GMSK
- Connecting/Patch chords
- Power supply
- 20MHz Dual trace Oscilloscope

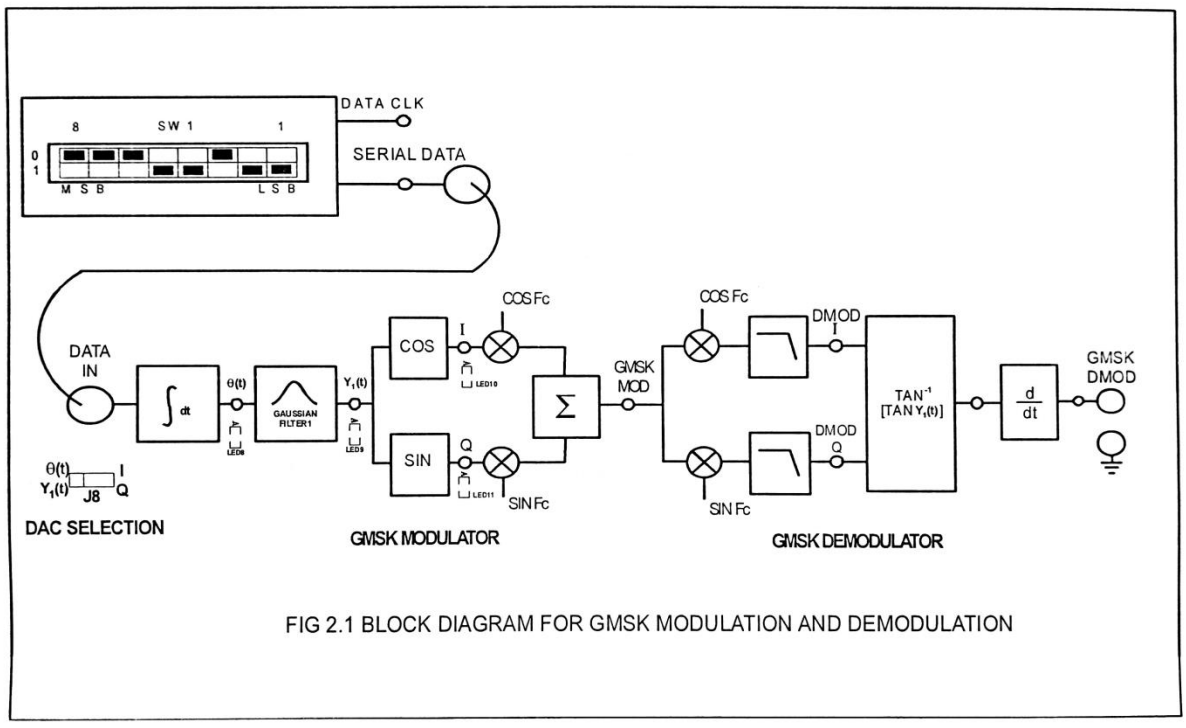


FIG 2.1 BLOCK DIAGRAM FOR GMSK MODULATION AND DEMODULATION

Procedure:

1. Carry out the connections and switch settings as in Block Diagram
2. Connect power supply in proper polarity to the kit DCL-GMSK and switch it on.
3. Select a Data pattern "00011011" using switch SW1 of DATA GENERATOR BLOCK
4. Connect SERIAL DATA generated on board to DATA IN of INTEGRATOR of GMSK MODULATOR section
5. Select the DAC selection jumper (J8) position as I block diagram to observe output of the GMSK MODULATOR. By setting the J8 jumper, the respective LEDs glow. When LED8 and LED9 glow then observe the output at $\theta(t)$ and $Y_1(t)$ test points. When LED 10 ad LED 11 glow then observe the output at I and Q test points.

6. Observe Modulated signal
7. Output of GMSK MODULATOR is connected to GMSK DEMODULATOR internally. Observe Demodulator output.

GMSK MODULATOR:

In DCL-GMSK for GMSK, Gaussian low pass filter has a BT product of 0.3. Accordingly, for a binary data rate of 256 Kbits/sec the filter's -3.0 dB Bandwidth is 76.8 kHz.

Filter's -3 dB cutoff = BT product x Bit rate
= 0.3 x 256 e3
= 76.8 e3
= 76.8 kHz

Modulation index is 0.5. The modulation index (μ) is the frequency deviation divided by bit rate. Therefore:

Frequency deviation = μ x bit rate
= 0.5 x 256 e3
= 0.128 e6
= 128 kHz

With a frequency deviation of 128 kHz, the RF carrier for a binary 0 will be offset -64 kHz, and a binary 1 will produce a +64 kHz offset.

Center Frequency = Fc = 512 KHz.

Frequency of the high frequency carrier = 512 KHz + 64 KHz = 576 KHz.

Frequency of the low frequency carrier = 512 KHz - 64 KHz = 448 KHz.

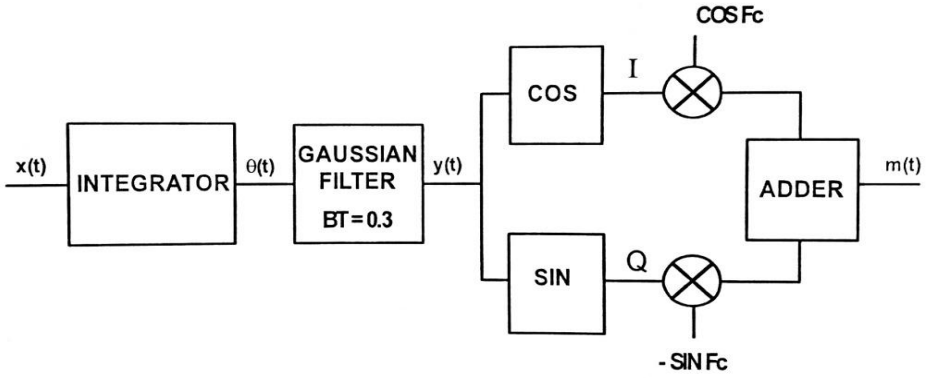


Fig. 2.2 GMSK Modulator Block Diagram

- Input NRZ sequence x(t) is fed to the Integrator.
- The Integrator integrates the NRZ sequence to give the phase plot.

$$\theta(t) = \int x(t)\, dt$$

- To smooth out the phase transition, output of Integrator is passed through the Gaussian Filter which gives the continuous phase change.

$$y(t) = h(t) * \theta(t)$$

- The I and Q components are obtained from Cos LUT and Sin LUT, using the Gaussian Filter output as an address. This I and Q are the quadrature components of the baseband GMSK equivalent signals.

$$I(t) = \cos [y(t)]$$
$$Q(t) = \sin [y(t)]$$

- By multiplying the I and Q components with the corresponding cos(Fc) and –sin(Fc) carriers the modulate I and Q signals are obtained .

- By adding these two modulated signals GMSK modulated signal is obtained.

$$m(t) = I(t)\cos(Fc) - Q(t)\sin(Fc)$$

GMSK DEMODULATOR:

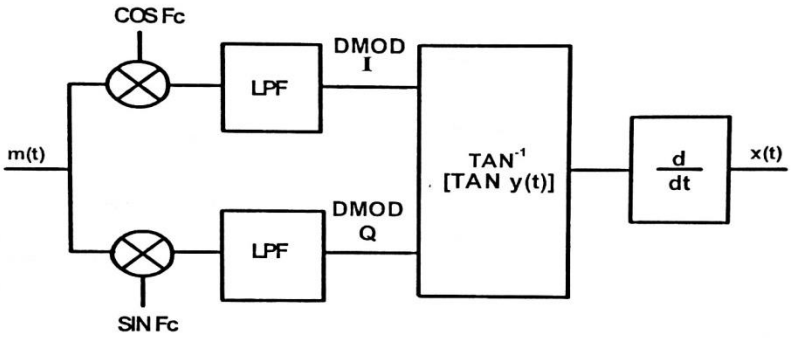


Fig. 2.3 GMSK Demodulator Block Diagram

- Modulated GMSK signal m(t) is fed to the GMSK DEMODULATOR.
- Multipliers at demodulator remove the phase from the modulated signal.
- Low Pass Filter by pass the high frequency component and follow the shape of its input. The demodulated I and Q are obtained at the output of Low Pass Filters.
- TAN^{-1} block is used to recover the phase plot.

$$\text{i.e. } \tan^{-1}[\tan y(t)] = y(t)$$

$$\text{where } \tan[y(t)] = \frac{\text{dmod Q}}{\text{dmod I}}$$

$$= \frac{\sin[y(t)]}{\cos[y(t)]}$$

- Derivator is used to recover the input NRZ signal.

$$x(t) = \frac{d\,y(t)}{dt}$$

CAPTURED WAVEFORM:

CH 1: DATA CLK (256 KHz) & CH 2: SERIAL DATA (00011011)

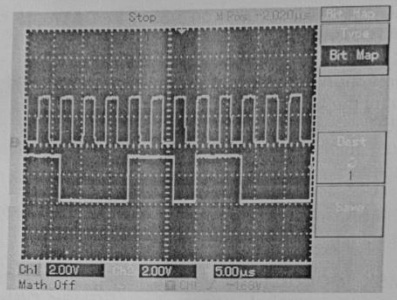


FIG. 2.4 (a)

CH 1: θ (t) & CH 2: Y_1 (t)

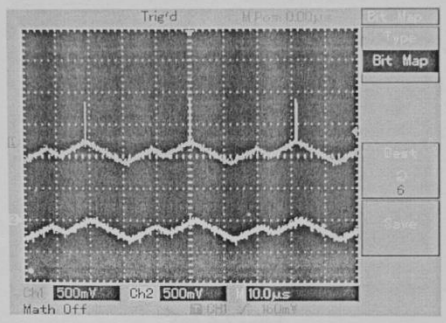


FIG. 2.4 (d)

CH 1: I & CH 2: Q

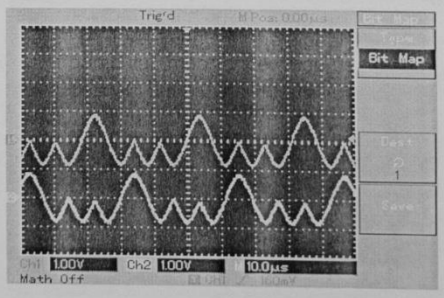


FIG. 2.4 (e)

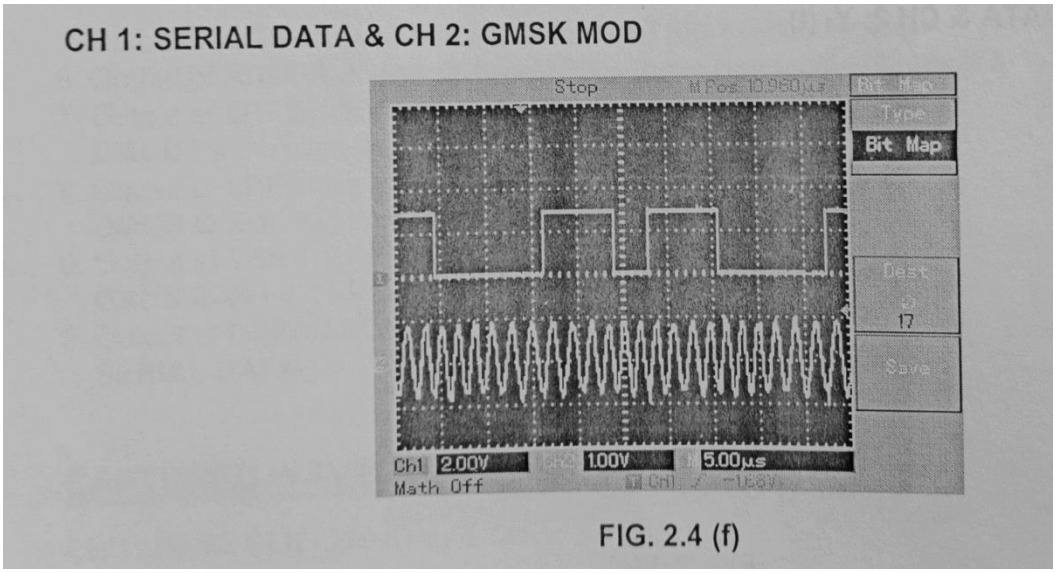


FIG. 2.4 (f)

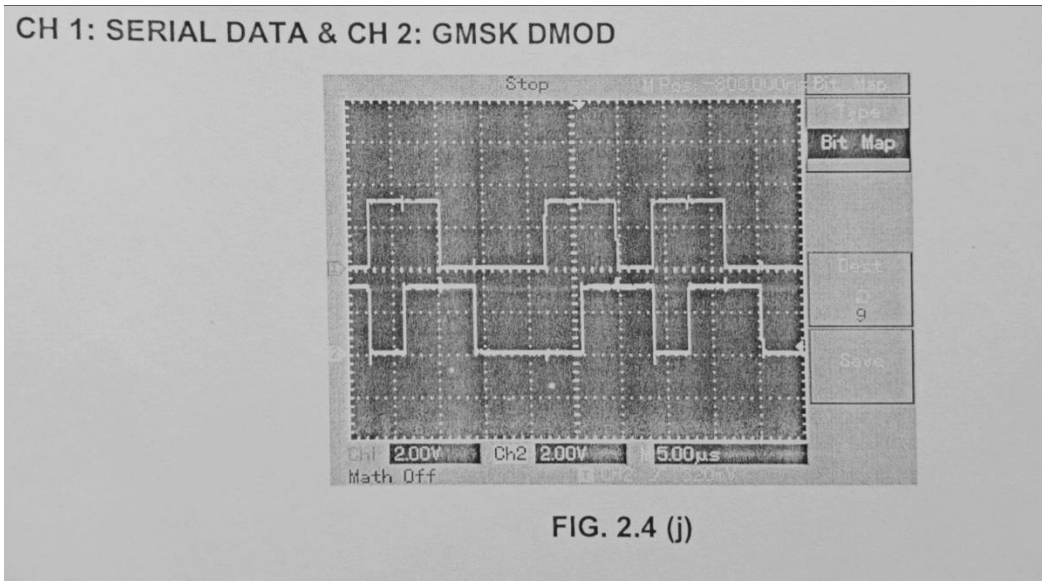


FIG. 2.4 (j)

Conclusion:

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EXPERIMENT-5
STUDY OF MSK MODULATION AND DEMODULATION

OBJECTIVE:

The objective of this experiment is to

a) Study MSK modulation and demodulation

b) Observe the constellation diagram of MSK

THEORY:

In digital modulation MSK is a type of continuous phase frequency shift keying. It uses changes in phase to represent 0's and 1's, with phase shift used depending on the previous phase value.

In MSK difference between higher and lower frequency is identical to half the bit rate. Consequently, the waveforms used to represent a 0 and 1 bit differ by exactly half a carrier period. This is the smallest FSK modulation index that can be chosen such that the waveforms of 0 and 1 are orthogonal.

EQUIPMENTS:

DCL CRC board

Equivalent power supply

BLOCK DIAGRAM:

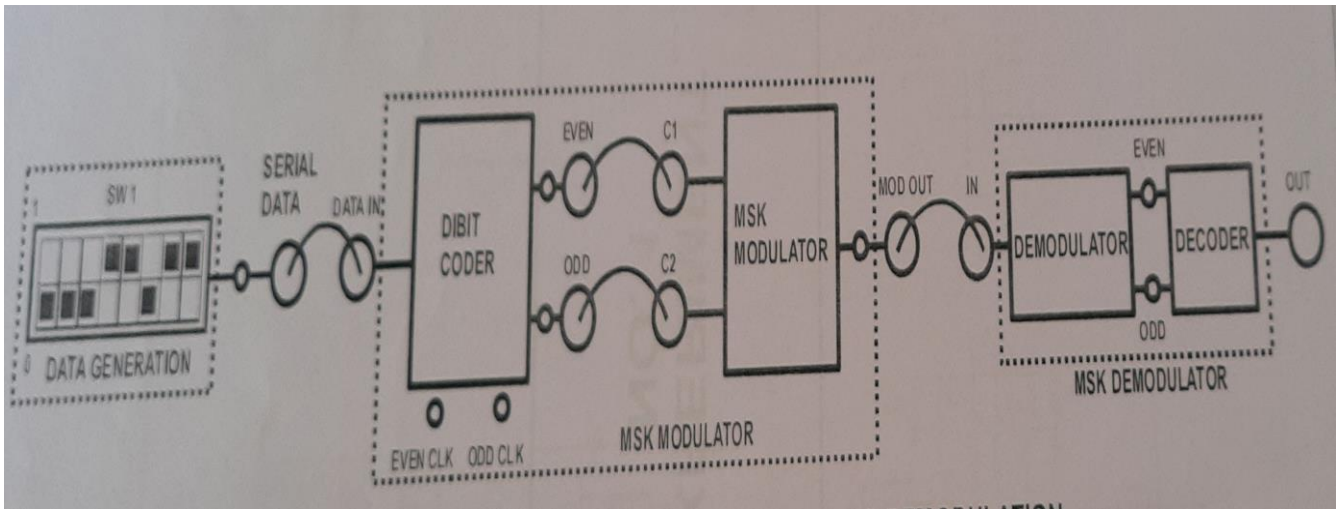


Fig: MSK modulator and demodulator

PROCEDURE:

a) Make the connections as shown in the block diagram

b) Connect the power supply to the kit and switch it ON

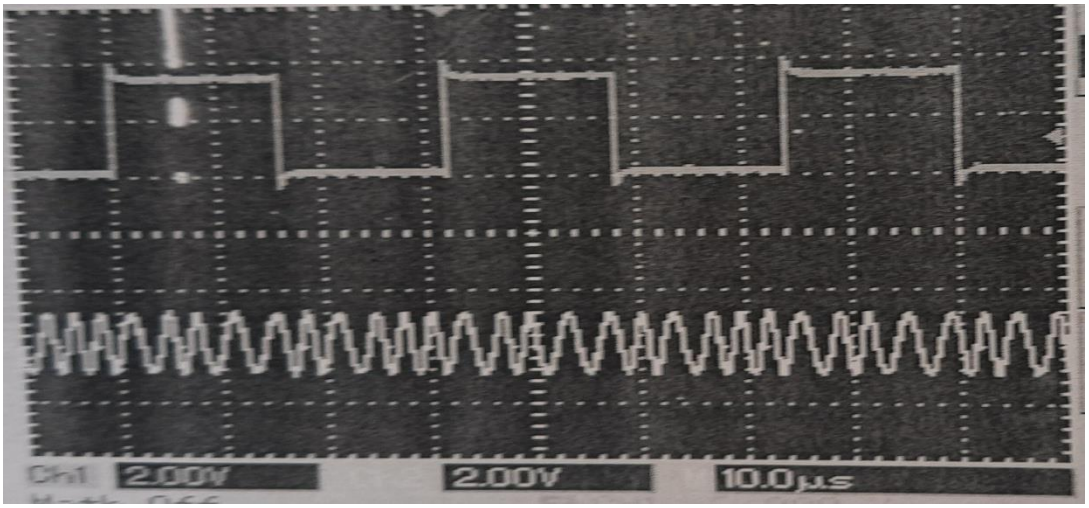
c) Set the data pattern as shown in block diagram using SW1.

d) Observe the MSK modulated signal at MOD OUT post of carrier modulator and demodulated signal at OUT post of MSK demodulator and compare it with original signal

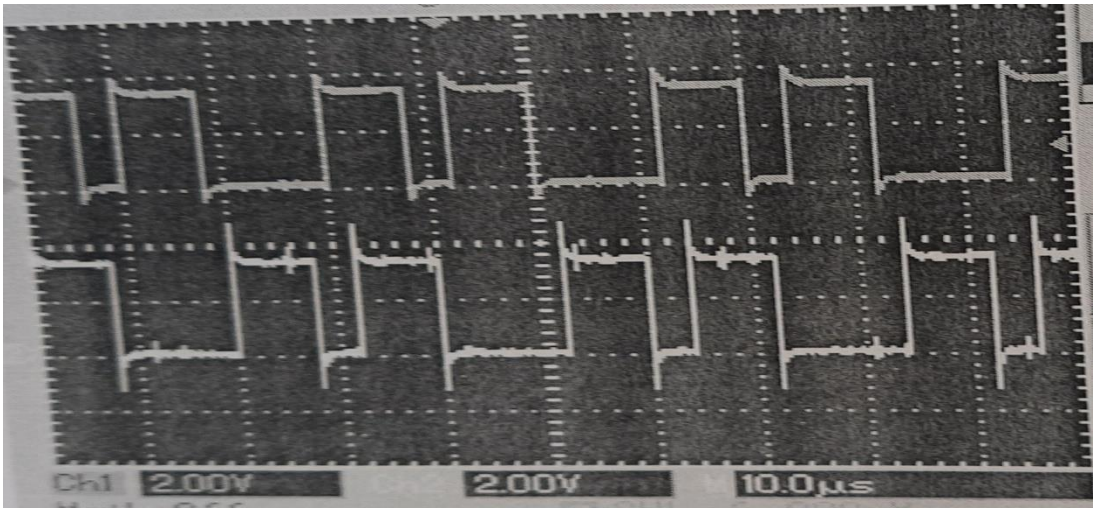
e) To observe the constellation diagram, connect X to CH1 and Y to CH2 and put oscilloscope display mode to X-Y

EXPECTED RESULTS/WAVEFORMS:

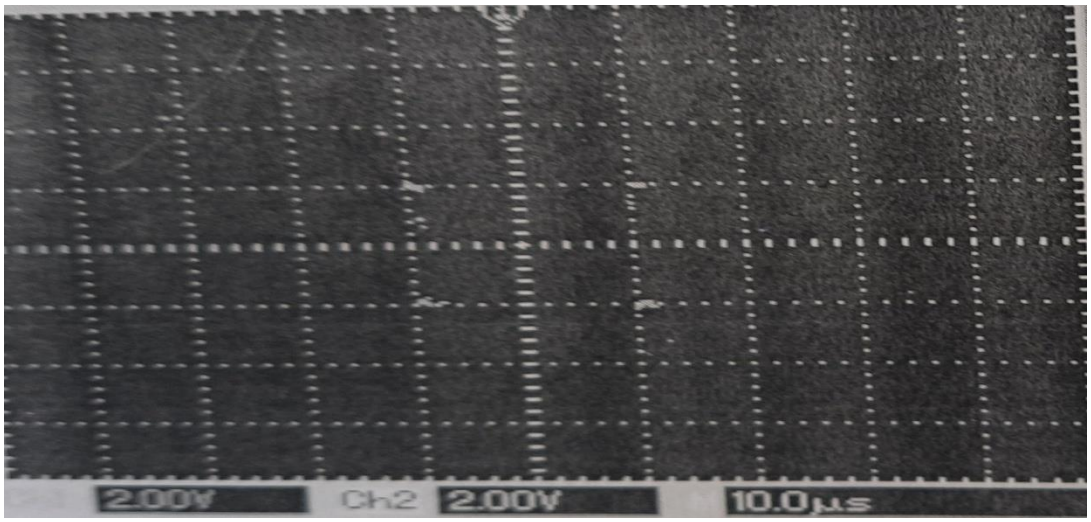
a) MSK MOD OUT



b) MSK DEMOD OUT



c) CONSTELLATION DIAGRAM



INFERENCE:

EXPERIMENT-6
STUDY OF CRC ENCODING AND DECODING

OBJECTIVE:

To study the cyclic redundancy code encoding and decoding

THEORY:

CRC is a non-secure hash function used to detect accidental changes to raw computer data and is commonly used in digital networks and storage devices. The algorithm for CRCs are based on cyclic codes. They accept data streams of any length as input, but always outputs a fixed length code. They are popular because they are simple to implement in binary hardware, are easy to analyze mathematically and are particularly good at detecting common errors caused by noise in transmission channels.

EQUIPMENTS:

DCL CRC board
Equivalent power supply

BLOCK DIAGRAM:

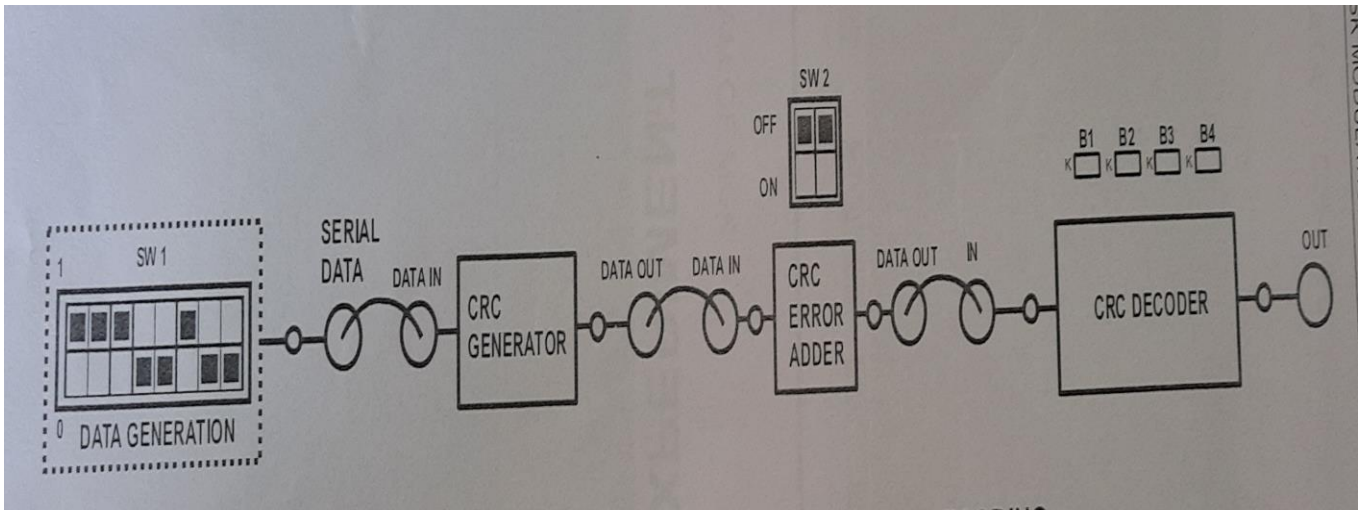


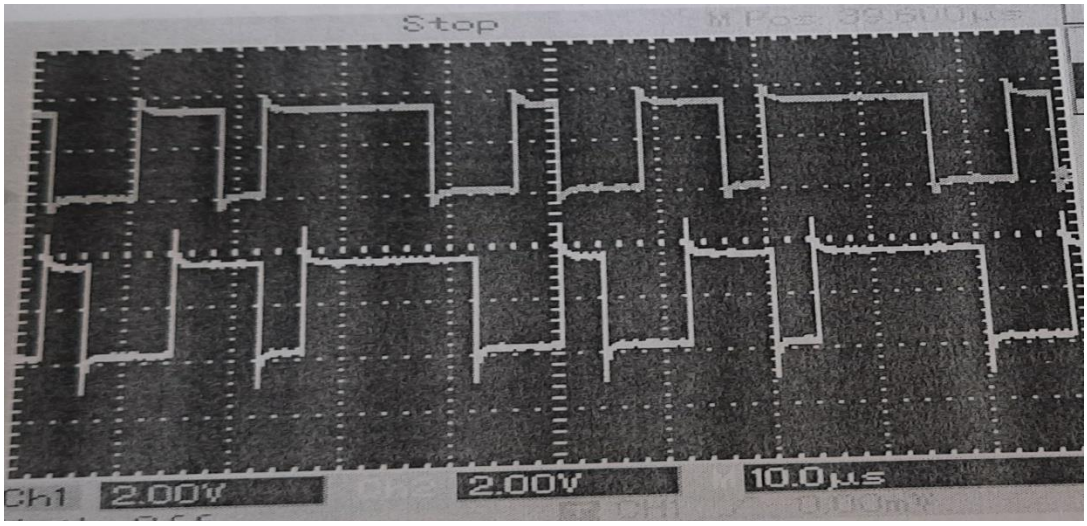
Fig: CRC encoder and decoder

PROCEDURE:

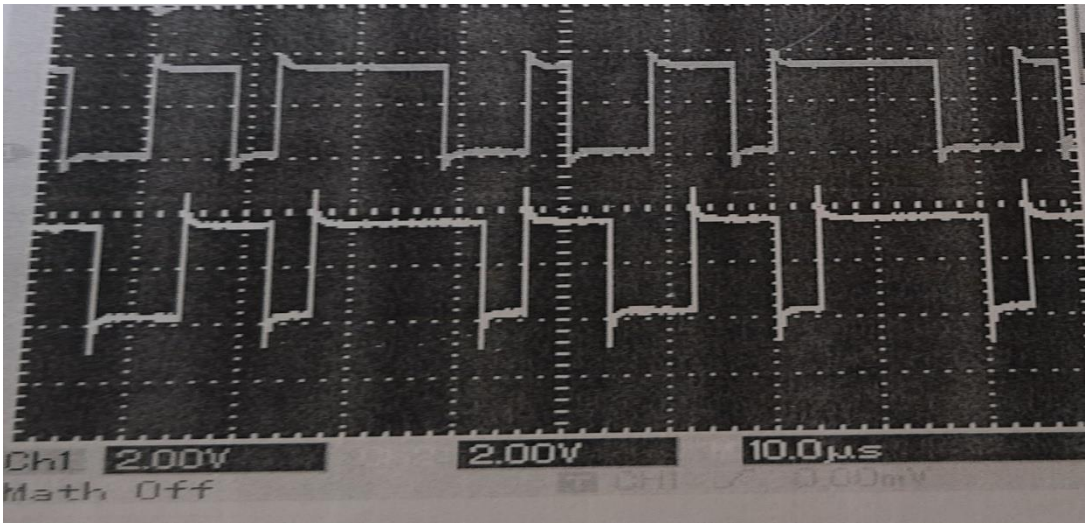
a) Make the connections as shown in the figure
b) Connect the power supply to the kit and switch it on.
c) Set the data pattern as shown in the block diagram using SW1
d) Observe CRC encoded signal at DATA OUT post of CRC generator
e) Introduce 2 bit manual error using SW2 and observe the output
f) CRC decoded and corrected signal can be observed at OUT post of CRC decoder. Calculated CRC at receiver end is displayed on LED B1 to B4

EXPECTED RESULTS/WAVEFORMS

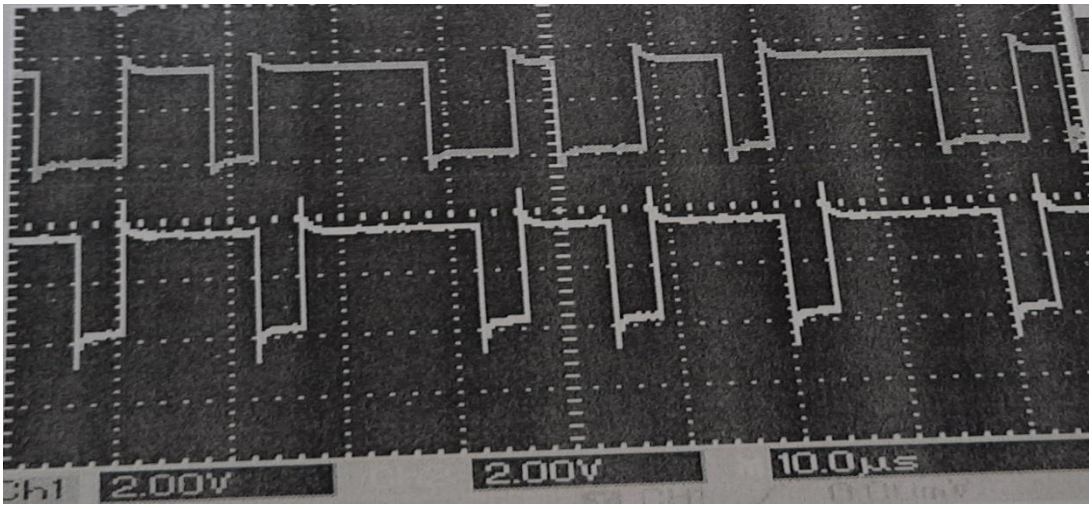
a) CRC generator and error adder output without any error



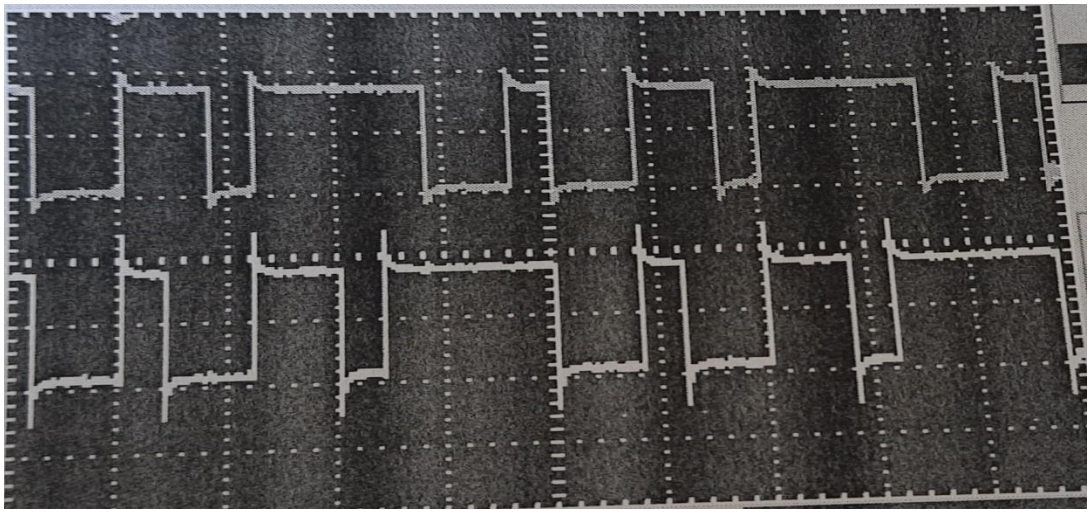
b) CRC generator output with one bit error added



c) CRC generator output with two bit error added



d) CRC decoded data output without any error



INFERENCE:

EXPERIMENT-7
PERFORMANCE ANALYSIS OF FIBER OPTIC LINK

OBJECTIVE:

The objective of the experiment is to study the performance of fiber optic analog and digital links

THEORY:

Fiber optic links are used for transmission of analog and digital signals. A fiber optic link consists mainly of three elements, namely, transmitter, an optical link and a receiver. The transmitter converts the input electrical signal into optical form which contains the same information. Fiber optic link is a medium which carries the optical energy to the receiver. At the receiver, light is converted back into electrical form with same pattern as originally fed to the transmitter.

EQUIPMENTS:

FCL-03
FG-02 with power cable
1 meter fiber cable
Patch chords
Power supply
20 MHz dual channel oscilloscope

BLOCK DIAGRAM:

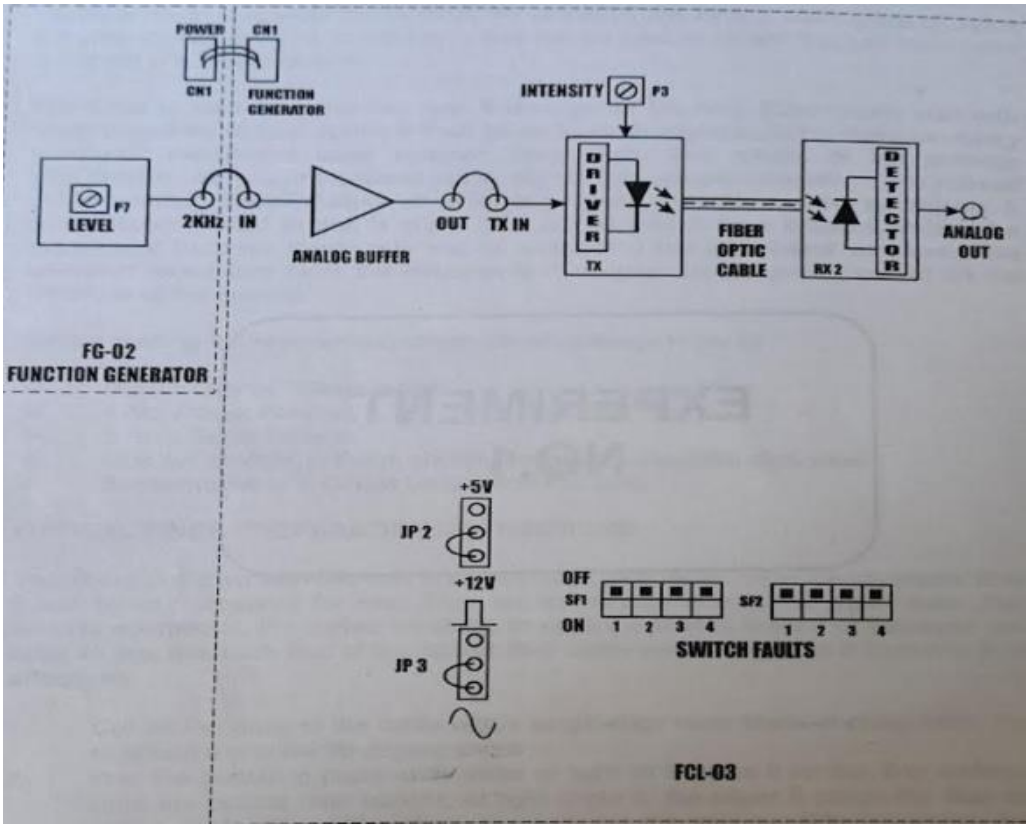


Fig1: Block Diagram of Fiber optic analog link

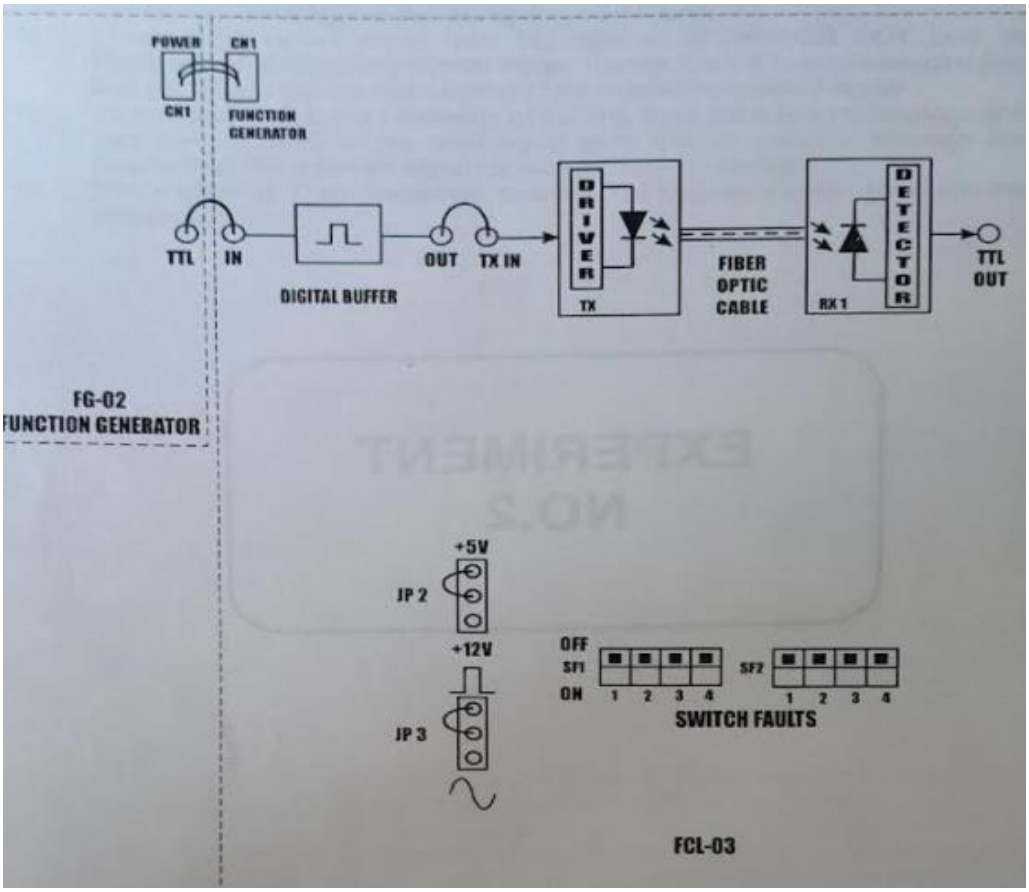


Fig2: Block Diagram of Fiber optic digital link

PROCEDURE:

A. To find the transmission loss

a) Make connections as shown in fig1 for analog link and fig2 for digital link

b) Connect the power supply cables with proper polarity to FCL-03 kit

c) Connect function generator FG-02 to FCL-03 using power cable

d) Keep the jumpers JP2 and JP3 FCL-03 as shown in fig1 for analog link and fig2 for digital link respectively

e) Connect the 2KHz, $2V_{pp}$ signal from FG-02 as a constant signal to the IN post of analog buffer on FCL-03 for analog link

f) Connect TTL signal from FG-02 as a constant signal to the IN on FCL-03 f for digital link

g) Insert the fiber by unscrewing the cap of LED SHF756V at transmitter end SFH 250V at the receiver end

h) Observe the output at Analog OUT/TTL OUT for analog and digital links respectively

i) Note down the output Vpp value and observe the signal transmission loss

j) Connect a fiber of different length and observe the signal loss due to variation of length

B. To find the bending loss

a) Bend the optical fiber connected at certain diameters and note down the diameters

b) Note down the output voltages for different bend diameters
c) Observe the signal loss due to bending of the fiber

TABULAR COLUMN:

A) Transmission loss:

Input voltage Vpp =

Analog/DIgital	Fiber length(m)	V_{pp}(volts)
Analog link		
Digital link		

B) Bending loss:

Input voltage Vpp =

Analog/DIgital	Fiber bend diameter	V_{pp}(volts)
Analog link		
Digital link		

RESULTS/INFERENCE:

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EXPERIMENT NO: 8

NAME: Study Of Transmission And Reception Of Band Limited Pulse Train In Baseband Digital Transmission System

OBJECTIVE

To study the effect of band limitation in the baseband digital transmission system

EQUIPMENTS

- DCL-BASE BAND kit
- Connecting Chords
- Power supply
- 20MHz Dual Trace Oscilloscope

NOTE: Keep The Switch Faults In Off Position**.**

THEORY

This section develops a design for baseband digital systems when the transmission channels impose bandwidth limitation. By this we mean that the available transmission bandwidth is not large compared to the desired signaling rate and, consequently, rectangular signaling pulses would be severely distorted. Instead, we must use band-limited pulses specially shaped to avoid Inter Symbol Interference. Base-band systems therefore require the use of a low-pass channel with a bandwidth large enough to accommodate the essential frequency content of data stream and also to minimize error probabilities.

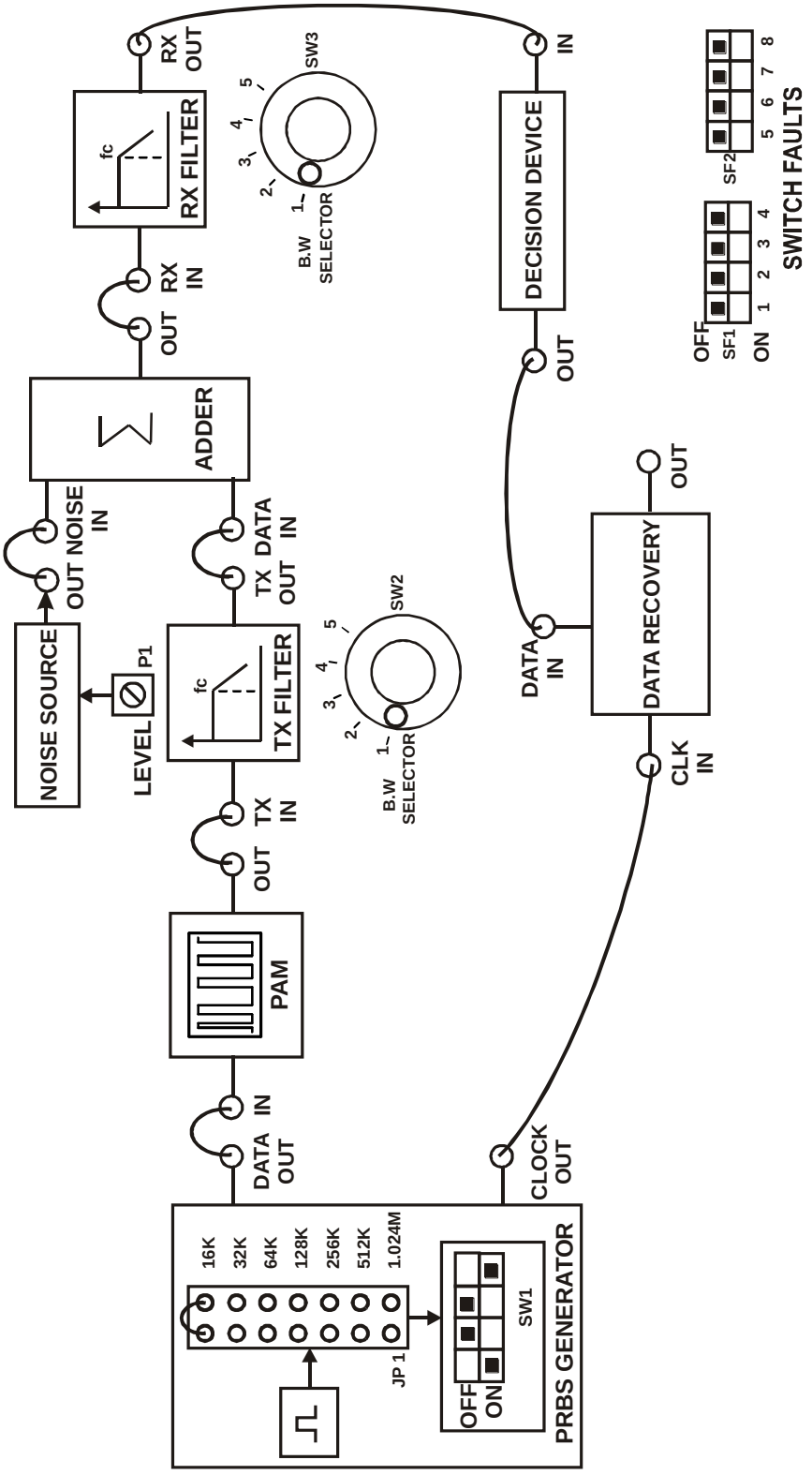

FIG. 3.1 BLOCK DIAGRAM FOR STUDY OF TRANSMISSION AND RECEPTION OF BAND LIMITED PULSE TRAIN IN BASE BAND DIGITAL TRANSMISSION SYSTEM

PROCEDURE

1. Refer to the block diagram (Fig.3.1) and carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-BASE BAND** and switch it ON.
3. Keep the switch of the PRBS generator **SW1** as shown in the Fig.3.1 for the generation of the PRBS pattern.
4. Select the **PRBS** clock frequency to **16 KHz** using jumper **JP1**.
5. Connect the PRBS **DATA OUT** post to the **DATA IN** post of the **PAM.**
6. Keep the position of the rotary switch **SW2** of the TX channel to **1**.
7. Connect the PAM **OUT** post to the **TX IN** of the TX Filter and connect the data from the **TX OUT** post to the **DATA IN** post of the Adder.
8. Connect **TX OUT** post of TX Filter to **DATA IN** post of the Adder.
9. Connect the noise from the **NOISE OUT** post of the noise source to the **NOISE IN** post of the Adder.
10. Connect the **OUT** post of the Adder to the **RX IN** of the RX filter.
11. Keep the position of the rotary switch **SW3** of the RX filter to **1**.
12. Connect the data from the **RX OUT** to the **IN** post of the Decision device. Note that green LED will glow.
13. Connect the **OUT** post of the Decision device to the **DATA IN** post of the Regenerator.
14. Connect the **CLK OUT** from the PRBS generator to the **CLK IN** post of the Regenerator.
15. Note that the bandwidth of both the TX filter and RX filter should match.
16. Observe the output at the **OUT** post of the regenerator section on the oscilloscope.
17. Keeping the clock frequency of the PRBS data to 16 KHz change the bandwidth of the TX Filter and the RX Filter to position no.**2,** later to position **3** and position **4**.
18. Observe the filter response of both the TX and RX filters at their respective out posts at increased bandwidth.
19. Similarly transmit the PRBS data keeping the clock frequency to 256 KHz, set the bandwidth to position **5**, later to position **4** and position **3**.
20. Observe the filter response of both the TX and RX filter at their respective out posts at decreased bandwidth.
21. Observe the effect of the bandwidth on the output data at the **OUT** post of the Regenerator.

OBSERVATION

Observe the band limited pulses at the **TX OUT** post and **RX OUT** post on the oscilloscope. For different frequencies of PRBS data pattern set the bandwidth as follows:

Clock frequency	Bandwidth position
1. 16 KHz	Position 1
2. 32 KHz	Position 2
3. 64 KHz	Position 3

4. 128 KHz Position 4

5. 256 KHz Position 5

Mismatch the bandwidth settings of TX filter and RX filter and observe the variations in the output.

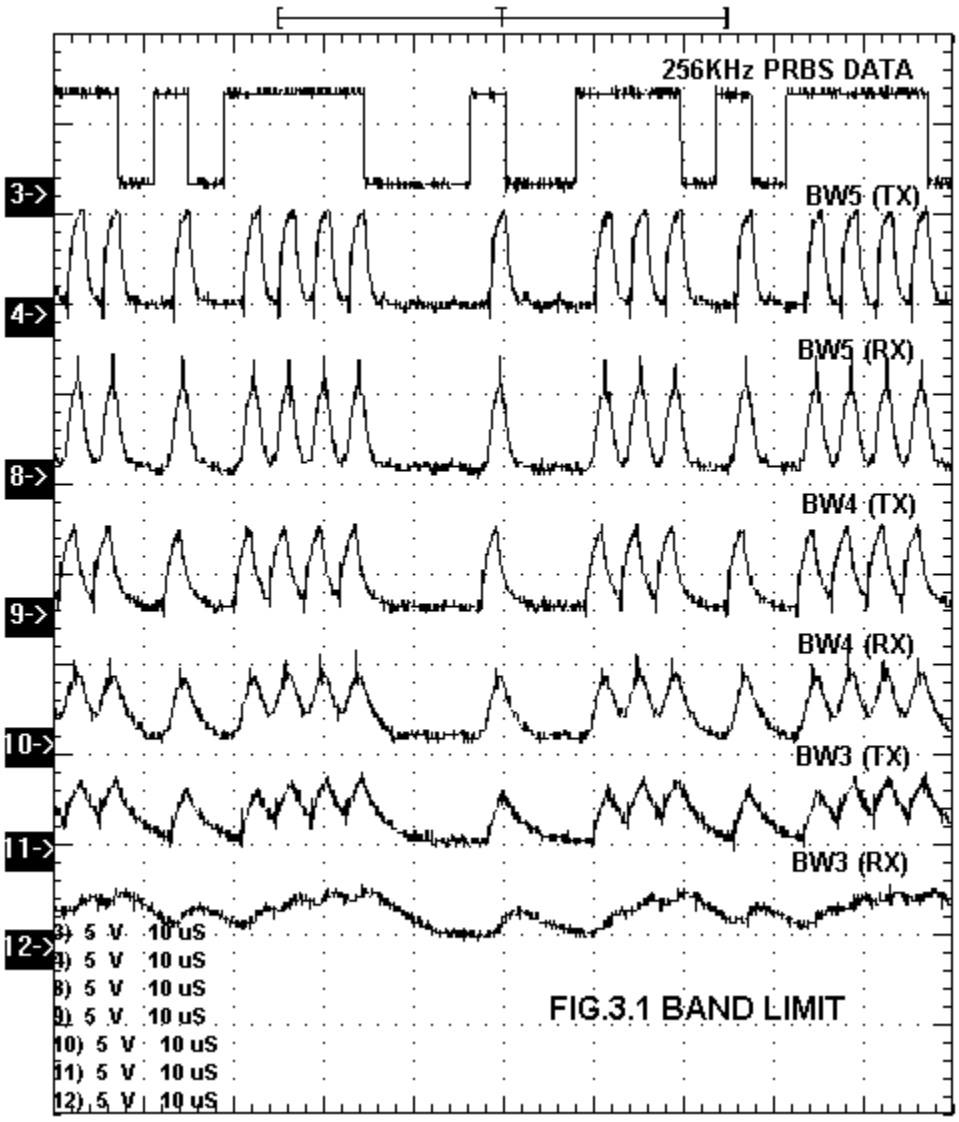

FIG.3.1 BAND LIMIT

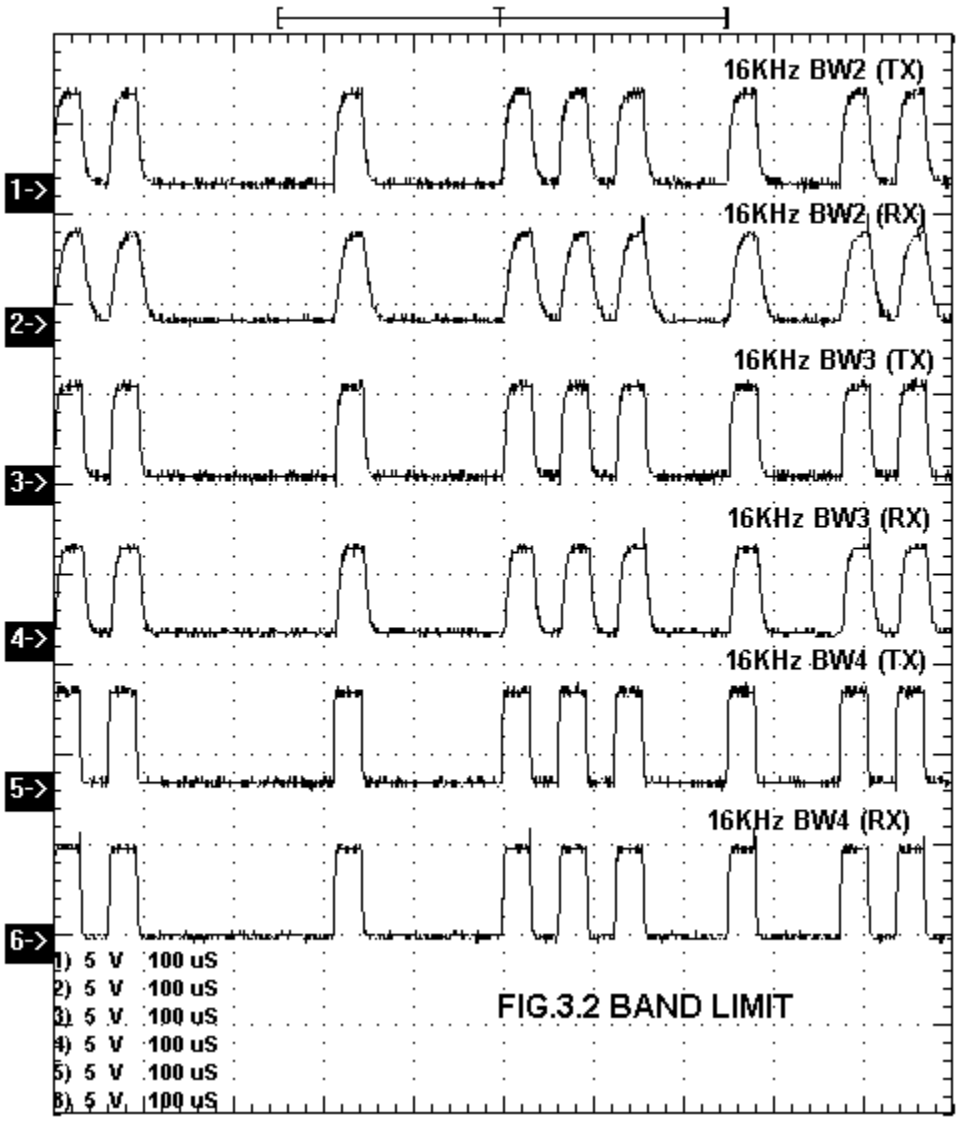

FIG.3.2 BAND LIMIT

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EXPERIMENT NO: 9

NAME: Measurement Of Bit Error Rate Using Binary Data

OBJECTIVE

To measure bit error rate.

EQUIPMENTS

- DCL-BASE BAND kit
- Connecting Chords
- Power supply
- 20MHz Dual Trace Oscilloscope

NOTE: Keep The Switch Faults In Off Position.

THEORY

In telecommunication transmission, the bit error rate (BER) is a ratio of bits that have errors relative to the total number of bits that have errors relative to the total number of bits received in a transmission. The BER is an indication of how often a packet or other data unit has to be retransmitted because of an error. Too high a BER may indicate that a slower data rate would actually improve overall transmission time for a given amount of transmitted data since the BER might be reduced, lowering the number of packets that had to be resent.

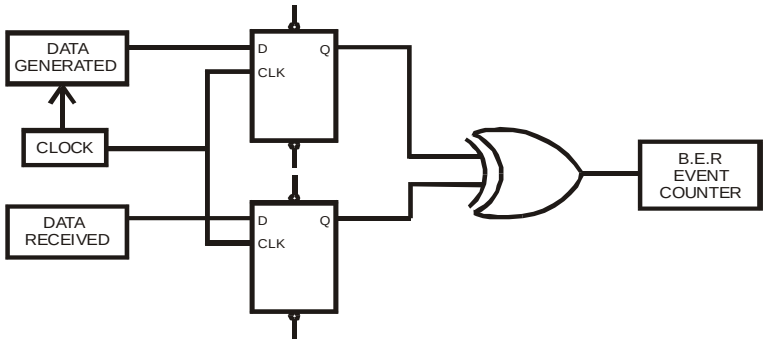
Measuring Bit Error Rate

A BERT (Bit Error Rate Tester) is a procedure or device that measures the BER for a given transmission. The BER, or quality of the digital link, is calculated from the number of bits received in error divided by the number of bits transmitted.

BER = (Bits in error) / (Total bits transmitted)

Using a bench test setup, this is easily measured by means of a comparator in which the transmitted bits are matched in an XOR gate with the received bits.

Fig shows the schematic of the device used for the following measurements.



BIT ERROR RATE TESTER (B.E.R.T.)

If the bits are alike at the XOR gate inputs when clocked in from the D flip-flop, the output is low. If they are different, the XOR output goes high, causing an event count.

A random character generator and white noise source should be used for these measurements.

The number of bit errors is dependent upon the amount of noise entering the system.

The white noise, or background noise, has an average or RMS value that is exceeded periodically by peaks that rise many times that level. This peak exists only for a short period of time. When the peak equals or exceeds the signal level, that is noise energy = bit energy, there is a 50/50 chance of error. The peak time periods can be calculated statistically from the error function.

PROCEDURE

1. Refer to the block diagram (Fig.5.1) and carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-BASE BAND** and switch it on.
3. Keep the position of the switch **SW1** of the **PRBS GENERATOR** as shown in the Fig.5.1 for the generation of the PRBS pattern.
4. Select the **PRBS** clock frequency to **16 KHz** using jumper **JP1**.
5. Connect the PRBS **DATA OUT** post to the **IN** post of **ERROR BIT ADDER.**
6. Observe the noise pulses at **E.P.** by varying the pot **P2.**
7. Connect the **OUT** post of the Adder to the **RX DATA** post of the BER meter.
8. Keep the pot **P2** of the **ERROR BIT ADDER** at minimum position.
9. Connect the **CLK OUT** post to the **CLK** post of the BER meter.
10. Connect the **DATA OUT** post of **PRBS GENERATOR** to **DATA IN** post of the **BER METER**.
11. Press the **RST** switch to reset the counter to zero.
12. Press the **START** switch to start the counting.
13. Observe the error count on the display after 10 seconds upon pressing **START** switch.
14. Observe that when the pot is kept at minimum position the bit error count is very low. The error count will increase linearly as we increase the pot to the maximum (clockwise) position.

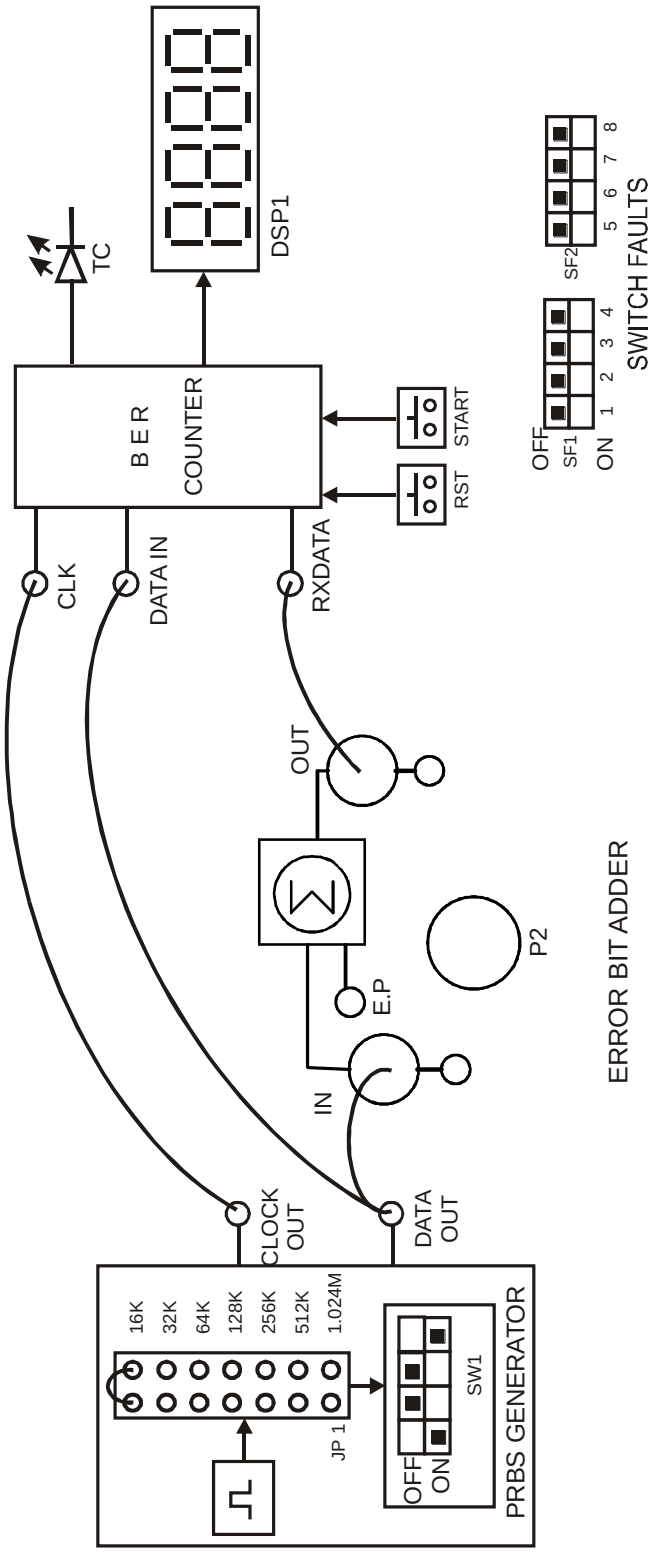


FIG. 5.1 BLOCK DIAGRAM FOR MEASUREMENT OF BIT ERROR RATE USING BINARY DATA

BER MEASUREMENT

The noisy data from the OUT post of the Adder is connected to the RX DATA IN of the BER meter As BER is the ratio of error bits (E_b) to total bits transmitted (T_b) in a period time *t* sec i.e.

$$BER = E_b/T_b$$

E.g. If PRBS data is transmitted at 32Kbits per sec for a period of 10 sec.

The total bits transmitted in 10 sec (T_b) = 320 bits.

The TTL out data with noise is fed to BER counter, which compares the two data input at each clock input.

The counter gives the 10 bit binary from error count (Eb) which is converted into decimal form and displayed.

E. g.

(0000001010 = 10 (decimal form))

BER RATIO then becomes:

$BER = 10/320*10E^3$

$= 0.00003125$

i.e. the channel Bit Error Rate ratio is $3.1*10E^{-5}$ (3/100000) or in other words we can say that out of 100000 bits transmitted through the channel, the channel gives 3 bits in error.