FLOW CHART FOR SCHEMATIC:-

Schematic entry

↓

Symbol creation

↓

Test the Schematic entry

↓

Launch ADE-L

↓

Specify Analysis

↓

Specify I/P & O/P to be plotted

↓

Save the state

↓

Run the simulation

SHORT CUTS:-

pick components - I
wiring - w
fit screen - f
hook of components - q
copy - c
move - m
undo - u
label - l

DEPARTMENT OF ELECTRONICS & COMMUNICATIONS Engg., LABORATORY RECORD

Experiment No. 01 Date .....

TITLE : STEPS FOR ANALOG CIRCUIT DESIGN IN CADENCE

SCHEMATIC :-

1) Create a new folder
2) Open terminal inside that folder and execute the following command to open virtuoso
   - ☆ csh
   - ☆ source /home/install/cshrc
   - ☆ virtuoso &
3) Create a new library and link the tech
   tech ⇒ gpdk180
4) create a new cell from cell view option and name the cell.
5) New schematic will appears, place the components using component tab or (I)
6) Connect the wire using (w) and i/o pins using (p), change the property of component using (q), rotate it using (r), undo using (u)
7) Create a symbol using these steps
   - ☆ create
   - ☆ cell view
   - ☆ symbol
   - ☆ apply

8) Check and save before creating a symbol
9) Create another cell view for schematic and use the symbol created and build the circuit
10) press (b) for bit wren, move the components if req'd wing (m), label the wires wing (l), and simulate the design

DC ANALYSIS :-

I/P for the ckt should be DC voltage

→ launch
→ ADE - L
→ Analysis
→ DC
→ Save DC point
→ Sweep variable
→ Component parameter
→ Select Vin
    # "DC voltage"
    # OK
→ Set sweep range
    # 0 - 1.2V ← for inverter
→ sweep type auto

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Experiment No..... Date .....

TITLE : .....

AC ANALYSIS;-

I/P for the ckt should be sine signal and a capacitor b/w o/p and gnd

→ launch → freq range = 100 - 1GHz
→ ADE-L → 10 pts/decade
→ analysis
→ AC

In Vin prop
→ number of noise = 0
→ DC voltage (Vmid in DC analysis)
→ AC mag = 1V
→ Amplitude = 1V
→ frequency = 1kHz

→ Run simulation
→ plot
→ AC mag & phase
→ select
→ press ok

TRANSIENT ANALYSIS;-

→ tran
→ set stop time
→ in Vin properties set Amplitude = 1mV

LAYOUT Simulation flow:

Launch layout-XL from original schematic ckt

↓

Layout Entry

↓

DRC

↓

LVS

↓

Quantum QRC

↓

Create config file for the test ckt

↓

Open configured test schematic ckt

↓

Launch ADE-L

↓

Load the state

↓

RUN

SHORTCUTS:-

Show layers = f + shift

fit screen = f

edit prop = q

draw path = p

to stretch = s

via/contact = o

move = m

undo = u

ruler = k

remove ruler = shift + k

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Experiment No..... Date .....

TITLE : .....

LAYOUT:-

1) Open schematic of symbol
2) Launch → Layout XL
3) create new layout and set it to auto
4) once the blank layout opens, search for "generate all from sources" at bottom left corner, select default settings
5) press "shift + f" to see all layers
6) press "P" for path and connect all to dkt, "S" for stretching the path. "O" for placing contact btw 2 layers
   → via definition (select appropriate as/req^{t}).
7) for body terminal to be visible, go to prop of trans^{r} and select body type as integrated
8) for connecting Vdd & gnd to horizontal rail, rather than single line,

→ select pin
→ right click
→ pin placements
→ attributes
→ edge type
→ top as Vdd & bottom as gnd
→ horizontal rail
→ apply.

TO CHECK DRC :-

1) click AURA (top)
2) tech
3) browse
4) go to home → install → boundary → analog → 180nm → aura_tech_lib.
5) click on AURA again
6) create a working dir (name it as DRC)
7) give user name and user dir
8) chg tech to 180nm
9) if DRC is violated, chg the design using m and measure distance b/w 2 components using ruler (k) [shift+k to remove ruler]

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Experiment No..... Date .....

TITLE : .....

LAYOUT vs SCHEMATIC CHECK.

1) run lvs
2) choose dir
3) chg layout if lvs is ~~on~~ violated

EXTRACTION:-

1) AURA
2) run quantum QRC.
3) extraction → extraction type to RC.
4) ref node "gnd!"
5) Create a config file for test ckt after extracting
   → create new cell
   → type config
   → view schematic
   → use template
   → click open
   → OK
6) TREE view
7) click on instance (folder type).
8) AV - extracted (right click)
9) open
10) RUN simulation

N.I.E.

27/03/23