ECE 385

Spring 2023

Experiment #1

Introductory Experiment

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Purpose of Circuit

In this experiment, we build a 2:1 multiplexer, which is a very basic logic circuit but is a great way to become familiar with building logic circuits and simplifying logic to NAND form. Multiplexers allow us to select which signal input will be our signal output which is a fundamental part of digital systems. We will examine the static hazard that arises out of the gate switching delays and how to eliminate the hazard. Static hazard is important because even though it seems like a small error, it can have more profound effects on a high speed digital system.

Written Description of Circuit

Starting from a Karnaugh map (Figure 1), we find that the SOP form of a 2:1 multiplexer is B'C + BA where B is the "select" line. However, this expression uses AND, OR, and NOT logic which would require 3 different chips to implement(Figure 4). Luckily, we can achieve the logical equivalent using just 4 NAND gates, which allows us to use just one 2 input quad-NAND 7400 IC chip(Figure 5). However, there is still an issue that exists which is called static hazard. Static hazard is a result of gate delay but it can be eliminated by adding redundancy(Shown in green on Figure 2). Normally if we switch the select from 0 to 1, the output will very briefly switch to 0 even when it should be 1, to combat this, the redundancy makes sure that if both A and B are 1, the output signal will stay 1 even during the select line switch. I will show both NAND implementation logic diagrams in the Logic Diagram section, but the design using only NAND chips was actually built.

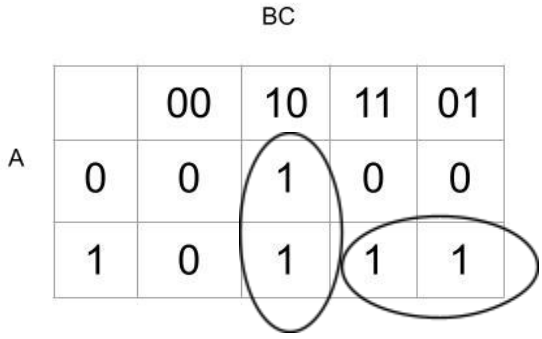

Figure 1: K-map for 2:1 MUX, Output Z

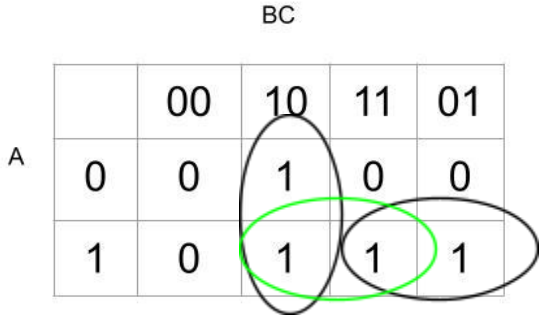

Figure 2: K-map for 2:1 MUX w/ redundancy, Output Z

High Level Block Diagram

The diagram below shows the 2:1 MUX which has 2 input lines(A and C), 1 output lines (D) and a select line (B) which picks which input the “connect” to the output.

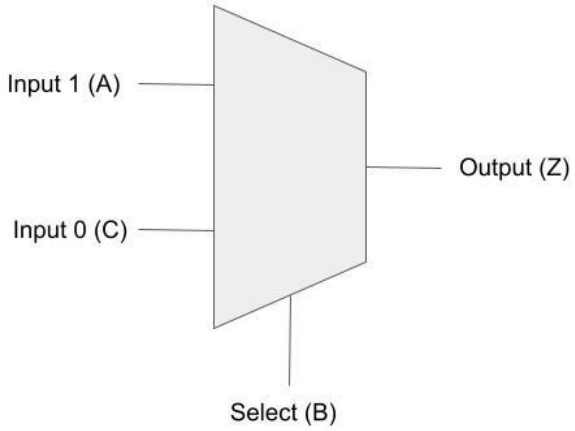

Figure 3: Diagram of 2:1 MUX

Truth Tables and Scope Plots

Below is the truth table and scope plots for the “naive” implementation of the MUX. The yellow line on the scope is the input B which is a 1 Mhz square wave. The output line which is purple shows the static hazard.

A	B	C	**Z**
0	0	0	**0**
0	0	1	**1**
0	1	0	**0**
0	1	1	**0**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

Figure 4: Truth Table for “naive” implementation of MUX

Figure 5: Oscilloscope plot for "naive" implementation

Below is the truth table and scope plots for the redundant implementation of the MUX. The output line now has no static hazard, but there is still some noise.

A	B	C	**Z**
0	0	0	**0**
0	0	1	**1**
0	1	0	**0**
0	1	1	**0**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

Figure 6: Truth Table for redundant implementation of MUX

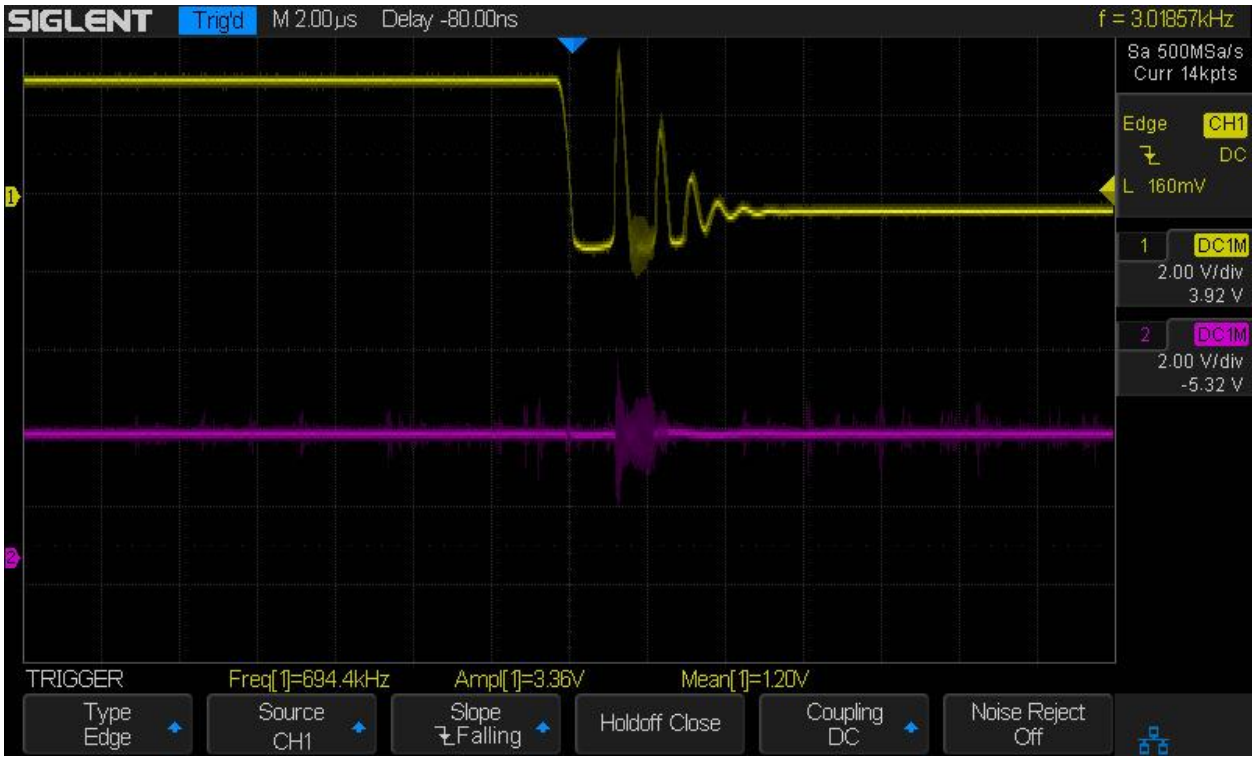

Figure 7: Oscilloscope plot for redundant implementation

Logic Diagrams

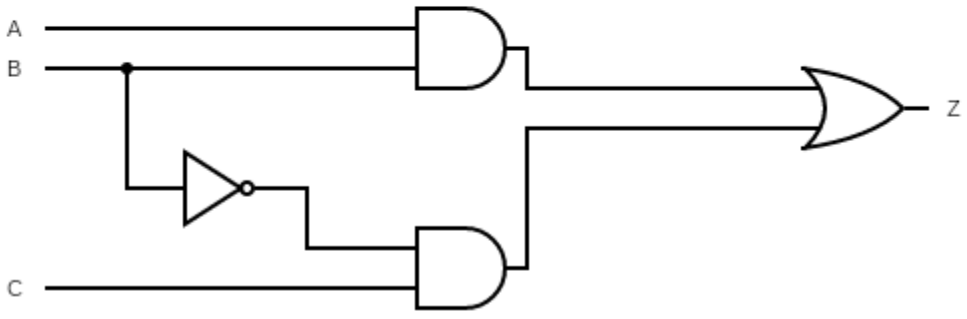

Figure 8: 2:1 MUX implementation with AND, OR, NOT

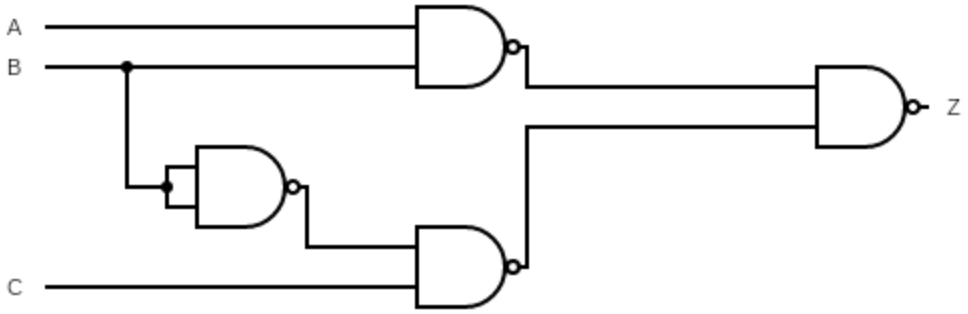

Figure 9: 2:1 MUX implementation with NAND

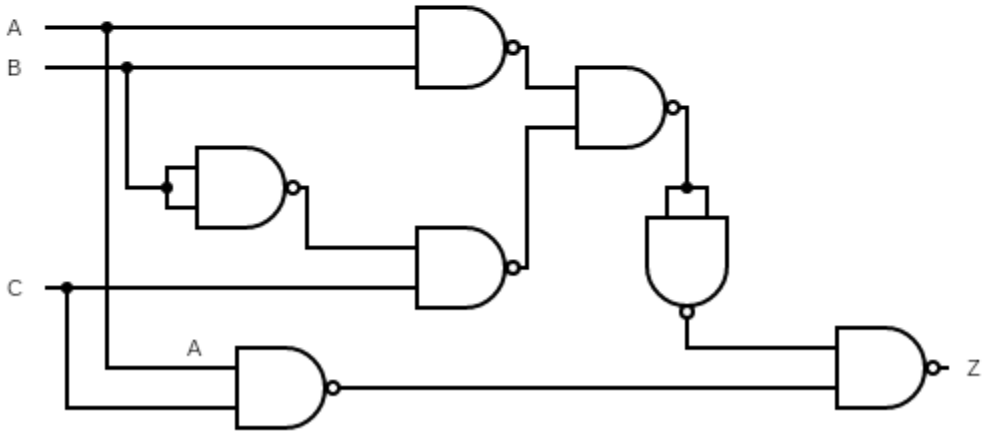

Figure 10: 2:1 MUX NAND implementation with redundancy

Component Layout

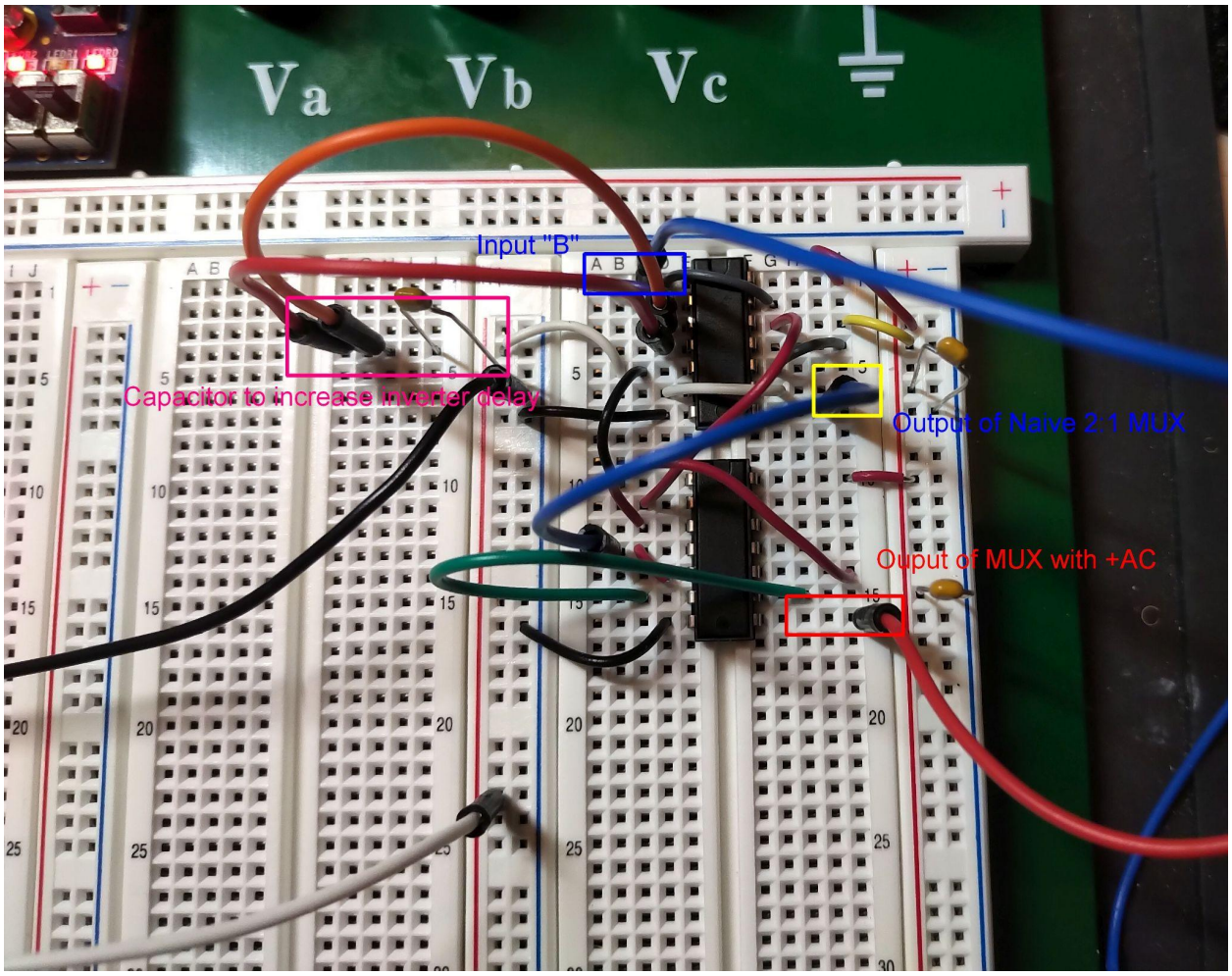

Figure 11: Component layout for MUX with redundancy

Pre-Lab Questions

1) Not all groups observe a static hazard because the static hazard is a product of gate delay. However, these gates have a minimum delay of 0 according to the General Guide(GG.25) so the delay may be too small to notice. In order to make a hazard appear, we add more inverters because this will add more delay.

General Guide Questions

GG.6) We measure the output of the last inverter so we can see the part of the circuit with the most noise. Noise arises as a result of the ICs so the more we put between our input and output measurements, the more noise we will see.

Larger noise immunity is better for the same reason that static hazard is bad, low noise immunity makes digital circuits vulnerable to errors and missteps so it is best to be more protected from noise to ensure proper functioning of a circuit.

Based on the graph and the definition of noise immunity, we can calculate that noise immunity is 1.15-0.7=0.45 V for logic 0 and 2-1.35=0.65 V for logic 0 which means the noise immunity for the gate overall is the lower of the two, 0.45V.

GG.31) If LEDs share a resistor, the current gets divided by each LED connected meaning each LED may not get enough current to light up.

Lab Questions

The truth tables for both implementations are identical(Figures 4 and 6).

The oscilloscope shows that with the “naive” application there is noise as well as a static hazard. When we add the redundancy we still see the noise when the B signal switches, but there is no hazard.

We are more likely to see static hazard on the falling edge because that is when Z may output 1 NAND 1 (0) briefly, if there is significant gate delay on the NAND gate which inverts B.

Post-Lab Questions

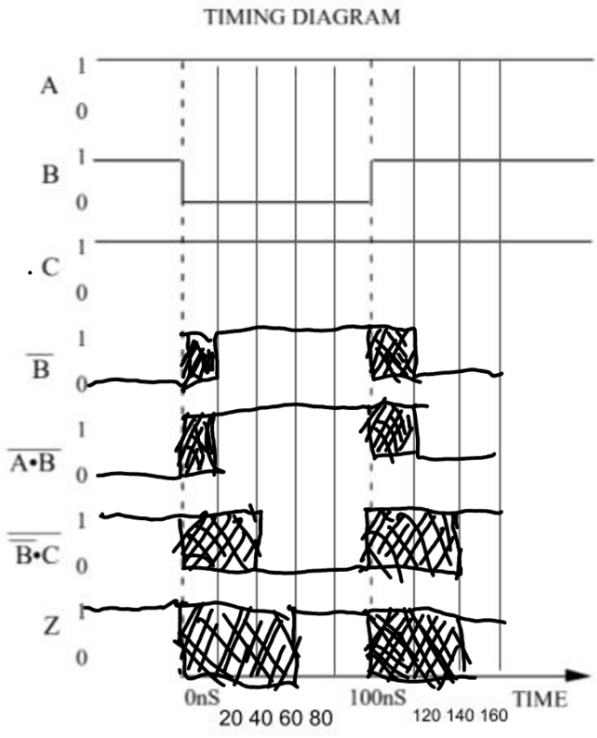

Figure 12: Timing Diagram

The timing diagram shows that there is a 60 ns delay for the output Z on both the rising and falling edge of the B signal because the output always depends on 3 gates with 20 ns max delay each. There are glitches that occur when B rises and falls because of the delay. We are more likely to see a glitch on the falling edge of B because the falling edge is when the output gate static hazard occurs because the input briefly becomes 11.

The debouncer circuit in GG fig 17 works by stabilizing the output even if the input changes briefly. The contact is made with point A, but then disconnects for a brief period of time, the output will remain as if contact was still made with point A. For example, if the switch is flipped towards A, D goes low, Q goes high, which makes QN low, so Q will stay high even if the bouncing makes A go high briefly.

Conclusions

In this lab we examined the consequences of delay, specifically static hazard. We examined how to eliminate static hazard by adding redundancies to “double cover” some of the minterms in the K map. By doing this we make sure that our system will function correctly because in the world of digital circuits, a small hazard can have larger impacts. Another thing we learned was the use of decoupling capacitors to allow smooth functioning of the ICs.