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Design and Implementation of a Stable Platform Digital Controller Based on DSP

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***Abstract*— The principle, configuration, and the special features of a stable platform digital controller are presented in this paper. The main goal of this paper is replacing an analog controller with its awaiting digital one. This has been done using TMS320LF2402 digital signal processor which offers the enhanced TMS320 DSP architectural design of the C2xx core CPU for low-cost, low-power, and high-performance processing capabilities. The experimental results show that the digital controller is identical to the analog one and can be a suitable replacement for the analog controller.**

I. INTRODUCTION

The advances made in microelectronics and microprocessors have infused new life into the growth of digital control systems and has made significant amount of processing available even at relatively high switching frequencies, so the realization of sophisticated and inexpensive digital control system has become feasible. It is expected that digital controllers will increasingly replace currently predominant analog controllers in many of applications. Potential advantages of digital controller implementation include much more reliability, improved flexibility, no drift, reduced design time, programmability, elimination of discrete tuning components, more compact, easier system integration, low-power-level signals, light weight, performing complex computations at high speed, multiplexing, extreme versatility , less effect due to noise and disturbance and possibility to include various performance enhancements [1]-[5] .

The above mentioned advantages make the digital control a viable option to meet the requirement. So, a stable platform digital controller is designed and implemented in this paper.

Sampling frequency selection and conversion of analog system to digital is described in section 2. Hardware configuration of the digital controller is described in section 3, while its software configuration is investigated in section 4. Next, the experimental results are shown in section 5. Finally, conclusions are drawn in section 6.

II. SAMPLING FREQUENCY SELECTION AND CONVERSION OF ANALOG SYSTEM TO DIGITAL

Block diagram of analog controller is shown in Fig. 1. The first thing to do is conversion of the analog system to digital. This is done using Z transform. Z transform is the counterpart of the Laplace transform for continuous-time signals and a highly valuable approach for formulating, analyzing and solving problems in the discrete domain. Similar to advantages of the Laplace transform in the continuous time domain, the major benefit is in the reduction of the complexity of equations to relatively simple algebraic equations [5], [6].

There are different methods for discretizing continuous-time systems like zero order hold, Triangle approximation, Impulse-invariant discretization and bilinear (Tustin) approximation.

The method used here is bilinear approximation or Tustin, which uses the approximation shown in Equation (1):

$$Z = e^{ST_S} = \frac{1 + ST_S/2}{1 - ST_S/2} \tag{1}$$

This approximation is a simple way for determination of a discrete-time representation of a continuous-time control system and is sufficiently precise, if a sampling interval is chosen properly, so the sampling rate plays a key role and should be determined prior to the synthesis of controller [7].

The sampling rate directly affects the achievable performance and the robustness properties of digital control system. Higher sampling rate is preferable for higher system bandwidth requirement; however, an increase of sampling rate may demand an increase in word length and computation speed of the digital controller. Lower sampling rate to achieve the given design specifications is always an engineering design goal [5]. To determine the sampling frequency, pole and zero frequencies of all transfer functions are calculated and the biggest frequency among them is selected. This frequency here is 765 HZ. The sampling frequency should be 1530 to avoid aliasing. Due to our hardware and its processing capability the sampling frequency is selected to be 8 KHZ.

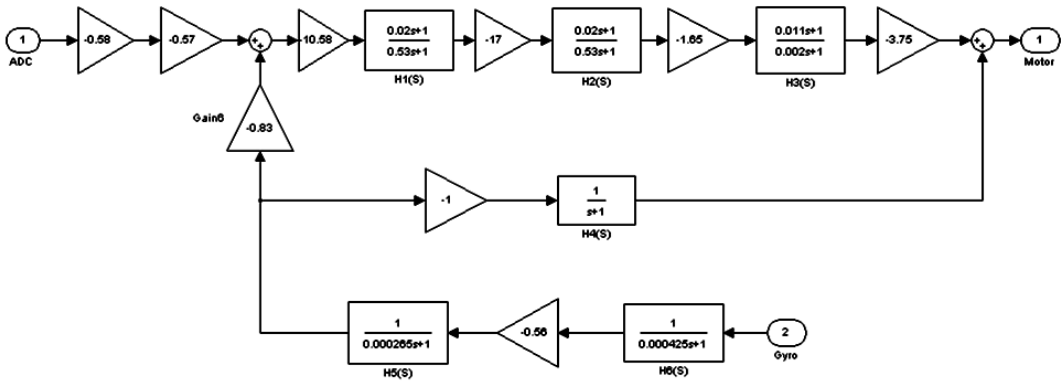

Fig. 1. Block diagram of Analog Controller

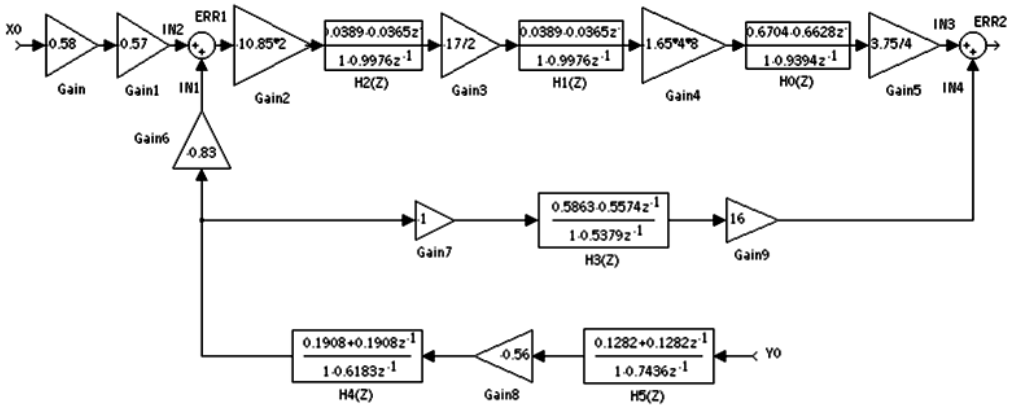

Fig. 2. Block diagram of digital Controller

Using the sampling frequency of 8KHZ and bilinear approximation method, the analog system is converted to digital. The digital system is shown in Fig. 2 .

III. HARDWARE CONFIGURATION OF DIGITAL CONTROLLER

The schematic diagram of the digital controller system is shown in Fig. 3. This system consists of an input section, DSP, PWM filter and power supply section. Also, the printed circuit board of digital controller is shown in Fig. 4.

The input section provides two functions; the first one is the necessary level shift (the input signal is in the range of ±5 while the input range of ADC is 0-3.3) and the other one is protection of ADC input.

There are many consideration factors in the selection of a microprocessor in the design of a digital control system [5]. After a through consideration of performance, price, simplicity in hardware design, and software support, a single-chip DSP (TMS320LF2402) from Texas Instruments is selected to realize the digital stable platform controller. The TMS320LF2402 has many good features , which makes it a good candidate to realize digital control of stable platform, such as multiple independent programmable timers, 50 n-sec instruction cycle, 16 bit parallel multiplier, 2 channels of multiplexed 10-bit A/D converters, and on-chip RAM and EEPROM, etc [8].

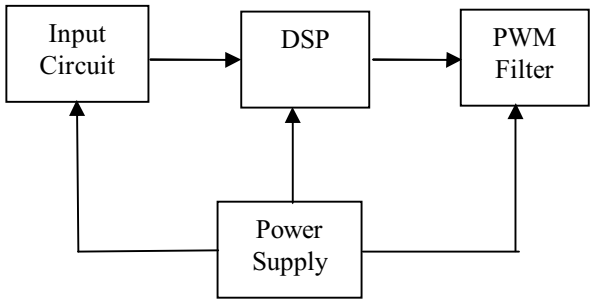

Fig. 3. Schematic diagram of digital controller

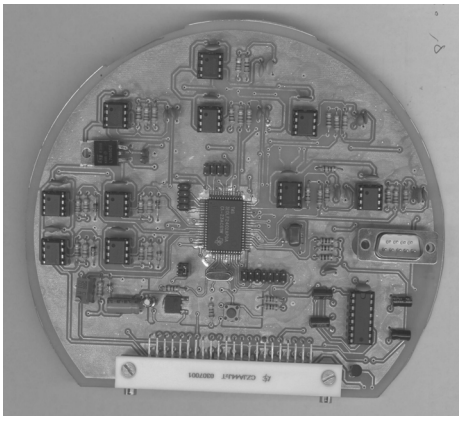

Fig. 4. Printed circuit board of digital controller

Another part of hardware is PWM filter. It should be noted that this digital system should replace an analog system, so the output should be analog. To do this, PWM is used. In fact, PWM is used as a digital to analog converter which its pulse width changes with digital value. This causes a change in the DC value of the output. To convert the PWM pulse to a DC value a PWM filter is used. This filter should provide three conditions: (1) passing 50 HZ frequency without phase difference (2) attenuation of 40 KHZ signal (the attenuation value is in the range of -40db to -50db) (3) conversion of the signal in the range of 0-3.3 to ±5 (because the output of analog board was in this range). The mentioned filter is implemented using an operational amplifier. Bode diagram of this filter is shown in Fig. 5. As can be seen the designed filter satisfies the conditions mentioned above.

The last part is power supply section which provides the necessary supply voltage for different parts.

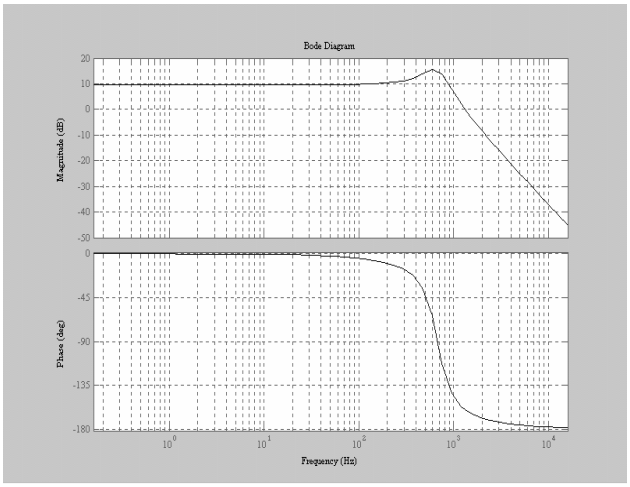

Fig. 5. Bode diagram of PWM filter

IV. SOFTWARE CONFIGURATION OF DIGITAL CONTROLLER

The software of digital control system relates to DSP program and is written using assembly language. The flow chart of the software is shown in Fig. 6.

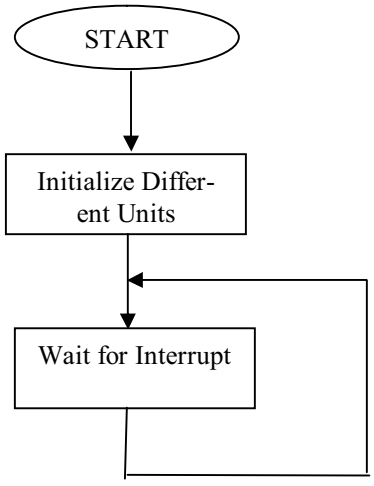

Fig. 6. Flowchart of the software

As can be seen there are two parts: the first part initializes different units of DSP like system registers, EVA registers and the ADC registers. The second part is the interrupt service routine that is the main part of software. The flow chart of the interrupt service routine is shown in Fig. 7. This subroutine is the subroutine of timer 2 which is repeated every 125 us. As mentioned before, this period is the sampling period.

The interrupt service routine provides three functions: (1) reading the analog data and converting it to digital, this is done using a subroutine located in interrupt service routine which reads the data through ADC of DSP and converts these data to digital and saves them. (2) implementing the digital control system shown in Fig. 2 .The method used to implement filters is canonic direct form which is illustrated in [7]. (3) writing the digital output value to PWM associated register(CMPR) which acts like digital to analog converter.

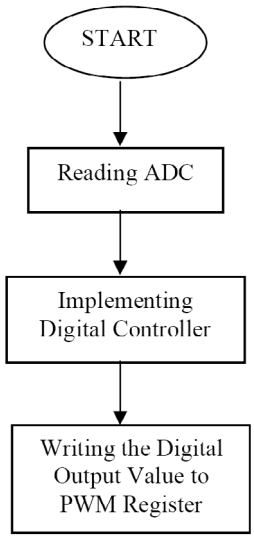

Fig. 7. Flowchart of the interrupt service routine

V. EXPERIMENTAL RESULTS

Experimental results obtained from the implemented system are discussed here. To verify the results, first the digital system shown in Fig. 2 is simulated using SIMULINK and the experimental results are compared with simulation results. This has been done for different cases, which two of them are shown in figures Fig. 8 to Fig. 11. Also, phase difference and gain of simulation and experimental results of these two cases are shown in Table I. Comparing the simulation and experimental results obtained from the implemented digital controller shows that the implemented system can be a suitable replacement for the analog controller.

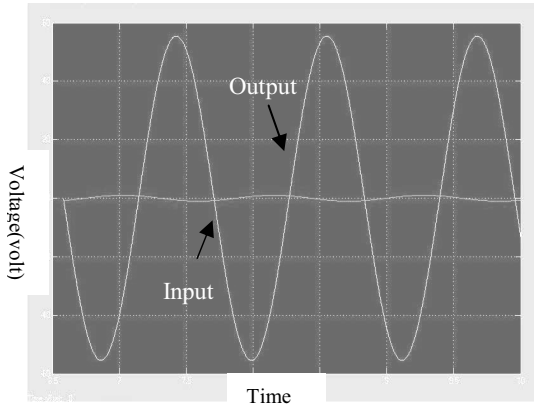

Fig. 8. Simulation results for the input case 1

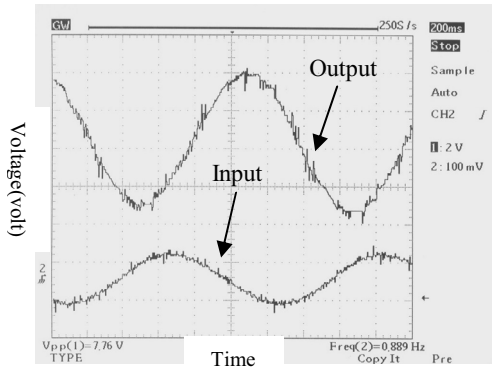

Fig. 9 Experimental results for the input case 1

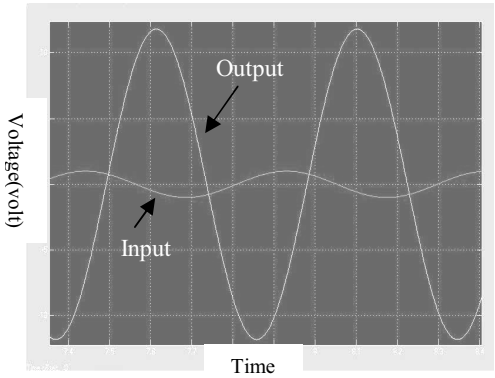

Fig. 10. Simulation results for the input case 2

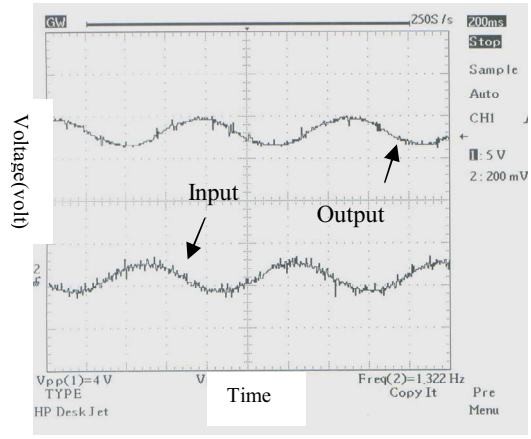

Fig. 11. Experimental results for the input case 2

TABLE I

PHASE DIFFERENCE AND GAIN FOR TWO DIFFERENT CASES

(IMPLEMENTATION AND SIMULATION)

	Phase difference	Gain
Case 1 (simulation)	128	55
Case1(implementation	120	60
Case 2(simulation)	132	27
Case2(implementation)	130	25

VI. CONCLUSION

Due to our sampling period which is 125 us, 5000 operations can be executed in this period (because the working frequency of DSP is 40 MIPS). Another thing that should be noted is that implementing a filter needs 10 instructions, so 500 filters can be implemented approximately. Implementing these filters using analog components needs 500 operational amplifiers and a lot of passive components. So implementing these filters using digital system lowers the power consumption and hardware redundancy drastically.

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