Interfacing with the DDR

ECE 153A/253, CMPSC 153A

September 26, 2016

This document is a tutorial on interfacing with the DDR2 memory on Nexys 4 DDR Board. For interfacing with the DDR2, the Memory Interface Generator (MIG) IP needs to be a part of the Vivado project. The two files (*mig.ucf and mig_b.prj*) that will be required to configure the MIG are attached. The first few steps of this tutorial are the same as the steps in the Hardware Handout.

1 Creating a Vivado 2016.2 Project with the MIG IP

1. Open Vivado, Click "Create new project" and Next. Name your project and choose the project location.
2. Select RTL project, click Next (through Add Sources) , click Next (through Add IP)
3. Add the constraints file "Nexys4_master_DDR.xdc" from the **/MIGFiles** directory. It contains additional configuration files:
   - mig.ucf
   - mig_b.prj

   The additional constraints file (mig.ucf) is used to specify the wiring of the DDR2 pins to the FPGA pins.
4. In the SEARCH bar, type: **xc7a100tcsg324-1** Click Next and Finish.
5. In the left menu called "Flow Navigator", click on "Create Block Design" and name your block design **system**. You can name your block design anything here. I use the name system throughout this document.
6. Click on "Add IP"

1.1 Creating a MicroBlaze Project

1. Begin to type "MicroBlaze", and select the "Microblaze" module to add to the design
2. Click on "Run Block Automation".
3. Choose **Local Memory**: 64KB, **Debug Module**: Debug & UART, and check "Interrupt Controller". Leave the other options unchanged.

1.2 Customizing a MicroBlaze Project

1. Double-click on the "Microblaze_0" block.
2. From **Predefined Configurations** select the "Typical" configuration and uncheck "Use Instruction and Data Caches". Leave the other options unchanged.
3. Click on the "clk_wiz_1" (Clocking Wizard) block and modify the settings as follows:
   (a) In "Clocking Options" tab under "Input Clock Information" in **Source** column select "Single ended clock capable pin" (Not differential). The clock source available on the Nexys 4 DDR Board is single-ended
   (b) In "Output Clocks" tab under "Enable Optional Inputs/Outputs" uncheck "reset"
   (c) The MIG IP needs an input clock of 200 MHz. Hence, the clocking wizard needs to be configured to output 2 clocks - one that drives Microblaze and related processor modules, and one that drives the MIG IP. Check "clk_out2"and set the Requested Output Freq for "clk_out2" to 200.000 MHz.
4. Click on "Run Connection Automation", and check **All Automation**. Click OK.
5. Rename the reset pin to btnCpuReset (to match the pin name specified in the .xdc file).

1.3 Adding the "AXI Timer" peripheral in Vivado

1. Open the block design
2. Click on the "Add IP" menu button
3. Begin to type "Timer" and select the AXI Timer Module
4. Click "Run Connection Automation", and check **All Automation**. Select "Auto" for **Clock connection (for unconnected nets)**. click OK
5. Connect "In0" port of the "Concat" module to the Microblaze "Debug Module interrupt port"
6. Connect "In1" port of the "Concat" module to the "AXI Timer interrupt port"

1.4 Create HDL resources

1. Right click on "system" in the "sources" window. Click "Create HDL Wrapper"
2. Right click on "system_i" (under "system_wrapper") in the "sources" window. Click "Generate Output Products" and "Generate"

2 Adding Peripherals

Add I/O peripherals (LEDs, buttons, seven-segment displays, etc.) required by your design following the same steps outlined in the Hardware Handout. Make sure that the names of the input and output pins match the pin names in the .xdc file.

3 Adding the MIG IP

1. Click on the "Add IP" menu button.
2. Begin to type "MIG" and select the Memory Interface Generator (MIG 7 Series).
3. Double-click on the MIG IP and launch the MIG Wizard.
4. Click Next. Under the MIG Output Options section, select "Verify Pin Changes and Update Design" and then click Next.

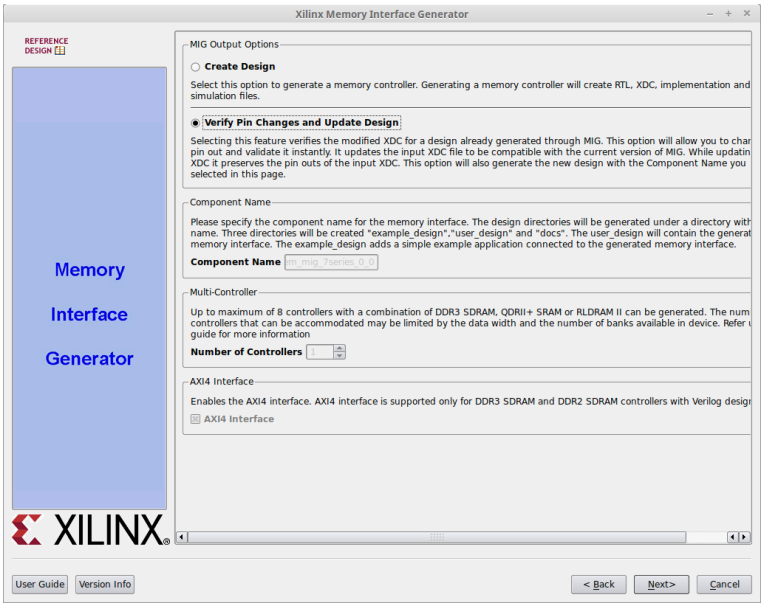

Figure 1: Verifying Pin Changes and Updating Design

5. Load the mig_b.prj and mig.ucf files included in the MIGFiles directory and click Next.
6. Click Validate, and then OK in the popup. You may ignore any warnings. Click Next.
7. Click Next, until you reach the final page. At one point you will need to accept a license agreement. Click Generate.
8. Again double-click on the MIG IP to launch the MIG Wizard.
9. Click Next. Make sure that the "Create Design" option is selected and the Number of Controllers is set to 1. Click Next.

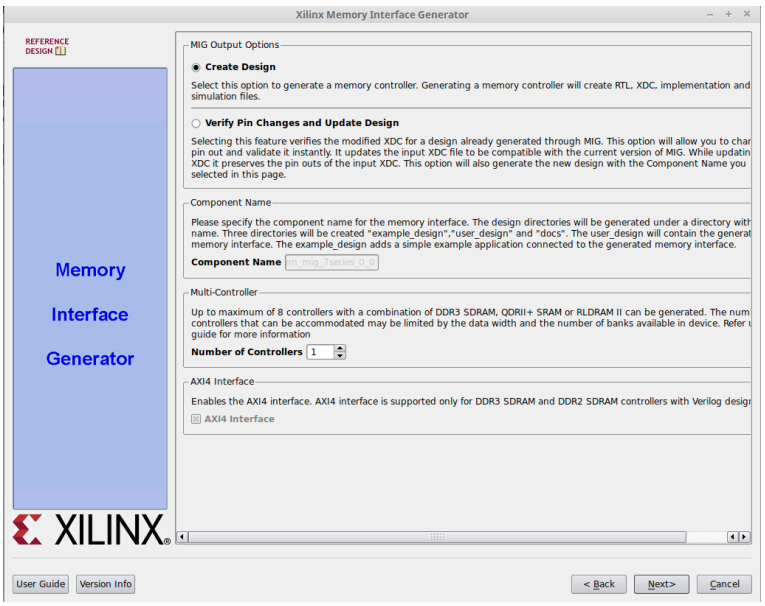

Figure 2: Creating Design

10. In the Pin Compatible FPGAs page, select nothing and click Next.

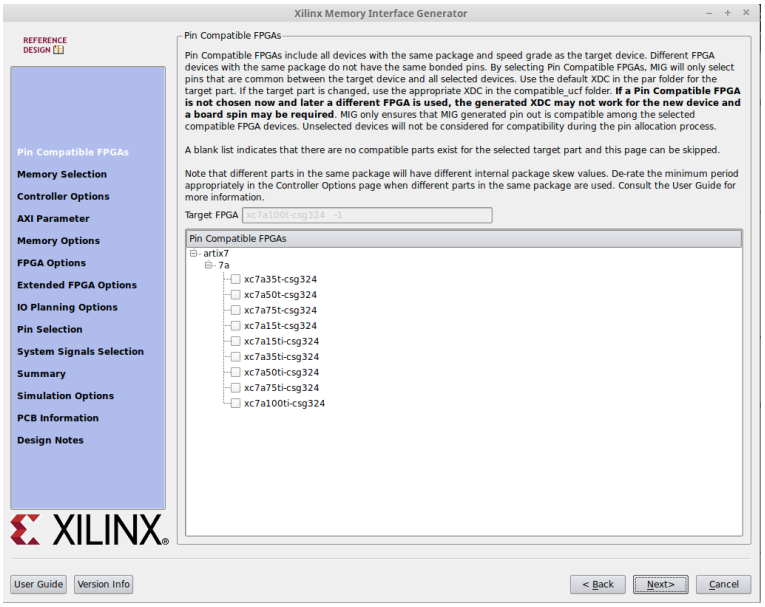

Figure 3: Pin Compatible FPGAs

11. Make sure that DDR2 SDRAM is checked and click Next.

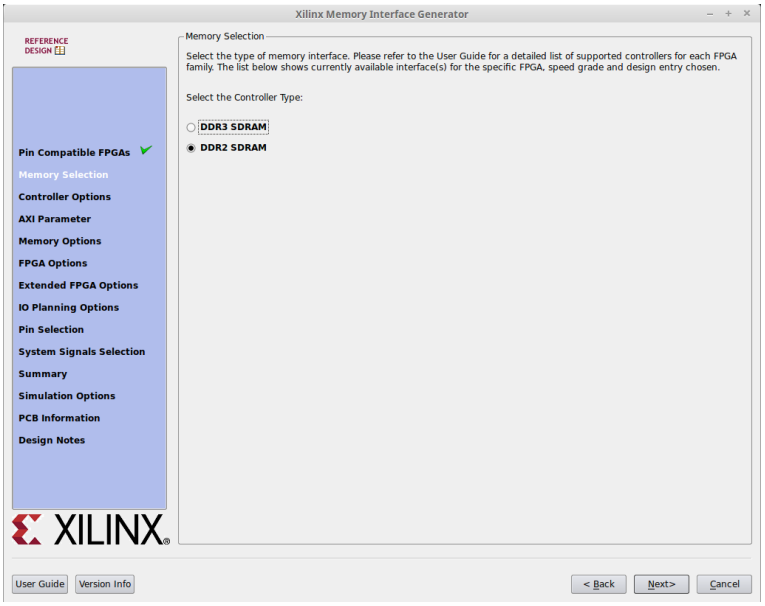

Figure 4: Memory Selection

12. Set the value of the Clock Period to 3077 ps (324.99 MHz). Make sure the Memory Part is MT47H64M16HR-25E and click Next.

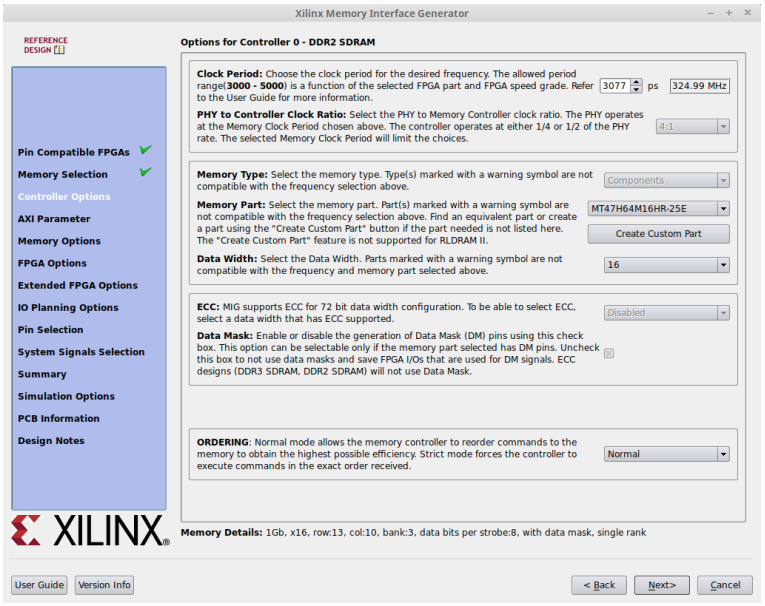

Figure 5: Controller Options

13. In the AXI Parameters Options page, Set Data Width to 64, Narrow Burst Support to 1 and click Next.

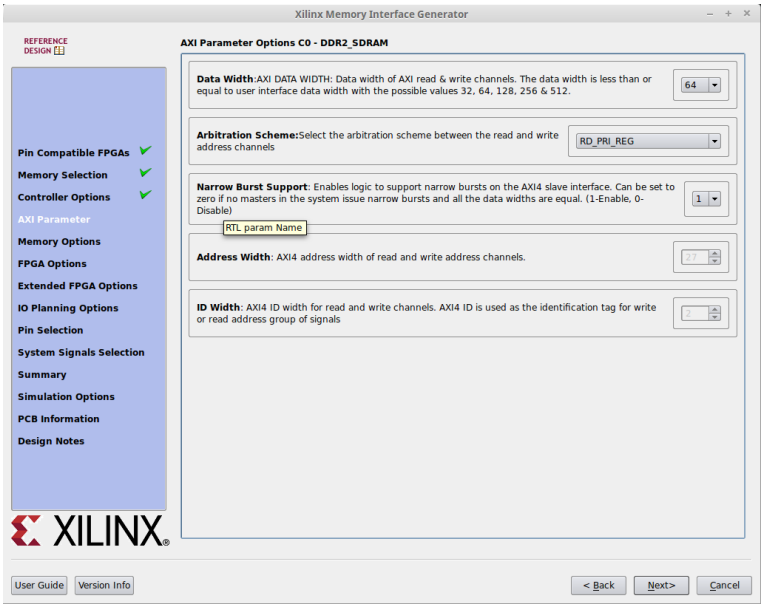

Figure 6: AXI Parameters

14. In the MIG Memory Options page, set the Input Clock Period to 5000 ps (200 MHz) and leave the other options unchanged. Click Next.

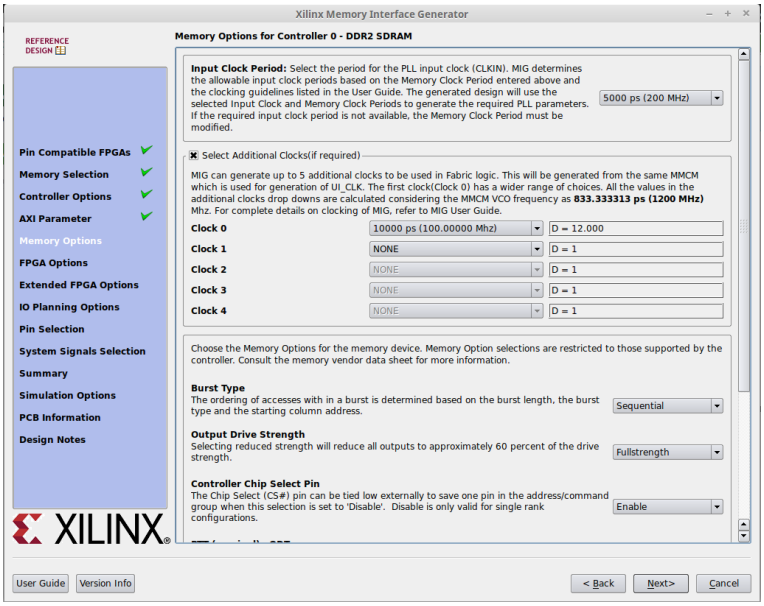

Figure 7: Memory Options

15. On the FPGA Options page, change the System Clock to “Single Ended” and leave the other options unchanged. Click Next.

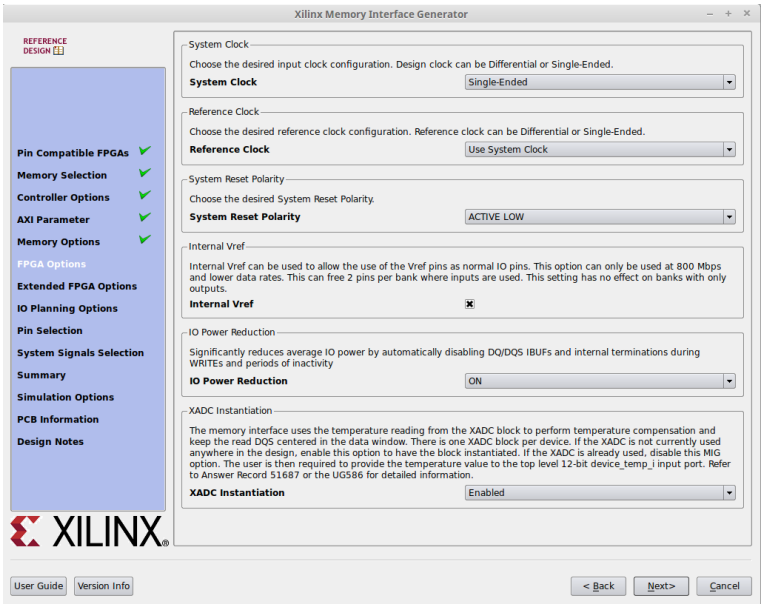

Figure 8: FPGA Options

16. Make sure that the internal termination impedance is 50 ohms. Click Next.

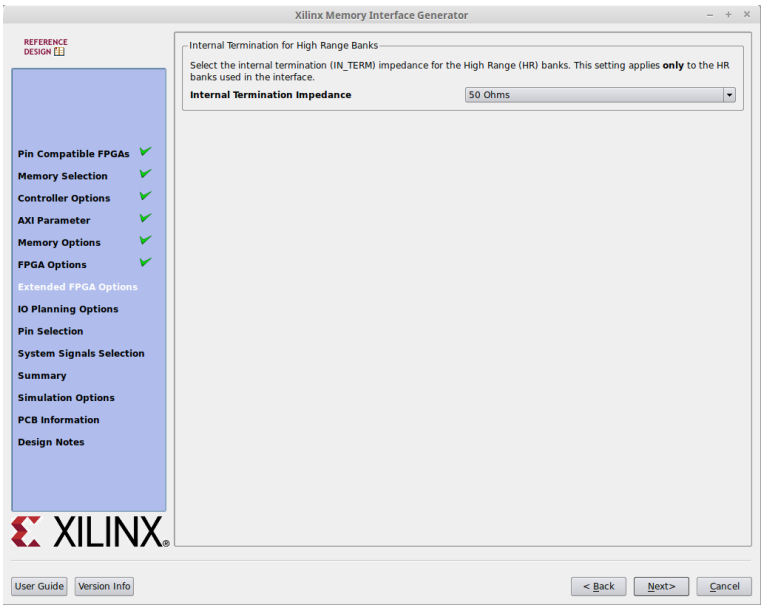

Figure 9: Extended FPGA Options

17. In the I/O Planning Options page, select “Fixed Pin Out”. Click Next.

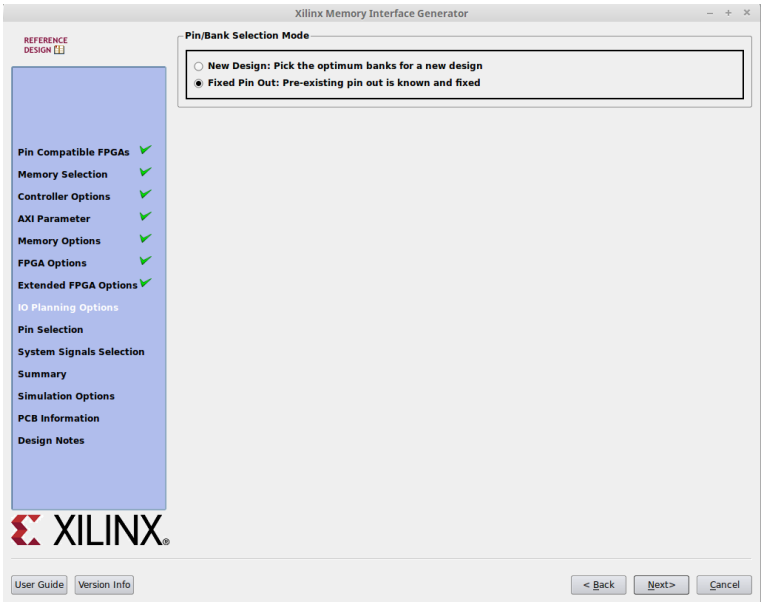

Figure 10: I/O Planning Options

18. In the Pin Selection page, click "Validate" and click Next.

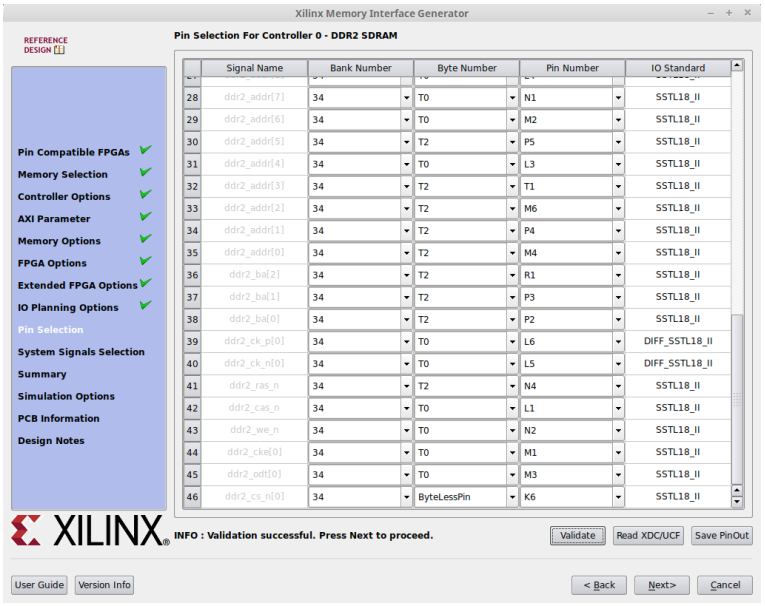

Figure 11: Pin Selection

19. In the Systems Signal Selection page, for *sys_clk_i*, select 35 for the Bank Number and E3 (MRCC_P) for the Pin Number. Leave the other options unchanged. Click Next.

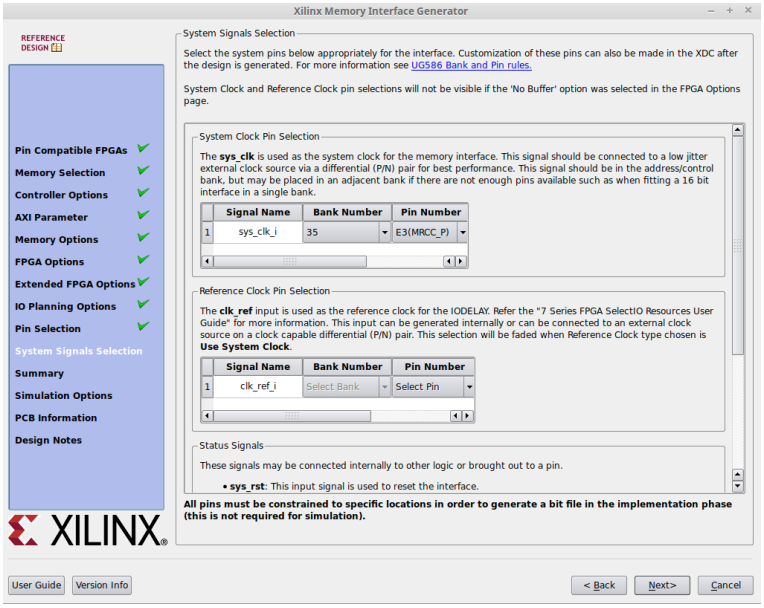

Figure 12: System Signals Selection

20. Click Next through the Summary page and accept the license agreement. Click Next through the PCB Information page and finally click on "Generate".

21. Go back to your block design and click on "Run Connection Automation". Check "S_AXI" only and click OK.

22. Connect the "sys_reset" pin on the MIG IP to the btnCpuReset pin.

23. Connect the "sys_clk_i" pin on the MIG IP to the "clk_out2" pin on the Clocking Wizard.

24. Right click on the DDR2 pin on the MIG IP and click "Make External".

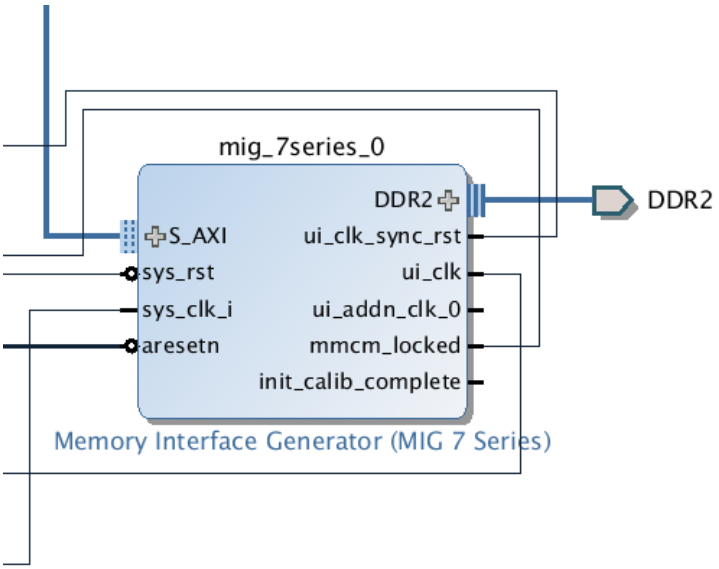

Figure 13: Make DDR2 External

25. Save the Block Design and make sure that only the pins being used in your design are uncommented in the .xdc file.

4 Generate Bitstream

1. Open the block design, right-click and select "Validate Design". This checks for possible errors or critical warnings

2. In the Flow Navigator, click on "Project Settings" and then click on the "Bitstream" menu.

3. In the tcl.pre option, browse and select the attached tcl script named "drc_err_warning.tcl". This script is being added to set a property that downgrades a DRC error to a warning. If the property specified in this script is not set, a DRC error related to the routing of the clock feeding the MIG IP will be reported and bitstream generation will fail. This is a bug in Vivado 2016.2!

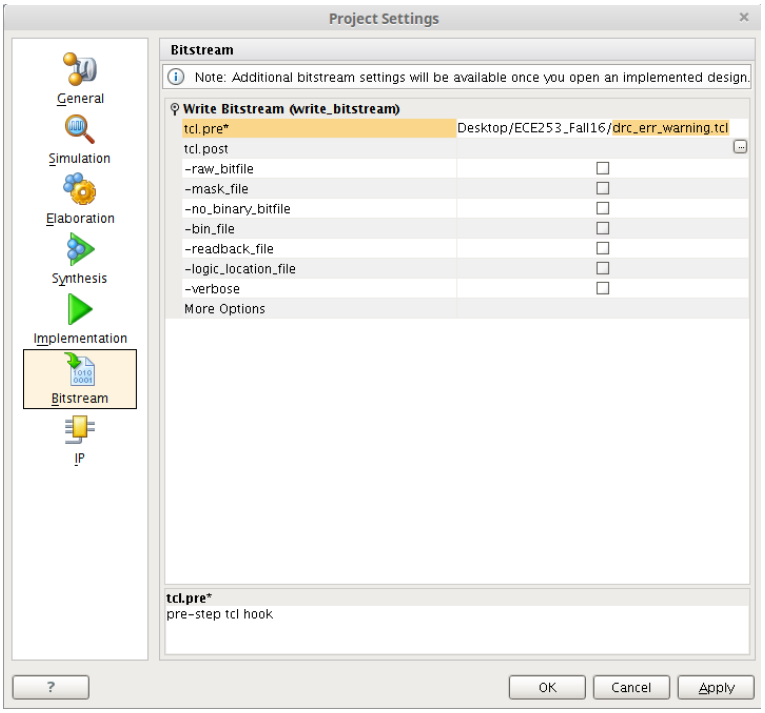

Figure 14

4. In the Flow Navigator, click on "Generate Bitstream". Vivado may ask if it can re-synthesize the design and run implementation. Click yes, and wait. It can take up to 30 minutes to generate a bitstream.

5 Exporting your hardware design to the software SDK

1. Open the implemented design and the block design. Failing to have the implemented design and block design open in Vivado will cause the bitstream to not be exported.

2. Click on File : Export : Export Hardware

3. Leave the default destination and check **Include Bitstream**.

4. Click on File : Launch SDK, OK.

6 Starting a Project in the SDK

1. Click on "File:New:Application Project"

2. Name your project and select 'Create New' for the BSP. Press Next.

3. Select "Memory Tests" from the choices and press "Finish".

4. In the Project Explorer, your project folder (named same as the project) contains a **"src"** folder which has all the .c and .h files for the project.

5. **memorytest.c** contains the main() for this project that calls functions to test the DDR memory.

7 Running your Project

Connect the Artix7 board to the USB port of the Computer. Make sure the Power jumper is connected to USB and make sure the JTAG is enabled by connecting the two center pins in the mode selector.

1. Turn on the board with the switch

2. Back in the SDK, click on "Xilinx Tools:Program FPGA"

3. Once the board is programmed right click on your project folder and select "Run As: Launch on Hardware (GDB)". The console might show an error about not being connected to UART. To fix this, click on "Run:Run Configurations" and select the tab STDIO Connection.

4. Select JTAG UART as the Port. Click Run.

5. The console should now display the results of the various memory tests. If everything is configured correctly, all the memory tests should have "PASSED".