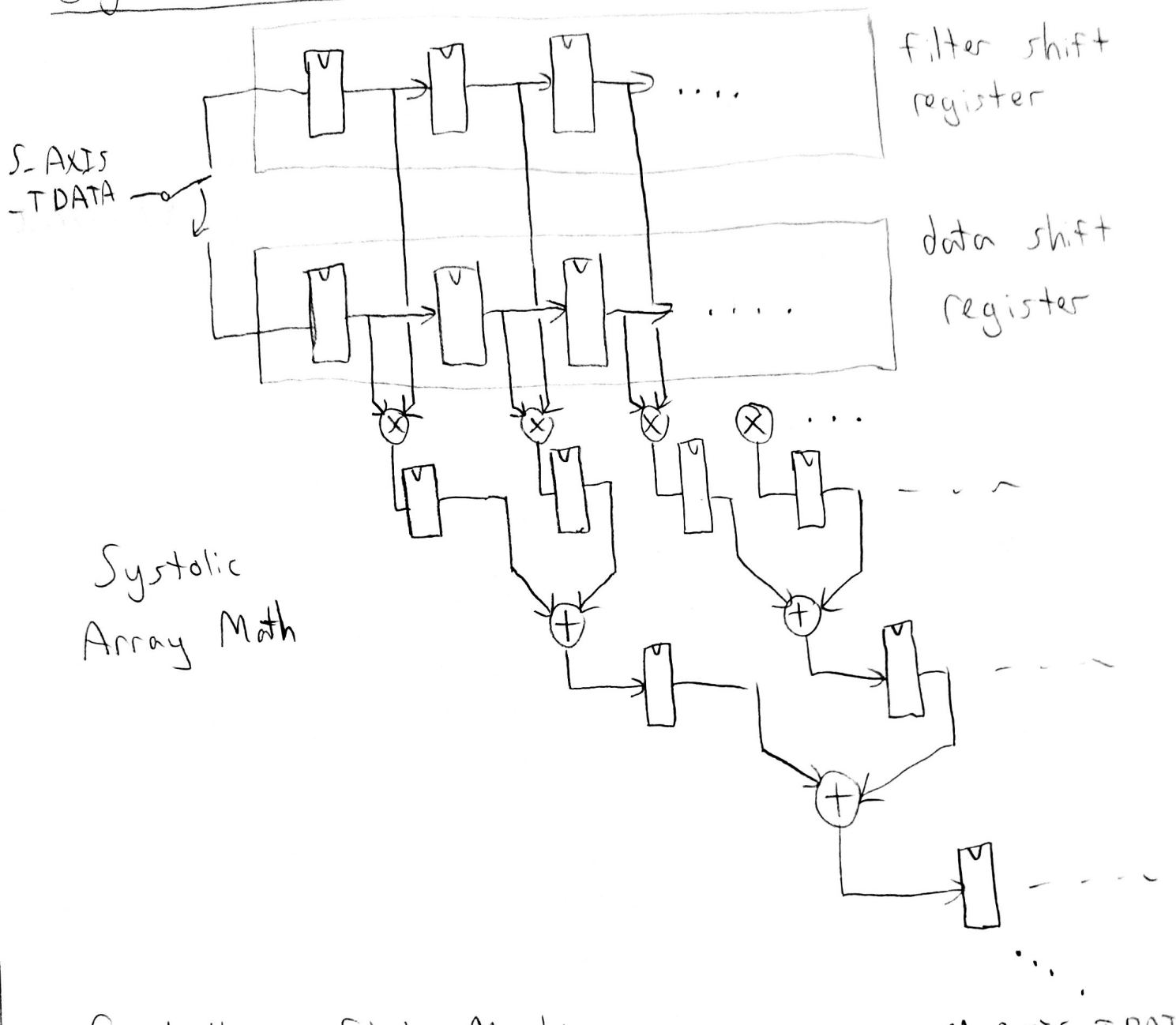
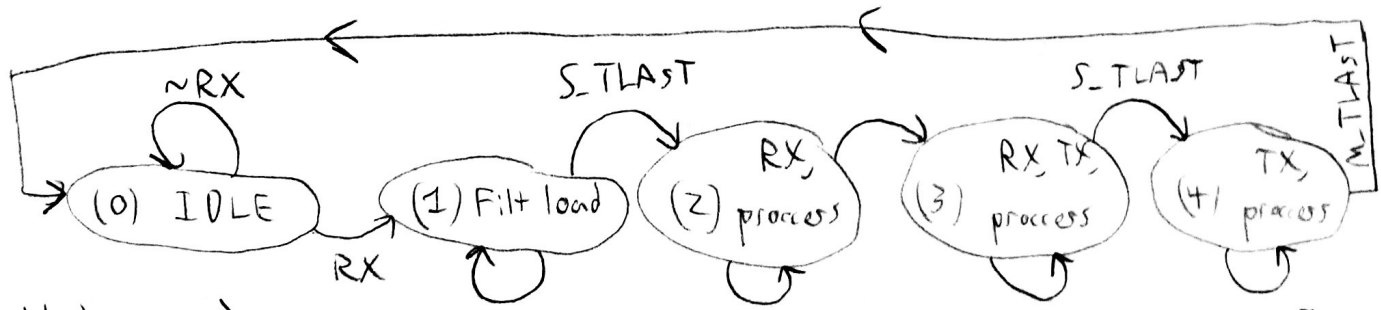
Systolic Array Design:



Controlling State Machine



(for padded conv, result is N+M-1 long)

Repeat for filter length

Repeat for delay latency

Repeat for data length minus latency

Repeat for latency & filter length