

# Scaling silicon-based quantum computing using CMOS technology: State-of-the-art, Challenges and Perspectives

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Complementary metal-oxide semiconductor (CMOS) technology has radically reshaped the world by taking humanity to the digital age. Cramming more transistors into the same physical space has enabled an exponential increase in computational performance, a strategy that has been recently hampered by the increasing complexity and cost of miniaturization. To continue achieving significant gains in computing performance, new computing paradigms, such as quantum computing, must be developed. However, finding the optimal physical system to process quantum information, and scale it up to the large number of qubits necessary to build a general-purpose quantum computer, remains a significant challenge. Recent breakthroughs in nanodevice engineering have shown that qubits can now be manufactured in a similar fashion to silicon field-effect transistors, opening an opportunity to leverage the know-how of the CMOS industry to address the scaling challenge. In this article, we focus on the analysis of the scaling prospects of quantum computing systems based on CMOS technology.

Quantum computation has just entered a new era, that of Noisy Intermediate-Scale Quantum (NISQ) technologies in which quantum advantage has been demonstrated [1]. This remarkable achievement represents an important milestone in quantum computing research and brings focus towards the ultimate goal of the quantum computing roadmap: building a universal quantum machine. A machine with sufficient error-free computing resources to run quantum algorithms with the potential to transform society.

Fault-tolerant quantum computing requires resilience against errors. Topological quantum computing models based on non-Abelian anyons, of which most characteristic example is that of Majorana zero modes, offer protection at the qubit level [2, 3]. However, so far, the most technologically promising routes to fault-tolerant quantum computing are based on the standard quantum computing paradigms that use noisy qubits in combination with Quantum Error Correction (QEC) [4–6]. In this scheme, topological protection is achieved by distributing the logical information over a number of physical qubits, as long as each satisfy a maximum error rate in the combined initialization, manipulation and readout. The most forgiving QEC method, the surface code, sets a 1% upper bound [7]. The exact physical qubit overhead (per logical qubit) depends strongly on the error rate but considering state-of-the-art qubit fidelities, it will likely be a figure in excess of a thousand [8]. QEC is then expected to take the number of required physical

qubits to many thousands and possibly millions for economically significant algorithms [9, 10] and to many millions or billions for some of the more demanding quantum computing applications such as Shor’s factorization algorithm [11]. Large-scale integration is hence a requirement to implement QEC schemes and a technological challenge for the most advanced quantum computing platforms relying on superconductors, semiconductors, ion traps or photonic circuits as the physical hosts for the qubits [12–15].

Recently, important developments in the field of nanodevice engineering have shown that qubits can be manufactured in a similar fashion to field-effect transistors (FET) [18], creating an opportunity to leverage the integration capabilities of the semiconductor industry to address the up-scaling challenge. From a technological perspective, CMOS-based quantum computing brings two key ingredients favouring large-scale integration: (i) a small qubit footprint, of the order of  $100 \times 100 \text{ nm}^2$ ; and (ii) compatibility with well-established, highly reproducible Very Large-Scale Integration (VLSI) techniques of the CMOS industry that routinely manufacture billions of quasi-identical transistors on the size of a fingertip. Those two ingredients may allow building compact fault-tolerant quantum processors that can fit in conventional cryostats without requiring the technically challenging development of large-scale infrastructures [19]. Furthermore, a quantum processing unit (QPU) will likely be a sub-module of a larger information processing system containing also analogue and digital electronics. In that scenario, CMOS could enable hybrid integration of quantum and classical technologies facil-

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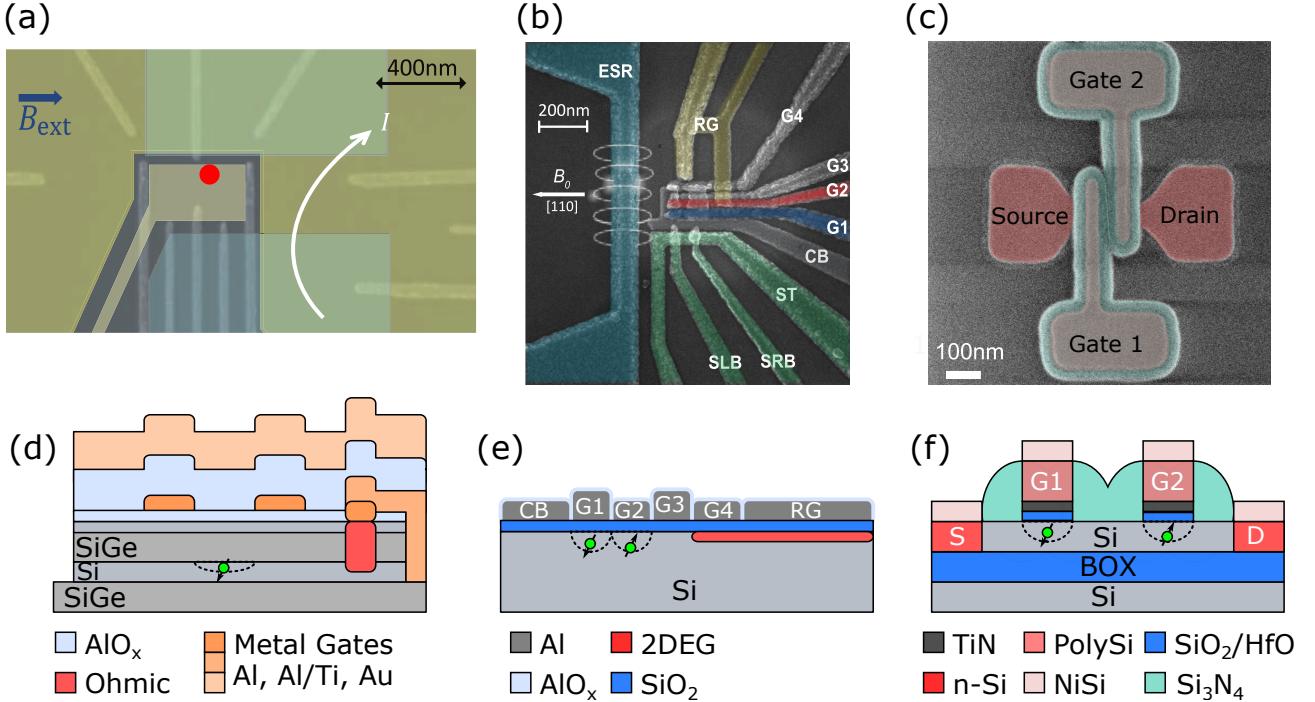


FIG. 1. Silicon quantum dot devices. (a) Scanning electron microscope (SEM) image of an accumulation mode Si/SiGe heterostructure. Two layers of gates, bottom (light grey) and top (dark green) are designed to form two quantum dots (centre of image) and a single-electron transistor for readout (right). The structure contains a micromagnet in an upper metal layer (light green) to produce a magnetic field gradient. The red dot indicates the position of a quantum dot used in ref. [16]. (b) SEM image of a metal-oxide-semiconductor multi quantum dot device with quantum dot gates (G1-4), confinement gate (CB), reservoir gate (RG), an integrated single-electron transistor (green) and microwave antenna for magnetic resonance spin control (blue) used in ref. [17]. (c) SEM image of a CMOS p-type double quantum dot on an etched silicon-on-insulator nanowire used in ref. [18]. Cross-sectional view of the Si/SiGe quantum dot device (d) MOS double quantum dot device (e) and CMOS double quantum dot device (f) shown above in (a-c).

tating data management and fast information feedback between them. And, even before a fault-tolerant quantum computer is built, compact CMOS manufacturing could deliver multi-core NISQ QPUs [20], ideal for hybrid quantum-classical algorithms that benefit from massive parallelisation [21, 22].

In addition to the technological benefits, silicon offers favourable physical properties enabling the realization of qubits with long coherence. The qubits are encoded by localized spins at deep cryogenic temperatures and finite magnetic fields. The simplest example is the spin  $\frac{1}{2}$  of a single electron (or hole) electrostatically confined in a quantum dot, as originally proposed by Loss and DiVincenzo [23]. Alternatively, one can use the nuclear spins of individual embedded dopants, as proposed by Kane [24]. Nowadays, quantum dots can be manufactured on demand at the interface of a silicon MOS nanodevice (typically Metal-SiO<sub>2</sub>-Si) [25] or Si/SiGe heterostructure [16], see Fig. 1(a,b). Recently, large enhancements in spin coherence were achieved by isotopic enrichment of the silicon lattice. The 5% naturally occurring spin-carrying isotope, <sup>29</sup>Si, is the major source of decoherence in sili-

con, whereas the dominant <sup>28</sup>Si isotope has zero nuclear spin. By enriching to nearly pure <sup>28</sup>Si, with only 800 ppm of <sup>29</sup>Si remaining, inhomogeneous spin-dephasing times ( $T_2^*$ ) and spin-coherence times ( $T_2$ ) exceeding 100  $\mu$ s and 20 ms, respectively, have been measured for electron spins placing silicon as one of the most coherent solid-state systems in nature [25]. For optimal performance, silicon qubits are cooled down to a few tens of millikelvin under magnetic fields of the order of 1 T but these parameters may be relaxed in the future [26–28].

Silicon spins qubits are initialized and read out using spin-to-charge conversion techniques [29–34], they are coherently manipulated via magnetically- or electrically-driven electron-spin-resonance for single-qubit operations [16, 35, 36] and spin-exchange-based methods for two-qubit logic [37]. Thanks to the increase in coherence, advancements in high-frequency readout techniques, and optimized spin projection mechanisms, all these steps have now been performed with fidelities approaching the requirements of the surface code. These are promising initial results for this relatively recent approach to quantum computing, indicating that attempting to build a

fault-tolerant quantum computer based on silicon technology is a realistic proposition. However, many technological challenges lie ahead. So far most of the aforementioned milestones were achieved with small-scale devices (one- or two-qubit systems) fabricated in academic clean-rooms offering relatively modest level of process control and reproducibility [17, 38, 39]. From this point onwards, a route to increase fidelities well beyond fault-tolerant thresholds in a reproducible way across large arrays of qubits needs to be established.

Some recent results demonstrating a qubit in an industry-standard CMOS platform [18] may shed some light on how to achieve this goal and could trigger a transition from lab-based demonstrations to spin qubits manufactured at scale, see Fig. 1(c). In this Article, we focus on the scaling prospects of quantum computing systems based on CMOS technology, discuss the state-of-the-art, highlight development challenges and provide our own personal perspectives to tackle them. The rest of the paper is structured as follows. In Sec. I, we discuss the concept of Quantum Processing Unit and explain the different elements that may constitute it. After, we examine the challenges at the Quantum Layer, Sec. II, and the common challenges when designing classical CMOS circuits at cryogenic temperatures, Sec. III, that affect both the Quantum-Classical Interface, Sec. IV, and the Classical Layer, Sec. V. We discuss the functional assembly of the layers into an Architecture, section VI, and finally, in Sec. VII, we present our conclusions.

## I. A QUANTUM PROCESSING UNIT

The problem of scaling requires a shift in the thinking process beyond the one- and two-qubit quantum processor proof-of-principle demonstrations to a full stack perspective: A Quantum Processing Unit [40]. Researchers have already started to tackle this problem, producing blueprints of what a large-scale quantum computer could look like in silicon [41–44]. These proposals share a common basic idea. The future silicon QPU should be composed of three distinct layers: the Quantum Layer, the Quantum-Classical Interface and the Classical Layer, all of which could potentially be manufactured using CMOS technology, at least to a certain extent. In Fig. 2(a), we present a schematic description of the distribution of the layers and in Fig. 2(b), we show a more granular description of the elements and the connectivity between layers.

First, the Quantum Layer. The configuration of the Quantum Layer is primarily dictated by the physical requirements of the surface code, see Fig 3(a): a two-dimensional distribution of physical qubits with nearest-neighbour interactions [7]. The qubits are split into data qubits – qubits in which the computational quantum states are stored (white circles) – and measurement qubits – qubits performing error detection (black circles). Measurement qubits come in two types, X and Z syndrome qubits which contribute to the measurement of

bit-flip and phase-flip errors, respectively. Each X-type and Z-type qubit is made to interact in an anticlockwise sequence with the four adjacent data qubits (yellow and green ellipses) and then measured to extract information of the system (stabilizer). The stabilizers can be measured repeatedly without perturbing the quantum state of the system. However, once one or more errors occur, the outcome of a stabilizer measurement changes. By correlating stabilizer outputs, the location of an error can be identified and then corrected. In silicon, the surface code could be implemented in a  $^{28}\text{Si}$  substrate, by distributing in a square array individually-addressable nanometer-scale MOS structures to enable the formation of few-electron quantum dots plus additional gates in between to control, locally, the exchange interaction between spins. Given the projective nature of spin readout, as we shall see in Sec. II, the surface code could be implemented in a  $2 \times 3$  quantum dot sublattice, using planar designs [41], or in a canonical  $2 \times 2$  sublattice, although this would involve using 3D integrated structures [45], see Fig 3(b).

Second, the Quantum-Classical Interface that will handle the control and readout of the individual qubits as well as the routing and input/output data management of the large number of signals required to operate the Quantum Layer [46]. This layer contains signal generators, (de)modulators, analog-to-digital (ADCs) and digital-to-analog converters (DACs) and amplifiers for control and readout and (de)multiplexing for I/O control (see Fig. 2(b)).

Finally, the Classical Layer, designed to assist in the QEC process by taking the outputs of the Quantum Layer via the Quantum-Classical Interface and correlating them, in classical logic, with a concrete error type, location and time step. Errors can be generally corrected in software but in order to enable universal computation, including non-Clifford operations, fast active feedback between readout and control would be necessary. Furthermore, the Classical Layer is expected to translate the quantum algorithms into a sequence of interleaved control and readout steps of the relevant qubits. This layer contains a processing unit (FPGA or ASIC) that, within the cooling power constraints of cryogenic systems, should be placed in close proximity to the rest of the layers to reduce latency in feedback operations.

The physical architecture of the QPU is still a matter of debate. In fact, it is likely that a number of approaches could be followed. The flexibility in the physical arrangements of the layers and the square-grid distribution of the quantum dots evoke image sensors as an example of the foreseeable future for CMOS-based quantum computing, see Fig 3(c). Charge Coupled Devices (CCDs) or CMOS image sensors, competing image technologies, both fulfill their image recording purposes but with a different set of specifications given their different levels of integration [47]. In both technologies, the physical layout is constituted by a two-dimensional array of unit cells (pixels). In the case of CCD, charge-to-voltage conversion occurs

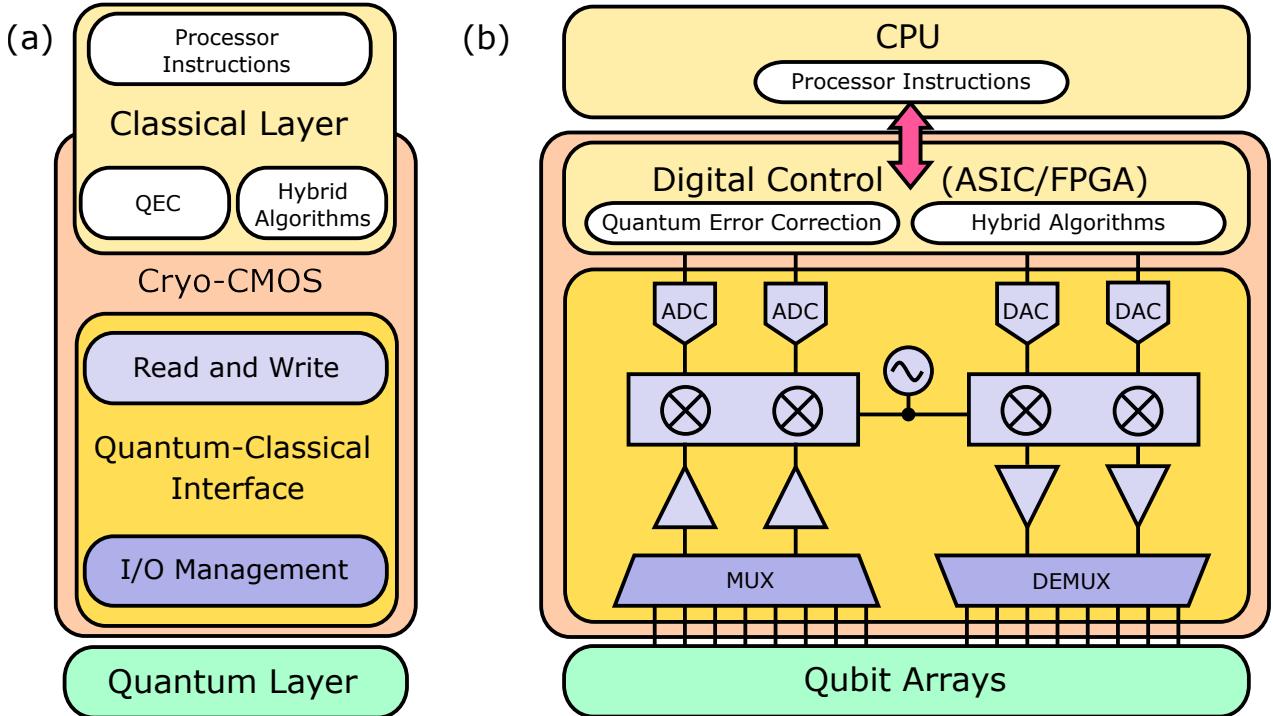


FIG. 2. A Quantum Processing Unit. (a) Schematic representation of the main layers of a QPU. (b) A more detailed representation of a QPU including the interconnection between modules. The quantum-classical interface uses (de)multiplexers to facilitate input/output data management. These components could operate using time-domain and frequency-domain multiplexing. Control and readout micro- and radio-wave tones are produced by IQ modulation and amplification and readout signals are detected after amplification via IQ demodulation. The digital controller is used for fast feedback between the classical and quantum units, especially for hybrid quantum-classical algorithms and quantum error correction, and also to send the quantum computer instructions received from a classical computer. It interfaces with the rest of the layers via ADC/DACs.

via shifting charges sequentially to a global amplifier sitting at the periphery. However, in the case of CMOS sensors, such as active-pixel sensors, readout occurs in a distributed manner with a first stage of amplification at the pixel level, followed by column and global amplification at the periphery, Fig 3(d). The different architectures result in a different set of technical specifications that can be tailored to the specific application. CMOS-based quantum computing could follow a similar path of development in which some architectures could have either local or global electronics for control and readout. Global techniques are likely to simplify the integration process and deliver architectures sooner, while local integration will provide enhanced functionality. We note that although the analogy works in first order approximation, qubits present radical differences to pixels. Qubits have comparably smaller footprints and qubit-to-qubit interactions need to be managed. These drastic differences impose restrictions for local electronics that will require technological innovation beyond state-of-the-art image sensors.

We see there is flexibility in the way ahead, that the optimal qubit cell is still to be defined (see Fig 3(e)), but also see that the abstract description of a quantum machine presented above has some clear consequences on

the required conditions to build a QPU. In the following, we present the areas where silicon quantum information processing could benefit from the know-how of the CMOS community.

## II. CHALLENGES AT THE QUANTUM LAYER

### A. Qubit Arrays

The first challenge pertains to the use of commercial-scale CMOS manufacturing lines to enable the fabrication of dense two-dimensional arrays of individually addressable gate-defined quantum dots with gate-controlled tunnel barriers. The unit cell of the qubit is likely to contain additional commensurable electronics either in-plane or in a 3D geometry, as discussed in detail in Sec. VI. Here, we exclusively concentrate on the quantum dot array.

The characteristic footprint of the gate electrodes that have been used to define few-electron quantum dots in CMOS platforms has been of the order of  $40 \times 40$  nm (width and length) with a gate pitch of 70 nm [18, 48–50], although these dimensions may differ depending on the exact gate stack. The dimensions are in line with the

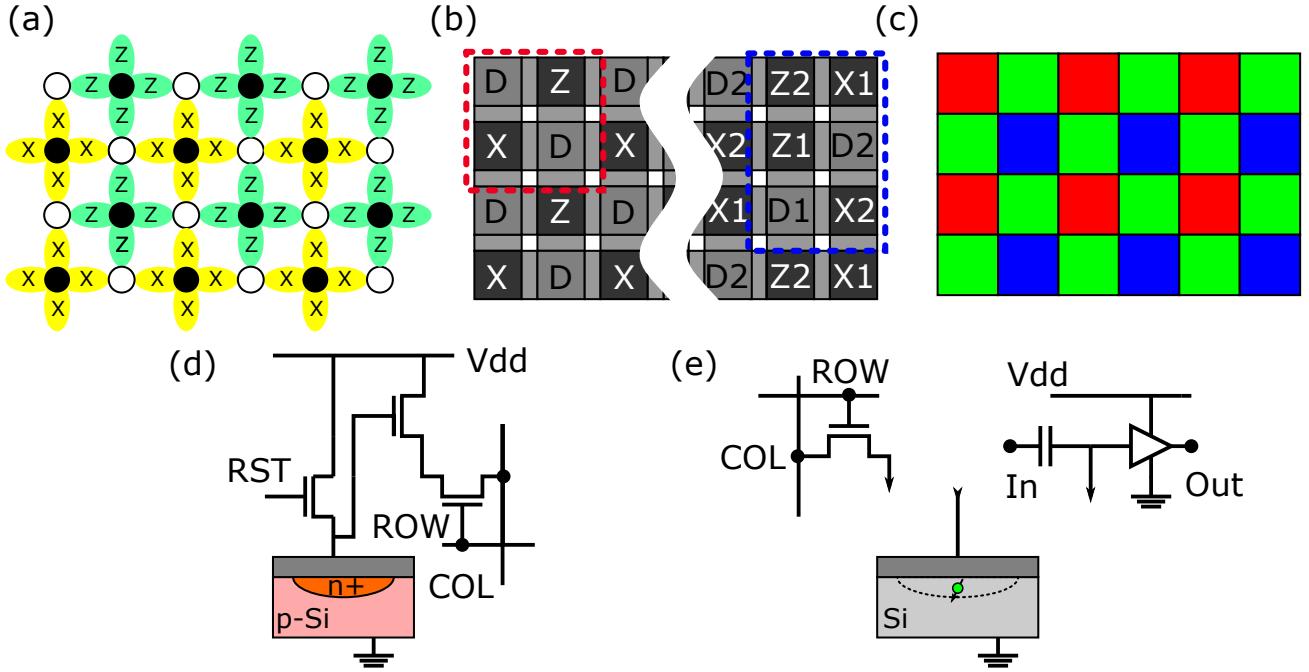


FIG. 3. Two-dimensional arrays. (a) Graphical representation of a two-dimensional qubit array with nearest neighbour interactions necessary to implement the surface code. The hollow dots are data qubits and the black dots are error detection qubits, either X or Z syndrome, redrawn from [7]. (b) Schematic representation of two ways of assigning data (grey) and syndrome qubits (dark gray) in a two-dimensional gate electrode array with tunable exchange gates (light grey). (Left) Standard 2x2 qubit sublattice (delimited by the red dashed line) that will require of vertically integrated readout [45]. (Right) Extended 2x3 qubit sublattice (delimited by the blue dashed line) with two additional syndrome qubits to enable readout in the plane [41]. (c) Graphical representation of a digital image sensor formed by a two-dimensional array of photodiodes (pixels) combined with filters to detect specific wavelengths (RGB). (d) Schematic of a three-transistor active pixel sensor, including a reset transistor for the photodiode (RST), a source-follower readout transistor and a selection transistor addressed via row-column inputs. (e) Cross-section schematic of a single-electron MOS quantum dot with possible combination of classical electronics. Left) Row-column access transistor for 2D addressing. Right) Local amplification at the cell level.

22 nm CMOS node and are not likely to pose a critical problem. However, the routing of the individual lines will be a major challenge, see Sec. IV A. In addition, the necessity to have a tightly packed exchange gate in between adjacent quantum-dot gates to control the interaction between spins, presents a significant challenge. Currently, there is no standard CMOS technology node that could deliver the required 2D gate array layout. Research efforts should be devoted to developing multi-gate-layer processes in CMOS foundries that will enable configuring exchange gates. So far two technological paths have been pursued to design the exchange gates: (i) three levels of overlapping gates [37, 51] and (ii) self-aligned barrier gates using chemical-mechanical polishing [44].

Currently, modules containing linear and bilinear arrays of quantum dots are being explored [50, 52–55] in which NISQ algorithms or logical qubits could be implemented [56]. This modular approach could help to tackle the scaling problem in successive approximations, first by producing 1D arrays, then by combining them in 2D arrays with sparse connectivity, and finally by helping develop the basic knowledge and technology to produce a fully-connected 2D architecture.

## B. High-fidelity control

When using electrons as the spin carrying particle, silicon-based spin qubits coming from academic research laboratories have so far reached single-qubit fidelities exceeding 99.9% in 200 ns [57], and two-qubit fidelities as high as 98% in 5  $\mu$ s [17]. While there is ample room for improvement, the challenge is to achieve gate-set fidelities well above 99% across a large array of qubits on timescales of the order of a microseconds or less to enable fast active error-correction protocols and minimise computation time. Achieving high-fidelity control requires managing the trade-off between manipulation speed and qubit coherence since typically physical mechanisms that allow for fast control also open channels for unwanted de-coherence.

Single-qubit rotations are typically achieved with electron spin resonance techniques that require the delivery of pulsed oscillatory magnetic (ESR) or electric fields (EDSR), typically in the 5 to 40 GHz range. The ESR implementation requires either the fabrication of on-chip antennas [58] or the placement of the chip inside a resonant microwave cavity [24], although this latter approach

has not yet been experimentally demonstrated for individual spin qubits in semiconductor quantum dots and is likely to lead to very significant heating since all metallic structures will have induced currents. The resonant microwave signal can be pulsed, to drive single spin rotations in-phase (X rotations) or in quadrature (Y rotations) [36]. Alternatively, a constant ESR signal can be applied, and qubits can be tuned in and out of resonance making use of the Stark shift using local pulses at the qubit gate [59]. Rotation rates are rarely much faster than a few MHz given the heat associated with producing B-field pulses with sufficient amplitude at the qubit location.

Alternatively, EDSR induces spin rotations by making use of spin-orbit coupling that converts oscillatory electric fields into oscillatory magnetic fields in the reference frame of the electron [35, 60]. Typically, micro-magnets are necessary to introduce synthetic spin-orbit interactions with sufficient strength to drive coherent rotations. Using this approach, rates up to tens of MHz have been reached [57]. However, the increased spin-orbit coupling created by the micromagnet field gradient also makes the qubit susceptible to electrical noise, which can limit  $T_2$  [57, 61] and may substantially reduce the relaxation time,  $T_1$  [62]. Careful engineering of micromagnet arrays will be crucial for improving the performance of EDSR-driven quantum dot electron spin qubits and to enable this methodology to be applied at scale. On the other hand, intrinsic spin-orbit coupling, of which there is enhanced evidence in low symmetry quantum dots [48], or in holes rather than electrons [63], may facilitate scaling since manipulation will not require additional elements in the qubit cell. Efforts in this direction will be worth exploring further experimentally and theoretically.

Two-qubit gates are based on the exchange interaction between neighbouring spins. The exchange strength ( $J$ ), which depends on the wavefunction overlap between participating charged particles, can be varied by changing the voltage detuning between quantum dots (asymmetric tuning) [37] or by tuning the potential barrier between dots (symmetric tuning) [64–66]. Symmetric tuning is less sensitive to charge noise allowing exchange coupling operations at a sweet spot where the  $J$  has zero derivative with respect to voltage detuning. The short-range nature of the exchange interaction and the preference for symmetric tuning, impose the tightest restriction on the gate layout as explained above: a quantum-dot gate pitch of the order of 70 nm and an exchange gate in the space between of adequate footprint to tune the exchange interaction by several orders of magnitude between the ON and OFF states (when  $J/h$  should be much smaller than the single- and two-qubit gate speeds).

Two-qubit gates can be performed in two distinct ways, either via exchange modulation or resonantly. Exchange modulation involves pulsing the exchange interaction. Depending on the pulse scheme a CPhase [37] or a  $\sqrt{\text{SWAP}}$  gate [32, 67] can be implemented. In the latter case, a subnanosecond two-qubit gate has been

demonstrated for P-donor spins in silicon [67], emphasizing the speed advantages of gate-voltage pulses over resonant two-qubit gate schemes. Resonant two-qubit gates involve turning on the exchange interaction and performing ESR/EDSR on the coupled two-spin system to perform a CROT gate [17, 38] which has, to date, set the benchmark for two-qubit gate fidelity: 98% in 5  $\mu\text{s}$  [17].

Going beyond one and two-qubit interactions, control at scale requires careful management of crosstalk between closely spaced qubits. Research should be directed towards assessing the impact of manipulating target qubits on idle qubits (or even simultaneously addressed qubits) and determine compensation signals to minimise this effect. Benchmarking of the optimal gate-set in terms of fidelity, operation timescales and impact on deselected qubits must be undertaken.

### C. High-fidelity readout

To implement fast feedback in active error correction protocols and minimise the duration of the surface code cycle, high-fidelity readout needs to be performed in times much faster than the spin dephasing time [68], setting the challenge to achieve a readout fidelity well above 99% in timescales of the order of a few microseconds or less [69]. Readout of spins in silicon is achieved by spin-dependent tunnelling processes that translate the spin information to a charge-based signal that can be read using amplification techniques [29, 70]. The most commonly used method, the single-electron transistor (SET), has an upper bandwidth limit of a few tens of kHz, but this can be extended to hundreds of kHz using co-integrated transistors [71] or to tens of MHz using high-frequency LC impedance matching techniques [72, 73]. With these two approaches readout fidelities of 99.9 % in 6  $\mu\text{s}$  [74], and 97 % in 1.5  $\mu\text{s}$  [75], have been achieved respectively. An alternative method, gate-based readout, simplifies the architecture by removing the charge sensor and directly embedding the qubit in a radio- or microwave frequency electrical resonator [76–82]. The resonant state of the circuit is then conditional on the qubit state which manifests as an additional quantum capacitance [83]. With this methodology a readout fidelity of 98 % in 6  $\mu\text{s}$  has been obtained [84]. High-frequency techniques enable simultaneous readout via frequency-domain multiple access (FDMA) [85]. Furthermore, gate-based readout can be used in conjunction with quantum-limited Josephson parameter amplification to speed up the readout [86], see Sec.IV B.

In both cases, the footprint of the resonator (or inductor in lumped-element configurations) poses a challenge in terms of scaling with typical footprints of the order of  $100 \times 100 \mu\text{m}$ . Research on industry-compatible high kinetic inductance materials [87], like TiN, with an inductance of  $L_K = 234 \text{ pH/sq}$  in 8.9 nm thin films [88], could drastically reduce the resonator footprint to sub

micrometer square. Josephson metamaterials formed by arrays of Josephson junctions may also be a compact alternative [89]. Additionally, time-division multiple access (TDMA) techniques could enable reducing the total number of resonators by performing qubit readout in a sequential manner using a common resonator [90].

If SET readout is to be pursued, research efforts should be directed at increasing the bandwidth by directly integrating low-power low-noise amplifiers on chip. The community should also think of ways to go beyond SETs and resonators by adapting concepts from classical electronics to resolve the capacitance associated the ff-scale capacitance associated with quantum tunneling between adjacent dots [91]. A compact solution that could be integrated on-chip with a footprint commensurable to the qubit size will facilitate the massively parallel readout required for quantum error correction codes.

#### D. Qubit Variability

Possibly one of the greatest challenges is the necessity to manufacture high-fidelity qubits at scale. Although VLSI technology guarantees a high level of reproducibility, variability acquires a much higher degree of importance in the quantum realm, since quantum device performance varies significantly with parameters like the tunnel coupling or the valley-splitting, both of which can be affected by a single atomic defect [92–94]. Special emphasis should be put on the quality of the interfaces and on the purity and crystallinity of the materials.

From a channel material perspective, the development of isotopically enriched Si or Si/Ge stacks will be necessary to provide nuclear spin-free active substrates, which are key to suppressing the spin dephasing associated with the hyperfine interaction. Modules including  $^{28}\text{Si}$  enriched silane for Si, as well as  $^{73}\text{Ge}$  depleted germane for SiGe will need to be developed. Critical issues will need to be addressed such as the correct level of isotopic enrichment, the optimal thickness of the isotopically enriched channel taking into account performance, cost and the thermal budget to cope with the self-diffusion between natural and enriched silicon layers [95].

From a gate stack/dielectric perspective, material development remains critical since charged defects can affect the static and dynamic properties of the qubits. Stacks with minimized trapped charge densities below  $10^{11} \text{ cm}^{-2}$  will be required. This is likely to rule out high-k dielectrics known to have a large density of defects at the  $\text{SiO}_2/\text{high-k}$  interface ( $10^{11} - 10^{12} \text{ cm}^{-2}$ ) and put an emphasis on high quality Si-SiO<sub>2</sub> interfaces, which can have defect densities as low as  $5 \times 10^{10} \text{ cm}^{-2}$ . Furthermore, due to the necessity to operate at cryogenic temperatures, the effect of thermal contraction of different materials will need to be studied and minimised. Thermal contraction mismatch between the gate stack and the device body can lead to defect/strain generation [96, 97] resulting in enhanced variability in the physical location

of the quantum dots. Doped polycrystalline silicon gates are likely to minimise these effects. Tungsten, with a thermal expansion coefficient similar to that of silicon ( $4.5 \times 10^{-6} \text{ K}^{-1}$  vs  $2.6 \times 10^{-6} \text{ K}^{-1}$ ), may be an interesting candidate for lower resistivity gate material. The impact of metal gate granularity on the variability of the gate voltage for quantum-dot formation should also be minimised to avoid workfunction fluctuations [98–100].

Considering now the variability in spin qubit operation frequencies, this is primarily determined by the electron (or hole) G-tensor, which in turn is influenced by a number of device and materials-related parameters, including interface roughness [101] and valley occupancy [102]. The level of variability in G-tensor components for electron spins is also strongly dependent upon the orientation of the static magnetic field with respect to the silicon crystal axes such that when the field is aligned along the [100] axis the variability is strongly suppressed [103]. Residual variability in qubit resonance frequencies can also be corrected for by engineered control pulses.

Finally, variability associated with process changes will also need to be rapidly evaluated at scale to provide statistical evidence of improvement. High-throughput characterization techniques, e.g. based on low temperature ( $< 4 \text{ K}$ ) wafer-scale probe stations or cryogenic multiplexers, will need to be developed to correlate process-induced variability [104–106], and help identifying routes for its control and/or optimization. Furthermore, given the time-requirement to tune multiple gate voltages to bias levels where qubits can be operated, the field will strongly benefit from the development of computer-assisted auto-tuning routines for qubit initialization and parameter extraction [107, 108]. Once sources of variability are minimised, techniques to cope with residual variation will need to be developed, perhaps by constructing machine learning models that anticipate qubit performance from room-temperature diagnostic data.

#### E. Modelling

In order to speed up our understanding of the parameters that have an impact on qubit performance, microscopic modelling is necessary. Modelling provides insights about the optimal methods of operation as well as guidelines for fabrication optimization. The methods to model qubit devices are inspired by techniques used in the CMOS community to understand, for example, disorder and scattering. The main differences with respect to standard CMOS modelling are that, for qubits, modelling needs to be done in the one/few charge regime and rather than simulating electrical currents, the models need to address charge densities and wavefunctions.

From a methodological perspective, finite volume Poisson solvers can initially be used to compute the electrostatic potential in the active region of the device. From there, two methods can be used to compute the figures

of merit such as electron filling, valley-splitting, tunnel coupling, g-factor, exchange coupling strength, etc. The first calculates the  $N$  single-particle states in the electrostatic potential using either a multi-band  $k \cdot p$  or a tight-binding (TB) model [109]. The second leverages existing tool suites and modified effective mass theory [110].

Up to now, these tools have mostly been used *a posteriori* to explain valley-splitting [111, 112], EDSR for electron spins [113] and to model Rabi frequency [114]. Because more statistical data are now being generated, it might be possible to actually build a complete QCAD (Qubit Computer Aided Design) suite that goes from a microscopic description all the way to qubit array simulation.

### III. CHALLENGES FOR CRYO-CMOS DESIGN

Designing electronic circuits at deep cryogenic temperatures poses some major challenges that apply both to the Quantum-Classical Interface and the Classical Layer. In the following subsections, we describe the impact of temperature on device parameters, power dissipation restrictions and the impact of communication latency.

#### A. Temperature effects at the device level

Conventional integrated circuit design uses established transistor compact models and passive circuit equivalents that enable predicting the circuit performance before manufacture. Those models needed to be redeveloped for cryogenic temperature operation. In a preliminary exploratory phase, individual technologies were studied at low temperatures which enabled establishing some important initial rules of thumb about transistor performance at cryogenic temperatures and allowed constructing preliminary models [116–125].

Bipolar technologies and old CMOS technologies above the 160 nm node are ruled out either because of freeze out of carriers below 4 K or because of the non-linear transistor behaviour, commonly referred to as the “kink effect”, which occurs at  $V_{ds} \geq 1.2$  V [125]. However, in general, modern CMOS technologies, both bulk silicon and fully-depleted silicon-on-insulator devices, operate at deep cryogenic temperatures although with modifications that present a weak temperature dependence below 4 K. Firstly, the threshold voltage ( $V_{th}$ ) increases because of bandgap widening, carrier density scaling, and incomplete ionization with typical enhancements of 0.1–0.2 V [126, 127]. Such shifts may compromise technologies with low supply voltage ( $V_{dd}$ ), pointing towards low  $V_{th}$  or back-gated silicon-insulator-technologies as optimal choices for deep cryogenic design. The detrimental effect of the increase in  $V_{th}$  on the on-state current,  $I_{on}$ , is partially compensated by an increase in mobility because of the reduced phonon population. Furthermore, the subthreshold swing in MOSFETs decreases because

of the reduced thermionic transport down to the level of 10 mV/dec where it saturates to a value proportional to the extent of the conduction-band tail associated with shallow defect states [128, 129]. Although this represents a substantial reduction with respect to room temperature, with the consequent potential to reduce the dynamical power dissipation, it is far from the Boltzmann limit of 0.8 mV/dec and 20  $\mu$ V/dec at 4 K and 100 mK, respectively. Furthermore, figures of merit such as on-off current ratio,  $I_{on}/I_{off}$ , and  $g_m/I_D$ , significantly improve at 4 K, aspects that are expected to enhance the performance of both digital and analogue circuits at cryogenic temperatures. In terms of passive components, quality factors improve at low temperatures [130]. However, there are also disadvantages. At low temperatures, impedance mismatch deteriorates and 1/f noise becomes more prevalent due to the reduction of the thermal noise with respect to room temperature which creates different requirements when managing noise [131–133].

These initial findings have enabled moving to the next phase of cryogenic IC design in which heuristic knowledge and advanced compact models [132, 134–136] can be used to design analog and digital circuits to meet high-level specifications. In what follows, the field needs to move on to mass-scale characterisation of transistors and circuits to generate established cryogenic compact models and electronic computer-aided design (ECAD) tools for deep cryogenic temperatures.

#### B. Power consumption and communication latency

Active quantum error-correction protocols require fast feedback between measurement and control. Utilizing a classical processing unit at room temperature to process the readout outputs and determine the gate sequences to correct for errors can be problematic. Sitting approximately 1.5 m away from the Quantum Layer, the distance imposes a minimum latency time of 30 ns which becomes comparable, for example, to two-qubit gate times mediated by the exchange interaction [67]. This situation will ultimately limit the bandwidth and pose a synchronization challenge. Cryo-electronics circuits in close proximity with the qubit layer are then desirable to reduce the impact of latency on the efficiency of QEC protocols. However, dynamic operation at cryogenic temperatures puts some tight restrictions on the power budget and presents a clear concern of up to what level co-integration may be possible. At 4 K the available cooling power is a few watts whereas at 100 mK is typically below 1 mW. Considering that transistors will have to be (dis)charged at radio or microwave frequencies to produce the control and readout signals, dynamic power dissipation is a major concern.

Recent results indicate that the operation of silicon spin qubits may be performed within error correction thresholds at elevated temperatures (1.1–1.45 K) bridging the gap between the Quantum and Cryo-electronics

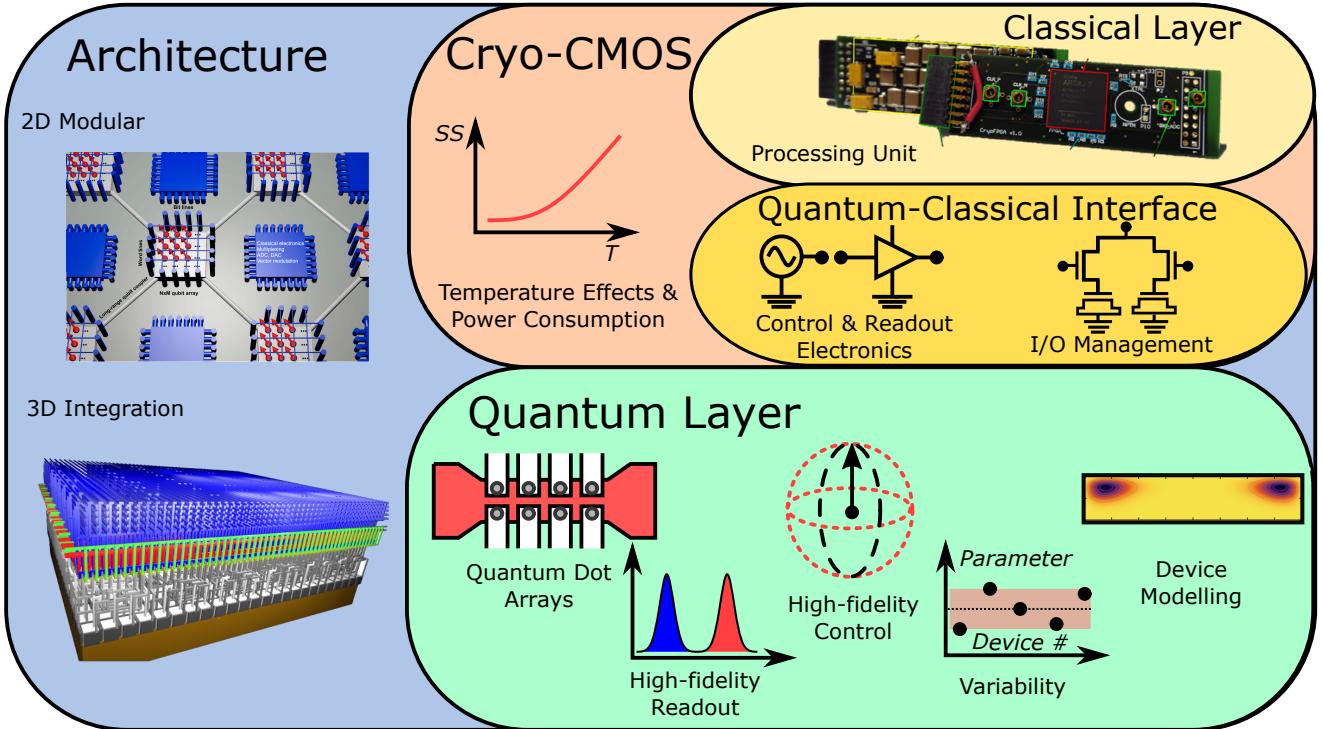


FIG. 4. Summary of the different challenges to scale silicon-based quantum computers using CMOS technology divided in to the Quantum Layer, the Quantum-Classical Interface, the Classical Layer and the Architecture. The 2D modular and 3D integrated schematic architectures are from ref. [42] and ref. [41], respectively. The photograph of the FPGA, indicated in red, in the section Classical Layer is from ref. [115]. The simulation exemplifying device modelling is from ref. [112].

by enabling a higher cooling power budget for cryo-CMOS [27, 28, 137]. It must be noted that, so far, operation at higher temperature has been achieved at the cost of reduced fidelity. QEC correction will then require a larger number of physical qubits, increasing the overall power consumption and possibly cancelling out the benefits of higher cooling power at elevated temperatures. Further research directed to overcome the deterioration of qubit performance as temperature is increased will benefit the field. Simultaneously, a new branch of IC design should emerge with the objective to deliver dynamic performance with ultra-low power consumption to meet the demanding specifications for low temperature operation.

#### IV. CHALLENGES AT THE QUANTUM-CLASSICAL INTERFACE

##### A. Signal routing (I/O management)

As opposed to classical circuits, quantum computers need to have every logic gate individually controlled by external inputs. Brute force approaches by wiring each qubit and exchange gate electrodes to room temperature electronics does not scale well as it requires macroscopic electrical wiring and extensive heat load management.

Efficiently delivering control and readout signals to increasingly more complex quantum circuits, while reducing the number of room temperature inputs per qubit, is a key challenge in developing a large-scale universal quantum computer [138, 139].

One solution is to explore shared-control approaches in which quantum dots or tunnel barriers share a common gate, mimicking the structure of CCD sensors. The approach relies on a high level of uniformity at the quantum layer and would require an improvement by approximately one order of magnitude in the variability of parameters such as the voltage range for single-electron occupancy and the tunnel coupling [43].

While advances are made on reducing variability, parallel efforts should focus on developing addressing methods that deliver independent signals to each gate with a smaller number of resources, for example row-column addressing methods as in dynamic random access memory (DRAM) and CMOS image sensors. Qubit cell matrices with row-column addressing could provide independent control over  $N$  qubits with  $O(\sqrt{N})$  room temperature resources by sacrificing simultaneous operation [41]. Memory functionality will need to be added in the form of floating capacitors to retain voltages at the relevant gates for a period much longer than the coherence time of the qubits [140, 141]. Efficient readout of such arrays could be achieved by using mixed high-frequency readout

methods combining FDMA [85] and TDMA [90].

### B. Control and readout electronics

As we have seen in Sec. II, to control and read out spin qubits, high-frequency analog signals are needed. A common feature to both is the necessity to generate IQ-modulated radio or microwave signals while additionally, for readout, reflected signals from the QPU need to be demodulated. For this purpose, a generic architecture amenable to integration is one of a radio transceiver, with the difference that it must be designed to operate at cryogenic temperatures. Fig. 2(b) shows such an architecture [142], where one can recognize the readout path, represented by multiplexers, amplifiers, demodulators, and ADCs. Typically, the voltage of the devices to be read is just a few tens of microvolts and, when using reflectometry techniques for sensing, the reflected amplitudes to be measured may even be smaller. Therefore, there is a need for amplifying the signals before demodulating them. Traditionally, this task is performed by a cryogenic high-electron-mobility low-noise amplifier (LNA), with as low as possible noise equivalent temperature ( $T_N$ ) – this figure determines the noise level of the measurement and is typically of the order of a few Kelvin. Furthermore, it requires an amplification of the order of 40 dB or more to minimise the impact of subsequent amplifying stages if placed at room temperature. Circulators are typically placed in between the QPU and the LNA to minimise interference between forward and backward travelling waves (not shown). As we have seen in Sec. II C, readout can be multiplexed in time (TDMA) and/or in frequency (FDMA). In the latter case, the bandwidth of the LNA becomes an important factor due to the need to spectrally pack several readout tones in the same channel. Thus, typically bandwidths of the order of a gigahertz or higher are desirable.. Although LNAs are typically manufactured using InP, SiGe-based amplifiers with  $T_N = 2$  K have been demonstrated and could be integrated with CMOS [143].

To reduce further the noise temperature, quantum-limited amplifiers such as the Josephson parameter amplifier (JPA) could be used in conjunction with dispersive readout sensors as the first amplifying stage [86], an approach routinely used for superconducting qubits [1]. The JPA in phase-preserving mode enables reducing the readout time by an order of magnitude with respect to conventional cryogenic amplifiers and in phase-sensitive mode could enable going beyond the quantum-limit using quadrature squeezing. For large amplification bandwidth necessary for frequency multiplexing, travelling wave amplifiers (TWPA) may be used. And for full-integration, parametric amplifiers based on the dissipationless quantum capacitance of silicon quantum dots need to be explored [91].

The control path in Fig. 2(b) shows DACs, IQ modulators and radio-frequency amplifiers aimed to assist

controlling the qubits, potentially through multiplexing. Spin control is achieved through local oscillators that are IQ modulated to create a series of carefully timed envelopes. In recent demonstrations using cryo-CMOS integrated circuits [130, 144], operation has been based on a programmable frequency, spanning from 1 to 20 GHz, so as to allow for sufficient flexibility in the type and number of qubits that can be controlled. More recently, the digital section of the control has grown substantially, to perform sophisticated modulation of  $4 \times 32$  frequencies, which are upconverted only in the last radio-frequency stage [130]. This approach could deliver the desired performance at power consumption compatible with 4 K operation for several tens of qubits simultaneously (1 mW/qubit) but would require further advancements. Furthermore, it has high flexibility in terms of signal generation, enabling a provable minimization of electrical cross-talk through spectral overlap in the control of individual qubits.

More generally, to link the impact of the control and readout electronics on qubit fidelity, a simulation framework SPINE (SPIN Emulator) [145] has been developed. SPINE enables determining the minimum set of specifications for the control and readout electronics in order not to become the bottleneck in QPU performance. It does so by linking a qubit's time evolution with the time varying signals generated by the classical electronics.

## V. CHALLENGES AT THE CLASSICAL LAYER

After the analog readout is performed, digital decoding of the qubit measurements and the formulation of a response to control them with an appropriate set of signals needs to be put in place. This poses some concrete challenges for the Classical Layer. First of all, the classical logic will need to operate significantly faster than qubits to read, identify the error, and produce the response with high fidelity. Even if the operation timescales for silicon qubits could be pushed down to 10 or 100 ns, this could still be managed with current classical processors with clock rates at 3 GHz. However, in terms of classical processor performance, error decoding at scale may pose a challenge. Assuming QEC cycles [7] in the submicrosecond regime, reading a million qubits and determining whether errors have occurred will require processing  $> 1$  Tbits/s. The most suitable processor architectures to handle the data efficiently while minimizing power consumption will need to be investigated.

Whereas low-power analog circuit design possesses some serious challenges given the stringent specifications on noise and power, digital circuits are much less problematic, due to the large noise margins allowed to operate correctly. The first circuits researchers have developed have been based on reconfigurable architectures, in particular field-programmable gate-arrays (FPGAs) [115, 125, 146]. These experiments showed that FPGAs could operate normally in deep-cryogenic temperatures

and that all the functions could be activated. Independently, several quantum error correction (QEC) algorithms have been designed and implemented in room temperature FPGAs [147]. The current trend is to combine these advances into FPGAs operated at cryogenic temperatures improving the feedback speed and reducing latency in QEC or enabling surface code decoding through machine learning techniques [148]. FPGAs will likely be used to enable fast back and forth communication in QEC but also in hybrid quantum-classical algorithms like the Variational Quantum Eigensolvers (VQE) [21] and quantum approximate optimization algorithms (QAOA) [22].

Another aspect relevant to classical logic performance at low temperature is that reduced leakage currents can make dynamic random access memories (DRAMs) essentially static, thereby enabling significant reduction in real estate utilization or alternatively in the increase of memory available to the controller. A considerable increase of memory could enable more sophisticated waveforms to counter the effects of simultaneous control of an increasing number of qubits and to enable true scalability.

Both digital and analog circuits designed for deep-cryogenic operation are still in their infancy, despite many decades of development for other applications. Thus, we believe that more solutions will be found in the future to address problems discussed above.

## VI. CHALLENGES AT THE ARCHITECTURE LEVEL

As presented in Sec. I, to build a QPU, the Quantum and Classical Layers and their interface need to be assembled in a functional manner. This raises the question of what the best system configuration is and what temperature the different function blocks should be placed at. In principle, these layers can be and are *de facto* almost independently optimised drawing on specific technical insight and following a similar methodology to other information processing systems. So far, the approach has been bottom-up, thinking of the optimal Quantum Layer and building all the way up. The established consensus at the Quantum Layer seeks long coherence times, high-fidelity short write and read times, and qubits placed in compact 2D arrays, as much as modern technology allows.

One of the big advantages of silicon in terms of scaling, its small qubit footprint, also poses some important challenges in terms of system design: The I/O problem, as we have already seen in Sec. IV A, and the location of the classical electronics with respect to the Quantum Layer. All considerations apart from that of power consumption indicate that monolithic integration would be optimal. However, if the classical electronics is co-located in the plane with the Quantum Layer, the 2D array necessary for QEC would be broken. With these requirements in mind, several architectures have been proposed with

varying levels of integration going from full 3D integration to 2D modular designs to account for limitations, leverage know-how and validate elementary designs, see Fig. 4.

Variability of the voltages used to confine the charges and to tune the coupling between adjacent dots, suggested individual gate addressing. To manage the large gate overhead researchers proposed to co-locate floating memory units with embedded control transistors (similar to 1T-1C DRAM modules) to minimise the number of I/O connections [41]. These memory units enable individual biases for each dot and exchange gate in a row/column addressed matrix but require of periodic voltage refreshing. Though indeed this architecture solves the challenge of managing local variability and the I/O problem, this pioneering work relied on very aggressive technological assumptions: short gate pitch, 3D integration of quantum and classical electronics, and the management of crosstalk between signal in the gigahertz regime, aspects that have not yet been routinely demonstrated by the semiconductor industry but will be worth tackling given that they solutions to those will have wide applications far beyond quantum computing.

An alternative monolithic 3D integrated architecture has been proposed with the focus on integrating readout on chip and providing a simpler way of initializing the qubits using two-layers: the bottom one for electrometer and reservoir definition, and the top one to encode qubits [45]. One advantage of the proposal is that enables implementing the surface code in a  $2 \times 2$  quantum dot sublattice, whereas the aforementioned design requires a  $2 \times 3$  sublattice [41], see Fig. 3(b). In any case, the architecture would equally need to handle power dissipation, crosstalk and would require of advancements on 3D integration.

Subsequent proposals simplified the architecture by moving to planar designs: the floating gate arrangement was replaced by a 2D monolithic design including three gate layers, row, column and diagonal, to control the dots and the horizontal and vertical exchange, respectively [43]. Although compatible with current technology, the architecture relies on shared control that requires a level of uniformity still to be demonstrated. To circumvent local electrostatic variations, one could think of applying large detuning energies but that could come at the expense of operation speed.

Recently, researchers proposed modular 2D sparse geometries to relax the fabrication and variability constraints [28, 42, 44]. The concept offers flexibility to accommodate the gate layouts to individually tune quantum dots and exchange interactions in local registers and introduces the concept of long-distance coupling between spatially separated registers over distances varying from microns to millimeters. Several methods for long-distance coupling exist but the most widely studied rely on CCD-inspired charge or spin shuttling [149–151] or microwave photon mediated interaction [152]. Separated qubit registers could alleviate wiring problems and free

up space to co-locate classical electronics modules. However, the fidelity of those long-distance links will be critical and will need to be at least the same as the qubits else they will rapidly become the performance bottleneck of the QPU.

More statistical data on uniformity levels will be required to determine the trade-off between technological complexity, performance, and size of the array achievable. QPU architecture design should also benefit from developments in the conventional semiconductor industry. To take one example, 5G deployment requires millimeter wave multiplexed frequencies synthesis that could be advantageously used for fast read-out of columns of qubits. From a material perspective, low-k/air gap developments for advanced CMOS nodes could also be used to lower the cross talk between adjacent RF lines and allow for compact and controllable arrays designs.

## VII. CONCLUSIONS

Silicon-based quantum computing has come a long way since the original proposals by the visionary scientists Bruce Kane, Daniel Loss and David DiVincenzo in 1998 [23, 24]. What seemed a dream at that time has now become a reality in the form of silicon-based quantum circuits realizing two-qubit processors with specifications approaching the requirements for error correction protocols. The next step is scaling and, as of today, we foresee no fundamental roadblock. However important engineering challenges lie ahead.

In this Perspectives, we have summarised those challenges that stretch beyond the engineering of high-fidelity qubits in academic laboratories and draw attention to the system-level design of a quantum computer. A perspective that includes the quantum-classical interface and the classical processing units. Silicon offers the enticing advantage that, in principle, these different layers could be manufactured using CMOS processes opening opportunities for compact system integration and low-cost manufacturing. However, some of the specifications of such a machine are beyond the capabilities of what current VLSI technology can deliver. Our target has been to highlight critical questions such as the optimal scalable qubit cell, the routing of the I/O signals and the spatial distribution of the support electronics within the QPU, and to provide directions on how these could be addressed.

A further challenge that we foresee permeates to all the different layers of the QPU. It pertains to a transi-

sition from fabrication at industrial-grade research and technology organizations to standard silicon foundries. Establishing a global Multi-Project Wafer prototyping service for silicon quantum circuits with larger flexibility in the violation of design rules could be a game changer in silicon-based quantum computing. It would enable standardization, increased fabrication throughout and improved accessibility to quantum devices and circuit and will enable reducing the timescales to the final product: A large-scale fault-tolerant quantum computer.

The realization of large-scale quantum computer will require a close synergy between researchers with expertise in the control of elementary quantum systems and specialists in systems engineering from the semiconductor industry. Equally valuable will be the promotion of specialised degrees that explore the boundaries between quantum physics and engineering to train new professionals with simultaneous expertise in Pauli matrices and Verilog-A, for example. We hope this Perspectives will help to trigger that synergy and feed the curiosity of experts from the CMOS community, quantum physics researchers, and new graduate students alike to join the exciting endeavour to build a large-scale silicon-based quantum computer.

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## AUTHOR CONTRIBUTIONS

All authors contributed to the writing of the manuscript.

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