PCB Thermal Design for a DC-DC Converter Report

SUMMARY

This report is a detailed method and findings from a project with the objectives of selecting a MOSFET transistor for a DC-DC converter and creating a PCB design that allows for the MOSFETs to dissipate heat at 5W and allow a maximum temperature increase of 40℃ from the ambient temperature of 30℃. Thermal management techniques were used to be used to optimise the design and ensure the system operates with the specified limits. This was done through calculations and custom footprints to match transistors chosen with a final output of a completed PCB board.

INTRODUCTION

The Project detailed in the report was a part of an industrial project to design and manufacture a DC-DC converter that was to be installed in an electric control system in a fuel tank. The system was to be designed with MOSFETs that dissipate heat at 5W and allow a maximum temperature increase of 40℃. Within these parameters the design is subjected to increased temperatures. With this comes the necessity for thermal management. Thermal managements are methods used to transfer and control heat generated and absorbed within a system, with the expressed purpose to ensure safe margins are maintained. Thermal management is a very important aspect of electrical design as many systems used in cars, generators, and aerospace are subjected to high temperature changes. In order to ensure these systems, operate correctly their design is, in part governed by thermal management techniques. For this project a PCB board was designed to be used as detailed above. The design used the Cadence proprietary software. Along with this these equations were used to calculate the required design within the scope of the project: (equations found in Reference (1))

Equation (1): This equation describes the thermal impedance of the junction of the integrated circuit tested with the ambient environment θ_{JA} being related to the temperature difference between the junction and the environment and power dissipation. The required thermal impedance for the DC-DC converter is therefore less than or equal to the θ_{JA} calculated

$$\theta_{JA} = \frac{T_{JUNCTION} - T_{AMBIENT}}{Power\ Dissipation} \quad (1)$$

Equation (2): This equation is used to calculate the thermal impedance of the vias (θ_{VIAS}) where length is the length of the vias and radius is the drill hole radius of the vias. This equation assumes that all vias are identical and in parallel

$$\theta_{VIAS} = \frac{\frac{1}{\lambda_{Cu}} \times Length}{(number\ of\ vias) \times \pi \times [(radius)^2 - (radius - plating\ thickness)^2]} \quad (2)$$

Equation (3): This equation is an estimate of the minimum required board area of a DC-DC converter without an exposed pad where θ_{JC} is defined as the thermal impedance of the junction to the top of the case of a package.

$$Board\ Area\ (cm^2) \geq \frac{500\ ℃ \times cm^2/\mathrm{W}}{\theta_{JA} - \theta_{JC}} \quad (3)$$

Equation (4): is an equation for calculating the thermal impedance of the copper where λ_{Cu} is the thermal conductivity of copper, length is the length of the copper plane and width is the width of the copper plane. Thickness is defined as the product of the weight of copper used in the plane and 0.0035cm.

$$\theta_{Cu} = \frac{\frac{1}{\lambda_{Cu}} \times Length}{Width \times Thickness} \quad (4)$$

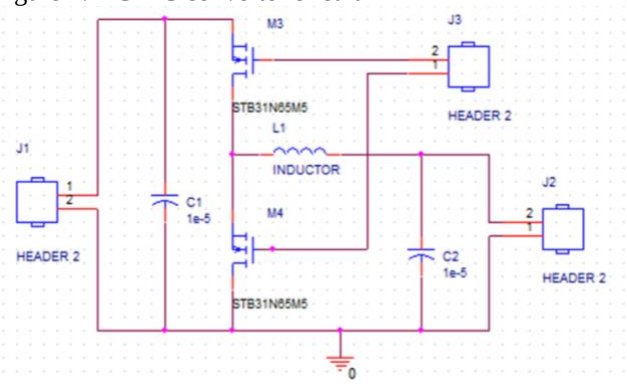
METHOD

For the project it was detailed that the PCB design should allow a maximum of a 40 degree increase in the system temperature from a 5W dissipating transistors within the DC-DC converting PCB board. To start, it was therefore essential to first select a metal-oxide-semiconductor field-effect transistor (MOSFET). Factors to be considered was θ_{JC}, Maximum Power dissipation, Operating Conditions. θ_{JC} using equation (1) the θ_{JA} is calculated giving a value of 4℃/W. With this it was estimated that a suitable transistor would have a θ_{JC} value of between 0.05 and 2.5℃/W.

With the transistor selected a DC-DC converting circuit was created. In addition, the datasheet for the selected transistor was found and the important information was recorded. For the created system footprints were applied to each component to allow netlisting to occur and imported into the PCB editor. For the footprint of the transistor to ensure optimal thermal management. A footprint was created in specification with the

datasheet using the padstack editor. In the padstack editor specific thermal via's for the thermal pads were constructed to optimise thermal transfer and ensure conformity with the maximum system value of 4℃/W. Using the dimensions of the footprint's pad and the size of thermal vias it was calculated how many vias would be required to be placed as close to the heat source to transfer the thermal energy to the heat spreader using equation (2). It was assumed that the heat spreader is covering the whole of the bottom of the PCB as this is case were the largest value thermal impedance for a heat spreader on the PCB. If at this point the system is above the threshold value of 4℃/W the transistor would be swapped for one with a lower θ_{JC}.

Figure 1: DC-DC converter circuit



From the footprint this was assigned to the transistors in the circuit in figure (1) and a DRC check was run to find any warnings or errors to resolve. After checking and correcting the relevant errors a PCB layout was constructed. To do this the board size is required, using equation (3) the minimum board area was calculated. The board shape was designed as a rectangle as this is one of the standard shapes most manufactures supply. Using this information, a value of thermal impedance could then be calculated for the copper bottom pour of the PCB (the heat spreader). Using equation (4) and a 4-layer board assumption a thermal impedance was calculated. If at this point the system is above the threshold value of 4℃/W the changes to the transistor, weight of the copper used, or size of the board would be changed. Continuing, the components can then be placed inside the outline and electrically connected to create the complete circuit from figure (1).

Finally, it was possible to add a heat sink however this is dependent on the previous values calculated above and the application/necessity. If a heat sink was chosen to be used the tool Reference (2) can be used to calculate the thermal impedance caused by the heat sink and the specifications/dimensions for construction and implementation. If a non-standard heat sink layout was chosen, then this may require the part to be costume ordered. In this case further research would be required to ensure it is producible.

RESULTS

Due to the inability to download transistor packages online, the only available parts for use in the circuit was those default packages provided in the OrCAD Capture Lite program used. From this the MBreakN3 symbol was used as an equivalent for STB31N65M5 MOSFET power transistor. With this the datasheet was found (Appendix (B)). Using this information, the Figure (1) was constructed and a value of 91cm^2 for the minimum board area. The *jumper2* footprint was assigned to the connectors, the ax1000x225034 footprint to the inductor, and the ck17-10pf to the capacitor.

The STB31N65M5 uses a DPAK TO-252AA package using the dimensions for this from Reference (3). Using these dimensions thermal pads for the signal, gate, and digital pin were constructed using Padstack Editor. Similarly, thermal vias were constructed using a 30mil diameter drill hole size with a plating thickness of 5mils. For the creation of the footprint Appendix (A) the three thermal pads where set as pins and a module was constructed and the footprint was assigned to the circuit. With the dimensions of the module defined it was calculated that 4-by-4 array in parallel of thermal vias were to be used on each transistor at the pad where the heating most occurred. The configuration gave a thermal impedance of 0.96℃/W for the total of all vias After completing the netlisting the PCB was constructed. As the minimum area of the board, assuming the path of JC to the SA is small, was found to be 140m^2 the dimensions of the outline were set to 11.9cm-by-11.9 cm. As advised in Reference (1) it was first selected that 5oz of copper be used in the pour however when calculating the thermal impedance this value gave an overall thermal of impedance of over 4℃/W. Therefore, as in the project description the area of the PCB should be as close to the minimum value previously calculated. To correct this 6 oz of copper was used and the thermal impedance was thus calculated to be 1.07℃/W. When calculated the overall value of the system is 3.94℃/W which is within the allowable range. From this the components from the netlist were placed and routed. For this solution routing was done on the top layer only.

Giving the final result of the completed board (Appendix (A). It is important to note that the vias placed by the pads are 1 mm apart from each other. This design did not include a heat sink.

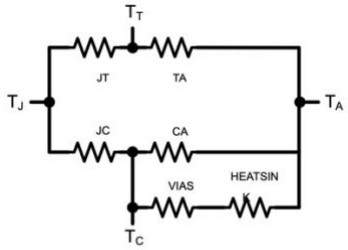
DISCUSSION

Ideally the transistor value would have been as low as possible θJC while still allowing for the proper power dissipation. When selecting the transistor the packages the transistor uses can play a big factor in the θJC as most importantly the package's surface area can help with heat dissipation. In addition, the type of mounting can be very important. For this project the transistor mounting was sought to surface mount technology (SMT) as it is a more industrial standard and allowed for the thermal pads and vias to be constructed in the ways described above. However, depending on the application of the DC-DC converter the through hole mounting's often stronger mechanical bonds and would do better in situations where the fuel tank may be attached to something that is moving and/or vibrating. Through hole however may restrict the space to create thermal vias and other structures within the board to allow for thermal management. It is because of this and the lack of application detail the often cheaper and more standard SMT was used. This choice of mounting limited the selection of transistors and led to the choice of a relatively thermal impedance junction to case.

During the design of the PCB the thermal impedances where calculated at different stages, this may have resulted in an inefficient design method. However, is still a valid method from this project further recommendations can be made on the design process. For example, calculating all thermal impedances at once before designing the PCB would allow for better manipulations of variables if required to ensure the threshold value was not exceeded.

The thermal vias dimensions were chosen as this is a standard as seen in Reference (1). They were place 1mm apart as this is standard (Reference (1)) and ensures the greatest number of vias can be placed by the heat source No heat sink was chosen as it was an unnecessary cost. However, it may be argued that using a heat sink to reduce the thermal impedance could benefit the design depending on relative budget. If this option was to be chosen it would be recommended to mount this on the bottom side of the board over the copper pour as this is the path with the least thermal resistance was seen with the package having a plastic top giving it a higher value than the path of the vias to the heat spreader. Also, all routing of the electrical components was done on the top layer, and in radial pattern from the heat sources when possible, to avoid breaks in the thermal path. The radial path lessens this affect by avoiding perpendicular traces to heat flow and there are no traces placed on the bottom layer to avoid this all together. The thermal resistance model could be represented as seen in Figure (2):

Figure (2): Thermal Resistance pathway.



From this a dominant thermal pathway from temperature at the junction and ambient temperature can be found. In the case of the designed PCB board as the path of lowest thermal resistance the dominant thermal path is through the thermal resistance of JC to the Vias and final to the heat spreader/heatsink. This was the path that was calculated to ensure safe operating temperatures/thermal management.

With the calculations it is important to note that these are only estimates. It is recommended that before manufacturing using a simulation software the PCB is tested under these thermal conditions to give a better understanding of the thermal impedances.

Conclusion

This report detailed the process taken to fully design a DC-DC converter PCB with a focus on the board's thermal management. Within the scope of the project, the PCB was designed to allow for MOSFETs to dissipate 5 W at a maximum temperature increase of 40℃ from the ambient temperature of 30℃. A transistor package was chosen and the thermal impedance of the paths within the board was calculated. The components where modified to ensure that the total of these values stayed below the threshold value of 4℃/W giving a final total of 3.94℃/W. The PCB was designed, but not fitted with a heat sink, however. further recommendations on the choice of a heat sink were included. With this the results are seen within the design, custom footprint, and board files (Appendix(A)) While all tasks set by the project were completed, the method involved was inefficient and would benefit from the recommendations detailed within the discussion.

References

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Appendix

A. The design files including, .brd, .dra, .pad and .psm files, which are needed to open your file on a second computer
B. Datasheet attached as PDF