The State University of New York at Binghamton

Department of Computer Science

CS 520 – Spring 2019

Project #2: Cache Design, Memory Hierarchy Design

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Honor Pledge: I have neither given nor received unauthorized aid on this test or assignment.

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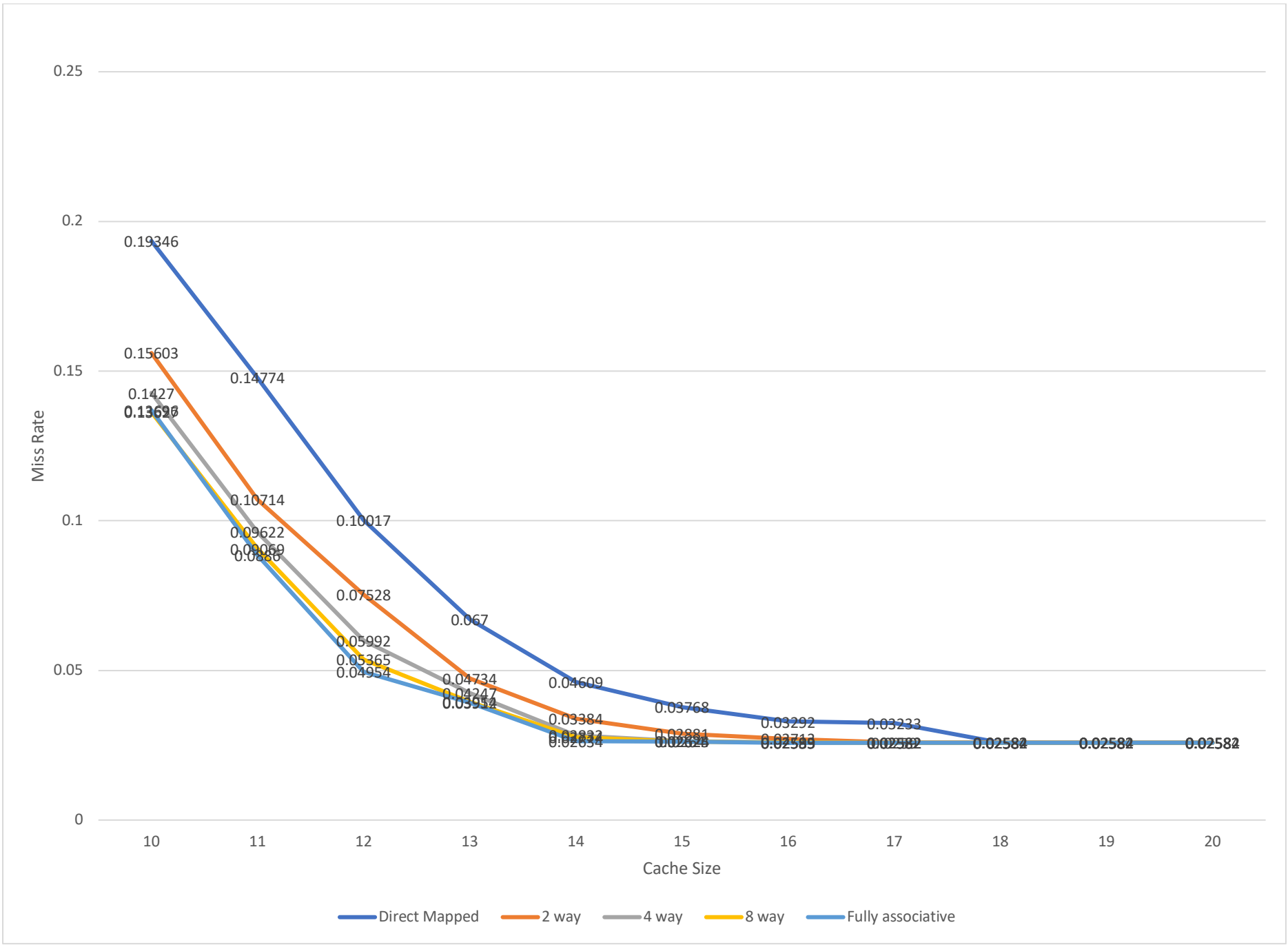
GRAPH #1

Q1. Discuss trends in the graph. For a given associativity, how does increasing cache size affect miss rate? For a given cache size, what is the effect of increasing associativity?

Cache Type	10	11	12	13	14	15	16	17	18	19	20
Direct Mapped	0.19346	0.14774	0.10017	0.067	0.04609	0.03768	0.03292	0.03233	0.02584	0.02584	0.02584
2 way	0.15603	0.10714	0.07528	0.04734	0.03384	0.02881	0.02713	0.0259	0.02584	0.02582	0.02582
4 way	0.1427	0.09622	0.05992	0.04247	0.02832	0.0264	0.02595	0.02582	0.02582	0.02582	0.02582
8 way	0.13627	0.09069	0.05365	0.03954	0.02774	0.02625	0.02589	0.02582	0.02582	0.02582	0.02582
Fully associative	0.13696	0.0886	0.04954	0.03912	0.02634	0.02624	0.02583	0.02582	0.02582	0.02582	0.02582



By observing the graph, we can conclude that as the cache size keeps increasing, the miss rates decreases exponentially. For a given associativity, if we increase the cache size then we can only compute compulsory miss rate. For a given cache size, if we increase the cache associativity then the miss rate decreases and conflict misses are removed.

Q2. Estimate the compulsory miss rate from the graph.

The compulsory miss rate is the miss rate in a large cache having full associativity. The compulsory miss rate can be estimated to be 0.02582 from the graph.

Q3. For each associativity, estimate the conflict miss rate from the graph.

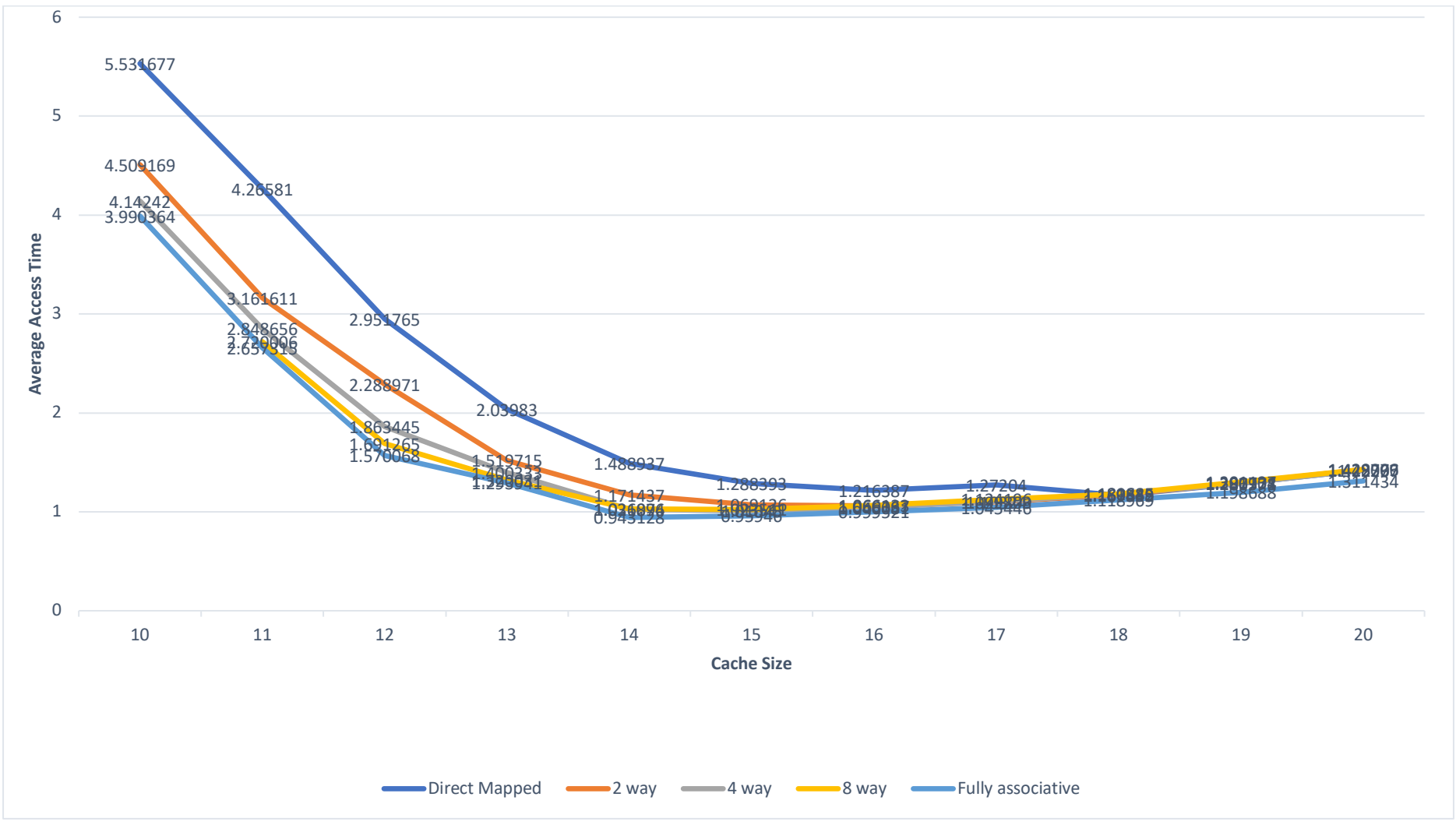
Cache Type	10	11	12	13	14	15	16	17	18	19	20
Direct Mapped	0.0565	0.05914	0.05063	0.02788	0.01975	0.01144	0.00709	0.00651	0.00002	0.00002	0.00002
2 way	0.01907	0.01854	0.02574	0.00822	0.0075	0.00257	0.0013	0.00008	0.00002	0	0
4 way	0.00574	0.00762	0.01038	0.00335	0.00198	0.00016	0.00012	0	0	0	0
8 way	0.00069	0.00209	0.00411	0.00042	0.0014	0.00001	0.00006	0	0	0	0

A fully associative graph does not have conflict misses so not values are there in the table. Conflict miss is calculated by the difference between direct mapped, 2 way, 4 way, 8 way cache and a fully associative cache.

GRAPH #2

Q1. For a memory hierarchy with only an L1 cache and BLOCKSIZE = 32, which configuration yields the best (i.e., lowest) AAT?

Cache Type	10	11	12	13	14	15	16	17	18	19	20
Direct Mapped	5.531677	4.26581	2.951765	2.03983	1.488937	1.288393	1.216387	1.27204	1.167332	1.286971	1.4229
2 way	4.509169	3.161611	2.288971	1.519715	1.171437	1.069126	1.060367	1.099803	1.169449	1.290704	1.429006
4 way	4.14242	2.848656	1.863445	1.400333	1.026896	1.01045	1.046081	1.10324	1.180645	1.287378	1.422567
8 way	-	2.720006	1.691265	1.320031	1.031074	1.023511	1.066133	1.124196	1.181885	1.301137	1.428779
Full associativity	3.990364	2.657315	1.570068	1.293941	0.943128	0.95946	0.999521	1.045446	1.118969	1.198688	1.311434



AAT (Average Access Time) is calculated by (hit time + miss rate * miss penalty). As observed from the graph, the lowest observed AAT is 0.943128 for a fully associative cache. If cache size increases, then hit time also increases and if cache size decreases then hit rate increases and miss rate decreases. Therefore, a fully associative cache with size 16KB has the best AAT.