Michael Jaggers

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OBJECTIVE

To work in a challenging electronics position where learning new tools, mastering skills, and creating new solutions is encouraged.

PROFESSIONAL EXPERIENCE

Broadcom Limited, Hardware Engineer **February 2016 - Present**

- Uses ESP-CV in equivalence checking between the TCAM model and netlist for functional verification.
- Maintains and updates the current TCAM Verilog model template across all technology nodes.
- Created a scalable verification solution for the TCAM compiler that increase ease of use in team design verification.
- Simulated the 7nm TCAM cell for essential performance metrics and comparison to previous technology cells.
- Created an Arduino ATE for use in MRAM testchip data acquisition.
- Developed new testing software in order to communicate with the Arduino and provide custom vectors to testchips.
- Coded the I2C protocol into Broadcom's custom ATE.

Broadcom Corporation, Electronic Design Engineer **December 2015 - January 2016**

- Improved Chandler's test software by recoding existing code to take advantage of existing hardware, resulting in 100x speedup in test times.
- Converted testing software from C++ to Python for posterity.
- Used perl scripts in conjunction with Finesim/HSPice to make a templatized simulation with varying conditions, PVT, and measurements.

Broadcom Corporation, Intern **July 2012 - December 2015**

- Developed test software using custom ATE hardware for the use of post-silicon verification and characterization across 40nm, 28nm, 20nm, FinFET (16nm), and 7nm technologies in SRAM and OTP designs.
- Designed, simulated, and laid-out a charge pump in 22nm FDSOI for use in OTP memory.
- Created perl scripts to post-process data for weekly presentation to the design team.
- Used Matlab to parse the results from SRAM testing to create a PDF summarizing the results from several tests.

EDUCATION

Masters of Science in Engineering, Electrical Engineering **December 2015**

Arizona State University, Tempe, AZ 3.60 GPA

Coursework -

- Computer Architecture I
- Computer Architecture II
- Advanced Computer Graphics
- Analog Integrated Circuits
- Adv Analog Integrated Circuits
- Analog to Digital Converters
- Digital Systems and Circuits
- VLSI Design
- System-Level Design for Multicore Architectures

Bachelor of Science in Engineering, Electrical Engineering **December 2014**

Arizona State University, Tempe, AZ 3.70 GPA

TECHNICAL SKILLS

Software

- Cadence Silicon Design Suite
- Cadence Encounter
- Mentor ModelSim
- Mathworks Matlab
- Xilinx Vivado Suite
- Synopsys ESP-CV
- Icarus Verilog
- Linux and Windows Environments
- Github

Programming Languages

- C/C++
- Perl
- Python
- Assembly Languages
  - MIPS, Intel Intrinsics
- SystemVerilog/Verilog/VHDL
  - OVM, UVM
- TCL
- HSpice