Michael Jaggers
253 N 87th Place
Mesa, Arizona 85207
(480) 452-4990
mgjaggers@gmail.com

HR Department
Corporation
123 Pleasant Lane
12345 City, State

September 15, 2017

Dear Sir or Madam,

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Sincerely yours,

Michael Jaggers

Attached: curriculum vitæ

Michael Jaggers

Curriculum Vitae

253 N 87th Place
Mesa, Arizona 85207
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mgjaggers@gmail.com

Education

2015–2015 **Masters of Science in Electrical Engineering**, *Arizona State University*, Tempe, *GPA – 3.6/4.0*.
Specialization: Electronics and Mix-Signal Circuit Design

2011–2014 **Bachelor of Science in Electrical Engineering**, *Arizona State University*, Tempe, *GPA – 3.7/4.0*.
Honors: Magna Cum Laude, Dean's List (all semesters)

Relevant Coursework

- Computer Architecture I & II
- Advanced Computer Graphics
- Advance Analog Integrated Circuits
- Analog to Digital Converters
- VLSI Design, Digital Systems and Circuits
- System Level Design for Multicore Architectures

Experience

2015 - 2017 **Hardware Engineer**, Broadcom Limited, Chandler, Arizona.
description
- Uses ESP-CV in equivalence checking between the TCAM model and netlist for functional verification.
- Maintains and updates the current TCAM Verilog model template across all technology nodes.
- Created a scalable verification solution for the TCAM compiler that increase ease of use in team design verification.
- Simulated the 7nm TCAM cell for essential performance metrics and comparison to previous technology cells.
- Created an Arduino ATE for use in MRAM testchip data acquisition.
- Developed new testing software in order to communicate with the Arduino and provide custom vectors to testchips.
- Coded the I2C protocol into Broadcom's custom ATE.
- Improved Chandler's test software by recoding existing code to take advantage of existing hardware, resulting in 100x speedup in test times.
- Converted testing software from C++ to Python for posterity.
- Used perl scripts in conjunction with Finesim/HSPice to make a templatized simulation with varying conditions, PVT, and measurements.

2012 - 2015 **Design Engineer Intern**, Broadcom Corporation, Chandler, Arizona.
description
- Developed test software using custom ATE hardware for the use of post-silicon verification and characterization across 40nm, 28nm, 20nm, FinFET (16nm), and 7nm technologies in SRAM and OTP designs.
- Designed, simulated, and laid-out a charge pump in 22nm FDSOI for use in OTP memory.
- Created perl scripts to post-process data for weekly presentation to the design team.
- Used Matlab to parse the results from SRAM testing to create a PDF summarizing the results from several tests.