Registros de PWM1 en el LPC1769

- ***PWM1TCR - PWM Timer Control Register***: De este registro solo se utilizan el bit 0, el bit 1 y el bit 3.

Table 448. PWM Timer Control Register (PWM1TCR address 0x4001 8004) bit description

Bit	Symbol	Value	Description	Reset Value
0	Counter Enable	1	The PWM Timer Counter and PWM Prescale Counter are enabled for counting.	0
		0	The counters are disabled.	
1	Counter Reset	1	The PWM Timer Counter and the PWM Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until this bit is returned to zero.	0
		0	Clear reset.	
2	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
3	PWM Enable	1	PWM mode is enabled (counter resets to 1). PWM mode causes the shadow registers to operate in connection with the Match registers. A program write to a Match register will not have an effect on the Match result until the corresponding bit in PWMLER has been set, followed by the occurrence of a PWM Match 0 event. Note that the PWM Match register that determines the PWM rate (PWM Match Register 0 - MR0) must be set up prior to the PWM being enabled. Otherwise a Match event will not occur to cause shadow register contents to become effective.	0
		0	Timer mode is enabled (counter resets to 0).	
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

  - ***Counter Enable***: Si coloco un 1, habilito los contadores del Timer y el Prescaler del PWM. Si coloco un 0, los deshabilito.
  - ***Counter Reset***: Si coloco un 1, se resetean ambos contadores mencionados en Counter Enable.
  - ***PWM Enable:*** Habilita el modo PWM, es decir, las salidas PWM.

- ***PWM1PR – PWM Prescale Register:***
  Se utiliza para controlar la resolución de las salidas PWM. El contador de temporizador (TC) incrementará cada ciclo de reloj periférico PWMPR + 1 (PCLK).

  Cuenta a realizar para calcular el valor a cargar al prescaler:

$$PR = (PCLK_{Hz} * PWM_{RES}) - 1$$

Donde: $PCLK_{HZ}$ es el valor del Clock seleccionado con PCLKSEL0 y podrá ser:

Table 42. Peripheral Clock Selection register bit values

PCLKSEL0 and PCLKSEL1 individual peripheral's clock select options	Function	Reset value
00	PCLK_peripheral = CCLK/4	00
01	PCLK_peripheral = CCLK	
10	PCLK_peripheral = CCLK/2	
11	PCLK_peripheral = CCLK/8, except for CAN1, CAN2, and CAN filtering when '11' selects = CCLK/6.	

y PWM_{RES} es la resolución que queremos para el PWM, puede ser, por ejemplo, 1 micro segundo → 1uS → 1.10^{-6} seg.

- ***PWM1MR0 – PWM1MR6 (Match Registers):***
  Estos son los siete registros de Match, que contienen valores de ancho de pulso, es decir, el número de marcas PWM1TC. El MR0 (Match Register 0) es el que contendrá el periodo de la señal de PWM, y del MR1 al MR6 estarán asociados a los pines de salida del PWM1.1 al PWM1.6. Por ejemplo, si quiero una señal con un cierto periodo y que este 50% en alto y 50% en bajo, lo que tengo que hacer es poner el MR0 con el valor correspondiente al periodo y en el match que me interese (por estar asociado a un pin de salida) colocar el valor del periodo dividido 2.
- ***PWM1MCR – PWM Match Control Registers:*** Se utiliza para especificar qué operaciones se pueden realizar cuando el valor en un Match particular es igual al valor en TC. Para cada registro tenemos 3 opciones: generar una interrupción, restablecer el TC o detener, que detiene los contadores y desactiva PWM. Por lo tanto, este registro se divide en un grupo de 3 bits. Los primeros 3 bits son para Match Register 0, es decir, PWMMR0, los siguientes 3 para PWMMR1, y así sucesivamente.

Table 450: Match Control Register (PWM1MCR - address 0x4001 8014) bit description

Bit	Symbol	Value	Description	Reset Value
0	PWMMR0I	1	Interrupt on PWMMR0: an interrupt is generated when PWMMR0 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
1	PWMMR0R	1	Reset on PWMMR0: the PWMTC will be reset if PWMMR0 matches it.	0
		0	This feature is disabled.	
2	PWMMR0S	1	Stop on PWMMR0: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR0 matches the PWMTC.	0
		0	This feature is disabled	
3	PWMMR1I	1	Interrupt on PWMMR1: an interrupt is generated when PWMMR1 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
4	PWMMR1R	1	Reset on PWMMR1: the PWMTC will be reset if PWMMR1 matches it.	0
		0	This feature is disabled.	
5	PWMMR1S	1	Stop on PWMMR1: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR1 matches the PWMTC.	0
		0	This feature is disabled.	
6	PWMMR2I	1	Interrupt on PWMMR2: an interrupt is generated when PWMMR2 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
7	PWMMR2R	1	Reset on PWMMR2: the PWMTC will be reset if PWMMR2 matches it.	0
		0	This feature is disabled.	

Bit	Symbol	Value	Description	Reset Value
8	PWMMR2S	1	Stop on PWMMR2: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR2 matches the PWMTC.	0
		0	This feature is disabled	
9	PWMMR3I	1	Interrupt on PWMMR3: an interrupt is generated when PWMMR3 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
10	PWMMR3R	1	Reset on PWMMR3: the PWMTC will be reset if PWMMR3 matches it.	0
		0	This feature is disabled	
11	PWMMR3S	1	Stop on PWMMR3: The PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR3 matches the PWMTC.	0
		0	This feature is disabled	
12	PWMMR4I	1	Interrupt on PWMMR4: An interrupt is generated when PWMMR4 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
13	PWMMR4R	1	Reset on PWMMR4: the PWMTC will be reset if PWMMR4 matches it.	0
		0	This feature is disabled.	
14	PWMMR4S	1	Stop on PWMMR4: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR4 matches the PWMTC.	0
		0	This feature is disabled	
15	PWMMR5I	1	Interrupt on PWMMR5: An interrupt is generated when PWMMR5 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
16	PWMMR5R	1	Reset on PWMMR5: the PWMTC will be reset if PWMMR5 matches it.	0
		0	This feature is disabled.	
17	PWMMR5S	1	Stop on PWMMR5: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR5 matches the PWMTC.	0
		0	This feature is disabled	
18	PWMMR6I	1	Interrupt on PWMMR6: an interrupt is generated when PWMMR6 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
19	PWMMR6R	1	Reset on PWMMR6: the PWMTC will be reset if PWMMR6 matches it.	0
		0	This feature is disabled.	
20	PWMMR6S	1	Stop on PWMMR6: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR6 matches the PWMTC.	0
31:21	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Se explicará con PWMMR0 pero es idéntico para los demás Match, solo cambia el bit que se debe modificar.

- ***Bit 0 – Interrupción:*** Si se coloca un 1, generará una interrupción, caso contrario se desactivará.
- ***Bit 1 – Reset:*** Si se coloca un 1, se resetea el contador de timer PWM, es decir, PWM1TC.
- ***Bit 2 – Stop(detener):*** Si se coloca un 1, tanto PWM1TC como PWM1PC se detendrán e inhabilitarán los contadores.

- ***PWM1IR – PWM Interrupt Register:*** Si cualquiera de los Match genera una interrupción, el bit correspondiente en PWM1IR se establecerá en alto. Escribir un 1 en la ubicación correspondiente eliminará esa interrupción.

Table 447: PWM Interrupt Register (PWM1IR - address 0x4001 8000) bit description

Bit	Symbol	Description	Reset Value
0	PWMMR0 Interrupt	Interrupt flag for PWM match channel 0.	0
1	PWMMR1 Interrupt	Interrupt flag for PWM match channel 1.	0
2	PWMMR2 Interrupt	Interrupt flag for PWM match channel 2.	0
3	PWMMR3 Interrupt	Interrupt flag for PWM match channel 3.	0
4	PWMCAP0 Interrupt	Interrupt flag for capture input 0	0
5	PWMCAP1 Interrupt	Interrupt flag for capture input 1.	0
7:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
8	PWMMR4 Interrupt	Interrupt flag for PWM match channel 4.	0
9	PWMMR5 Interrupt	Interrupt flag for PWM match channel 5.	0
10	PWMMR6 Interrupt	Interrupt flag for PWM match channel 6.	0
31:11	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

- ***PWMLER – Load Enable Register:*** Se utiliza para controlar la forma en que se actualizan los registros de coincidencia cuando la generación PWM está activa. Cuando el modo PWM está activo y aplicamos nuevos valores a los registros de coincidencias, los nuevos valores no se aplicarán de inmediato. En cambio, lo que sucede es que el valor se escribe en un "Registro de sombras"; puede considerarse como un Match duplicado. Cada Match tiene un registro de sombra correspondiente. El valor en este registro de sombra se transfiere al Match real cuando: PWM1TC se reinicia (es decir, al comienzo del siguiente período) y el bit correspondiente en PWM1LER es 1.

Bit	Symbol	Description	Reset Value
0	Enable PWM Match 0 Latch	Writing a one to this bit allows the last value written to the PWM Match 0 register to be become effective when the timer is next reset by a PWM Match event. See Section 24.6.4 "PWM Match Control Register (PWM1MCR - 0x4001 8014)".	0
1	Enable PWM Match 1 Latch	Writing a one to this bit allows the last value written to the PWM Match 1 register to be become effective when the timer is next reset by a PWM Match event. See Section 24.6.4 "PWM Match Control Register (PWM1MCR - 0x4001 8014)".	0
2	Enable PWM Match 2 Latch	Writing a one to this bit allows the last value written to the PWM Match 2 register to be become effective when the timer is next reset by a PWM Match event. See Section 24.6.4 "PWM Match Control Register (PWM1MCR - 0x4001 8014)".	0
3	Enable PWM Match 3 Latch	Writing a one to this bit allows the last value written to the PWM Match 3 register to be become effective when the timer is next reset by a PWM Match event. See Section 24.6.4 "PWM Match Control Register (PWM1MCR - 0x4001 8014)".	0
4	Enable PWM Match 4 Latch	Writing a one to this bit allows the last value written to the PWM Match 4 register to be become effective when the timer is next reset by a PWM Match event. See Section 24.6.4 "PWM Match Control Register (PWM1MCR - 0x4001 8014)".	0
5	Enable PWM Match 5 Latch	Writing a one to this bit allows the last value written to the PWM Match 5 register to be become effective when the timer is next reset by a PWM Match event. See Section 24.6.4 "PWM Match Control Register (PWM1MCR - 0x4001 8014)".	0
6	Enable PWM Match 6 Latch	Writing a one to this bit allows the last value written to the PWM Match 6 register to be become effective when the timer is next reset by a PWM Match event. See Section 24.6.4 "PWM Match Control Register (PWM1MCR - 0x4001 8014)".	0
31:7	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

- ***PWM1PCR – PWM Control Register:*** Este registro se utiliza para seleccionar entre salidas de Single Edged & Double Edged y también para habilitar / deshabilitar las 6 salidas PWM que van a sus pines correspondientes.

1) Single Edge PWM: El pulso comienza con un nuevo período, es decir, el pulso siempre está al principio.

2) Double Edge PWM: El pulso puede estar presente en cualquier lugar dentro del Período.

Table 452: PWM Control Register (PWM1PCR - address 0x4001 804C) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	Unused		Unused, always zero.	NA
2	PWMSEL2	1	Selects double edge controlled mode for the PWM2 output.	0
		0	Selects single edge controlled mode for PWM2.	
3	PWMSEL3	1	Selects double edge controlled mode for the PWM3 output.	0
		0	Selects single edge controlled mode for PWM3.	
4	PWMSEL4	1	Selects double edge controlled mode for the PWM4 output.	0
		0	Selects single edge controlled mode for PWM4.	
5	PWMSEL5	1	Selects double edge controlled mode for the PWM5 output.	0
		0	Selects single edge controlled mode for PWM5.	
6	PWMSEL6	1	Selects double edge controlled mode for the PWM6 output.	0
		0	Selects single edge controlled mode for PWM6.	
8:7	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Los bits 9 a 14 se utilizan para habilitar / deshabilitar las salidas PWM. Si el bit 9 se establece en 1, la salida PWM1.1 está habilitada, de lo contrario, se deshabilita si se establece en 0. De manera similar, los bits restantes para PWM1.x corresponden.

Bit	Symbol	Value	Description	Reset Value
9	PWMENA1	1	The PWM1 output enabled.	0
		0	The PWM1 output disabled.	
10	PWMENA2	1	The PWM2 output enabled.	0
		0	The PWM2 output disabled.	
11	PWMENA3	1	The PWM3 output enabled.	0
		0	The PWM3 output disabled.	
12	PWMENA4	1	The PWM4 output enabled.	0
		0	The PWM4 output disabled.	
13	PWMENA5	1	The PWM5 output enabled.	0
		0	The PWM5 output disabled.	
14	PWMENA6	1	The PWM6 output enabled.	0
		0	The PWM6 output disabled.	
31:15	Unused		Unused, always zero.	NA