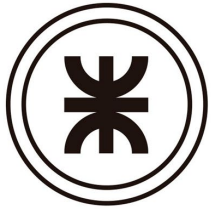

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FACULTAD REGIONAL BUENOS AIRES

Interrupciones externas (EINT)

Informática II - R2003

Ejercicio de práctica:

- Configurar dos botones como interrupciones externas que cambien un LED RGB entre verde y rojo

¿Qué pines vamos a configurar?

Revisar el manual de usuario o las hojas de ayuda para la configuración del LPC1769

Pines a utilizar (PINSEL)

Colocar función 1

- P2.10
- P2.11
- P2.12
- P2.13

8.5.5 Pin Function Select Register 4 (PINSEL4 - 0x4002 C010)

The PINSEL4 register controls the functions of the lower half of Port 2. The direction control bit in the FIO2DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 84. Pin function select register 4 (PINSEL4 - address 0x4002 C010) bit description

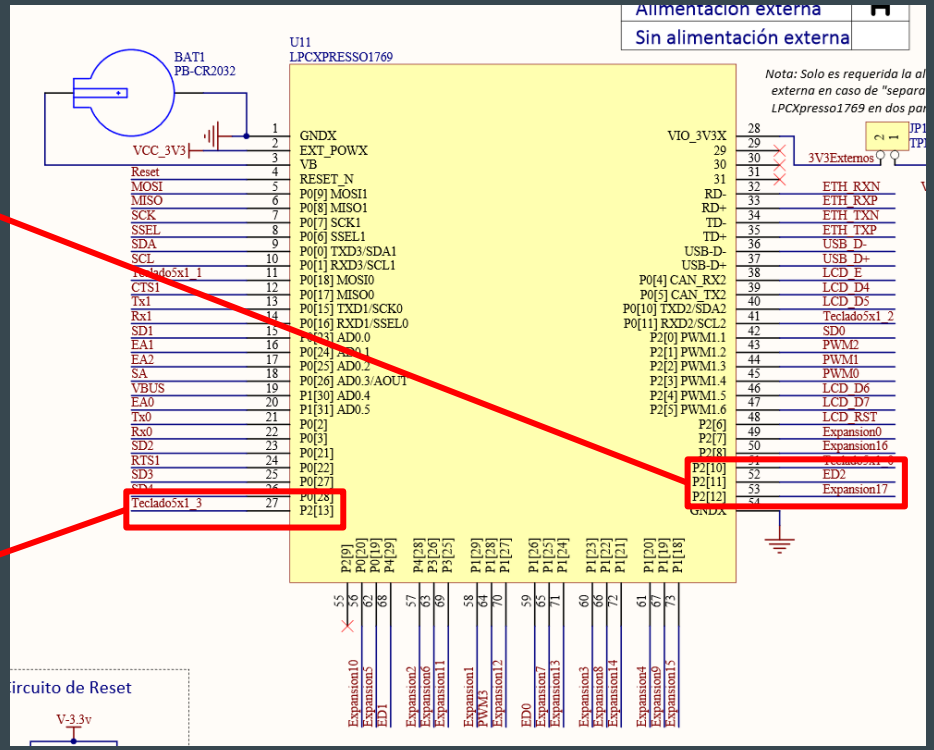
PINSEL4	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P2.0	GPIO Port 2.0	PWM1.1	TXD1	Reserved	00
3:2	P2.1	GPIO Port 2.1	PWM1.2	RXD1	Reserved	00
5:4	P2.2	GPIO Port 2.2	PWM1.3	CTS1	Reserved [2]	00
7:6	P2.3	GPIO Port 2.3	PWM1.4	DCD1	Reserved [2]	00
9:8	P2.4	GPIO Port 2.4	PWM1.5	DSR1	Reserved [2]	00
11:10	P2.5	GPIO Port 2.5	PWM1.6	DTR1	Reserved [2]	00
13:12	P2.6	GPIO Port 2.6	PCAP1.0	RI1	Reserved [2]	00
15:14	P2.7	GPIO Port 2.7	RD2	RTS1	Reserved	00
17:16	P2.8	GPIO Port 2.8	TD2	TXD2	ENET_MDC	00
19:18	P2.9	GPIO Port 2.9	USB_CONNECT	RXD2	ENET_MDIO	00
21:20	P2.10	GPIO Port 2.10	$\overline{\text{EINT0}}$	NMI	Reserved	00
23:22	P2.11 [1]	GPIO Port 2.11	$\overline{\text{EINT1}}$	Reserved	I2STX_CLK	00
25:24	P2.12 [1]	GPIO Port 2.12	$\overline{\text{EINT2}}$	Reserved	I2STX_WS	00
27:26	P2.13 [1]	GPIO Port 2.13	$\overline{\text{EINT3}}$	Reserved	I2STX_SDA	00
31:28	-	Reserved	Reserved	Reserved	Reserved	0

Registros PINSEL (*Pin function select register*): Manual → Capítulo 8 (Pin Connect Block) → Página 120

Ubicando pines en el Infotronic

P2[10]	51	Teclado5x1_0
P2[11]	52	ED2
P2[12]	53	Expansion17
	54	

Teclado5x1_3	27	P2[13]

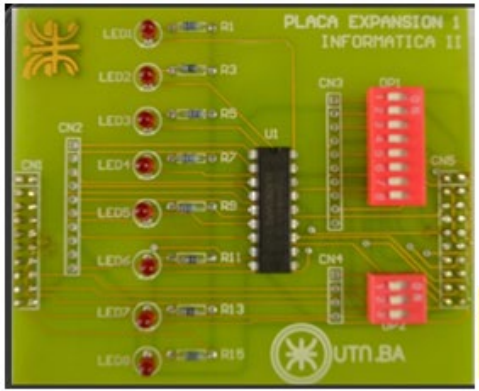


PlacaBaseInfotronic V1.02Esquemáticos y Circuito Impreso.pdf → *Página 4*

Interrupciones externas conectadas a pulsadores

Interrupción EXTERNA	Puerto	Infotronic	Función
EINT0	P210	SW1	KEY0
EINT1	P211	ENT.DIG2	BORNERA
EINT2	P212	EXPANSION 17	DIP2_2
EINT3	P213	SW10	KEY3

KEY4 P126 | **KEY3 P213 EINT3** | **KEY2 P011** | **KEY1 P018** | **KEY0 P210 EINT0**



DIP2-2 P212 EINT0

Registros involucrados en EINT

3.3 Register description

All registers, regardless of size, are on word address boundaries. Details of the registers appear in the description of each function.

Table 7. Summary of system control registers

Name	Description	Access	Reset value	Address
External Interrupts				
EXTINT	External Interrupt Flag Register	R/W	0	0x400F C140
EXTMODE	External Interrupt Mode register	R/W	0	0x400F C148
EXTPOLAR	External Interrupt Polarity Register	R/W	0	0x400F C14C

Manual → Capítulo 3 (System Control) → Página 20

Descripción de los registros

Register description

The external interrupt function has four registers associated with it. The EXTINT register contains the interrupt flags. The EXTMODE and EXTPOLAR registers specify the level and edge sensitivity parameters.

Table 9. External Interrupt registers

Name	Description	Access	Reset value[1]	Address
EXTINT	The External Interrupt Flag Register contains interrupt flags for EINT0, EINT1, EINT2 and EINT3. See Table 10.	R/W	0x00	0x400F C140
EXTMODE	The External Interrupt Mode Register controls whether each pin is edge- or level-sensitive. See Table 11.	R/W	0x00	0x400F C148
EXTPOLAR	The External Interrupt Polarity Register controls which level or edge on each pin will cause an interrupt. See Table 12.	R/W	0x00	0x400F C14C

Flags de interrupción

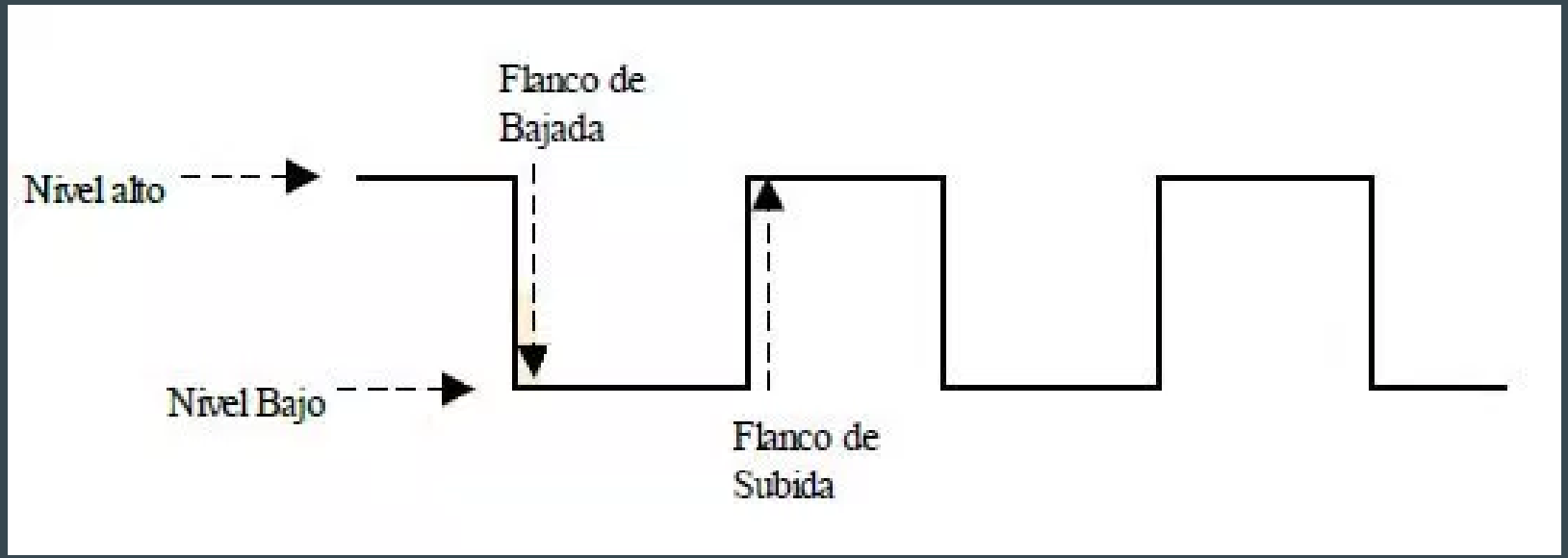
Configuración

Nivel ó Flanco

Alto ó Bajo

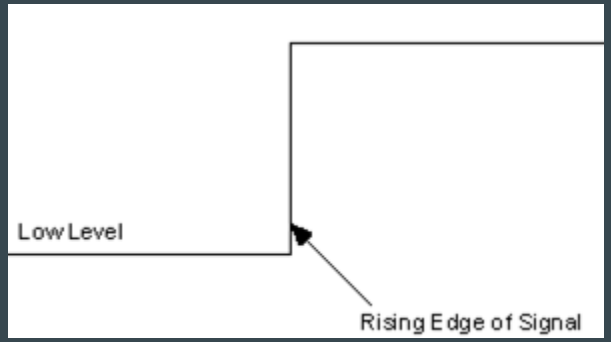
Manual → Capítulo 3 (System Control) → Página 26

Modos de funcionamiento

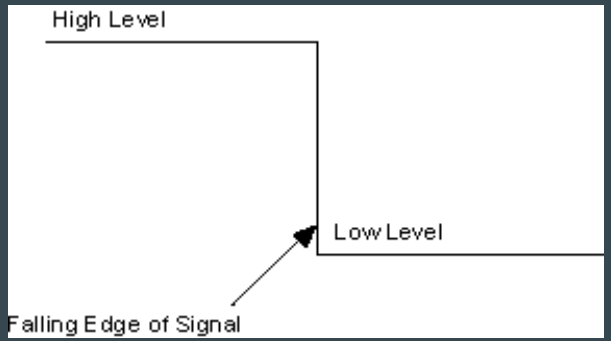


Configuración para el ejemplo

- EINT0 como flanco ascendente



- EINT3 como flanco descendente



Configuración EINT (EXTMO

3.6.3 External Interrupt Mode register (EXTMODE - 0x400F C148)

The bits in this register select whether each EINT pin is level- or edge-sensitive. Only pins that are selected for the EINT function (see Section 8.5) and enabled in the appropriate NVIC register) can cause interrupts from the External Interrupt function (though of course pins selected for other functions may cause interrupts from those functions).

Note: Software should only change a bit in this register when its interrupt is disabled in the NVIC (state readable in the ISERn/ICERn registers), and should write the corresponding 1 to EXTINT before enabling (initializing) or re-enabling the interrupt. An extraneous interrupt(s) could be set by changing the mode and not having the EXTINT cleared.

Table 11. External Interrupt Mode register (EXTMODE - address 0x400F C148) bit description

Bit	Symbol	Value	Description	Reset value
0	EXTMODE0	0	Level-sensitivity is selected for $\overline{\text{EINT0}}$.	0
		1	EINT0 is edge sensitive.	
1	EXTMODE1	0	Level-sensitivity is selected for $\overline{\text{EINT1}}$.	0
		1	$\overline{\text{EINT1}}$ is edge sensitive.	
2	EXTMODE2	0	Level-sensitivity is selected for $\overline{\text{EINT2}}$.	0
		1	$\overline{\text{EINT2}}$ is edge sensitive.	
3	EXTMODE3	0	Level-sensitivity is selected for $\overline{\text{EINT3}}$.	0
		1	$\overline{\text{EINT3}}$ is edge sensitive.	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

b31	b30	b29	b28	b27	b26	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	1	X	X	1

Registro EXTMODE *(EINT Mode Register).* Manual → Capítulo 3 (System Control) → Páginas 27/28

Configuración EINT (EXTPOLAR)

Table 12. External Interrupt Polarity register (EXTPOLAR - address 0x400F C14C) bit description

Bit	Symbol	Value	Description	Reset value
0	EXTPOLAR0	0	$\overline{EINT0}$ is low-active or falling-edge sensitive (depending on EXTMODE0).	0
		1	$\overline{EINT0}$ is high-active or rising-edge sensitive (depending on EXTMODE0).	
1	EXTPOLAR1	0	$\overline{EINT1}$ is low-active or falling-edge sensitive (depending on EXTMODE1).	0
		1	$\overline{EINT1}$ is high-active or rising-edge sensitive (depending on EXTMODE1).	
2	EXTPOLAR2	0	$\overline{EINT2}$ is low-active or falling-edge sensitive (depending on EXTMODE2).	0
		1	$\overline{EINT2}$ is high-active or rising-edge sensitive (depending on EXTMODE2).	
3	EXTPOLAR3	0	$\overline{EINT3}$ is low-active or falling-edge sensitive (depending on EXTMODE3).	0
		1	$\overline{EINT3}$ is high-active or rising-edge sensitive (depending on EXTMODE3).	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Registro EXTPOLAR*(EINT Polarity Register).* Manual → Capítulo 3 (System Control) → Páginas 28/29

Configuración del NVIC

- ISER → Habilitar interrupciones genera

17	ISE_RTC	Real Time Clock (RTC) Interrupt Enable. See functional description for bit 0.
18	ISE_EINT0	External Interrupt 0 Interrupt Enable. See functional description for bit 0.
19	ISE_EINT1	External Interrupt 1 Interrupt Enable. See functional description for bit 0.
20	ISE_EINT2	External Interrupt 2 Interrupt Enable. See functional description for bit 0.
21	ISE_EINT3	External Interrupt 3 Interrupt Enable. See functional description for bit 0.
22	ISE_ADC	ADC Interrupt Enable. See functional description for bit 0.
23	ISE_BOD	BOD Interrupt Enable. See functional description for bit 0.
24	ISE_USB	USB Interrupt Enable. See functional description for bit 0.
25	ISE_CAN	CAN Interrupt Enable. See functional description for bit 0.
26	ISE_DMA	GPDMA Interrupt Enable. See functional description for bit 0.
27	ISE_I2S	I^2S Interrupt Enable. See functional description for bit 0.
28	ISE_ENET	Ethernet Interrupt Enable. See functional description for bit 0.
29	ISE_RIT	Repetitive Interrupt Timer Interrupt Enable. See functional description for bit 0.
30	ISE_MCPWM	Motor Control PWM Interrupt Enable. See functional description for bit 0.
31	ISE_QEI	Quadrature Encoder Interface Interrupt Enable. See functional description for bit 0.

6.5.1 Interrupt Set-Enable Register 0 register (ISER0 - 0xE000 E100)

The ISER0 register allows enabling the first 32 peripheral interrupts, or for reading the enabled state of those interrupts. The remaining interrupts are enabled via the ISER1 register (Section 6.5.2). Disabling interrupts is done through the ICER0 and ICER1 registers (Section 6.5.3 and Section 6.5.4).

Table 52. Interrupt Set-Enable Register 0 register (ISER0 - 0xE000 E100)

Bit	Name	Function
0	ISE_WDT	Watchdog Timer Interrupt Enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.
1	ISE_TIMER0	Timer 0 Interrupt Enable. See functional description for bit 0.
2	ISE_TIMER1	Timer 1. Interrupt Enable. See functional description for bit 0.
3	ISE_TIMER2	Timer 2 Interrupt Enable. See functional description for bit 0.
4	ISE_TIMER3	Timer 3 Interrupt Enable. See functional description for bit 0.
5	ISE_UART0	UART0 Interrupt Enable. See functional description for bit 0.
6	ISE_UART1	UART1 Interrupt Enable. See functional description for bit 0.
7	ISE_UART2	UART2 Interrupt Enable. See functional description for bit 0.
8	ISE_UART3	UART3 Interrupt Enable. See functional description for bit 0.
9	ISE_PWM	PWM1 Interrupt Enable. See functional description for bit 0.
10	ISE_I2C0	I^2C0 Interrupt Enable. See functional description for bit 0.
11	ISE_I2C1	I^2C1 Interrupt Enable. See functional description for bit 0.
12	ISE_I2C2	I^2C2 Interrupt Enable. See functional description for bit 0.
13	ISE_SPI	SPI Interrupt Enable. See functional description for bit 0.
14	ISE_SSP0	SSP0 Interrupt Enable. See functional description for bit 0.
15	ISE_SSP1	SSP1 Interrupt Enable. See functional description for bit 0.
16	ISE_PLL0	PLL0 (Main PLL) Interrupt Enable. See functional description for bit 0.

b31	b30	b29	b22	b21	b20	b19	b18	b2	b1	b0
X	X	X	X	1	X	X	1	X	X	X

Registros ISER (*Interrupt Set-Enable Register*).

Manual → Capítulo 6 (NVIC) →

Configuración en código del EINT

```
void Init_IntExt(void)
{
    // P2.13 como EINT3
    // configuro el pin con función de interrupción externa
    SetPINSEL(P2, 13, INT_EXT);
    // P2.10 como EINT0
    // configuro el pin con función de interrupción externa
    SetPINSEL(P2, 10, INT_EXT);
```

Ahora vemos este bloque de código

```
    // Configuro a EINT0 por FLANCO
    EXTMODE |= 0x01 << 0;
    // Configuro a EINT3 por FLANCO
    EXTMODE |= 0x01 << 3;
    // Configuro a EINT0 sensible en flanco ASCENDENTE
    //Registro | 1 --> Pone en 1 el bit 0 dejando al resto como estaba
    EXTPOLAR |= 0x01 << 0;
    // Configuro a EINT3 sensible en flanco DESCENDENTE
    //Registro & 111...110111 --> Pone en 0 el bit 3  dejando al resto como estaba
    EXTPOLAR &= ~(0x01 << 3);

    // Habilito las int. externas
    ISER0 |= 0x01 << 18; // EINT0
    ISER0 |= 0x01 << 21; // EINT3
}
```

```
#define     EXTINT_     ( ( __RW uint32_t  * ) 0x400FC140UL )
#define     EXTINT      EXTINT_[0]

#define     EXTMODE_    ( ( __RW uint32_t  * ) 0x400FC148UL )
#define     EXTMODE     EXTMODE_[0]

#define     EXTPOLAR_   ( ( __RW uint32_t  * ) 0x400FC14CUL )
#define     EXTPOLAR    EXTPOLAR_[0]

#define     INT_EXT     1

#define     ISER        ( ( __RW uint32_t  * ) 0xE000E100UL )
#define     ISER0       ISER[0]
#define     ISER1       ISER[1]
```

Configuración en código de GPIOs

```
void Init_GPIOs(void)
{

    SetPINSEL ( RGB_BLUE , PINSEL_GPIO);
    SetPINSEL ( RGB_RED , PINSEL_GPIO);
    SetPINSEL ( RGB_GREEN , PINSEL_GPIO);

    SetDIR ( RGB_BLUE , SALIDA);
    SetDIR ( RGB_RED, SALIDA);
    SetDIR ( RGB_GREEN , SALIDA);
}
```

```
#define     SALIDA      1
#define     PINSEL_GPIO 0

#define     RGB_BLUE    2,1
#define     RGB_RED     2,2
#define     RGB_GREEN   2,3
```

La magia de las interrupciones:

```
int main(void)
{
    init();

    while(1) {

    }

    return 0 ;
}
```

Funcionamiento en las rutinas de atención de interrupción (ISR)

Atención de interrupción (EXTINT)

Table 10. External Interrupt Flag register (EXTINT - address 0x400F C140) bit description

Bit	Symbol	Description	Reset value
0	EINT0	In level-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
1	EINT1	In level-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
2	EINT2	In level-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
3	EINT3	In level-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

[1] Example: e.g. if the EINTx is selected to be low level sensitive and low level is present on corresponding pin, this bit can not be cleared; this bit can be cleared only when signal on the pin becomes high.

3.6.2 External Interrupt flag register (EXTINT - 0x400F C140)

When a pin is selected for its external interrupt function, the level or edge on that pin (selected by its bits in the EXTPOLAR and EXTMODE registers) will set its interrupt flag in this register. This asserts the corresponding interrupt request to the NVIC, which will cause an interrupt if interrupts from the pin are enabled.

Writing ones to bits EINT0 through EINT3 in EXTINT register clears the corresponding bits. In level-sensitive mode the interrupt is cleared only when the pin is in its inactive state.

Important: whenever a change of external interrupt operating mode (i.e. active level/edge) is performed (including the initialization of an external interrupt), the corresponding bit in the EXTINT register must be cleared! For details see Section 3.6.3 "External Interrupt Mode register (EXTMODE - 0x400F C148)" and Section 3.6.4 "External Interrupt Polarity register (EXTPOLAR - 0x400F C14C)".

Registro EXTINT *(EINT Flag Register).*

Manual → Capítulo 3 (System Control) → Páginas 26/27

Código atendiendo interrupción

```
void EINT0_IRQHandler(void)
{
    EXTINT |= 0x1 << 0; // Limpio el flag de la EINT0 escribiendo un UNO.

    SetPIN(PORT2, 2, 1); // Prendo el led rojo
    SetPIN(PORT2, 3, 0); // Apago el led verde
}

void EINT3_IRQHandler(void)
{
    EXTINT |= 0x1 << 3; // Limpio el flag de la EINT3 escribiendo un UNO.

    SetPIN(PORT2, 2, 0); // Apago el led rojo
    SetPIN(PORT2, 3, 1); // Prendo el led verde
}
```

Código de inicialización

```
void Init_IntExt(void)
{
    // P2.13 como EINT3
    // configuro el pin con función de interrupción externa
    SetPINSEL(P2, 13, INT_EXT);
    // P2.10 como EINT0
    // configuro el pin con función de interrupción externa
    SetPINSEL(P2, 10, INT_EXT);

    //Limpio flags como inicialización
    EXTINT |= 0x1 << 0; // Limpio el flag de la EINT0 escribiendo un UNO.
    EXTINT |= 0x1 << 3; // Limpio el flag de la EINT3 escribiendo un UNO.

    // Configuro a EINT0 por FLANCO
    EXTMODE |= 0x01 << 0;
    // Configuro a EINT3 por FLANCO
    EXTMODE |= 0x01 << 3;
    // Configuro a EINT0 sensible en flanco ASCENDENTE
    //Registro | 1 --> Pone en 1 el bit 0 dejando al resto como estaba
    EXTPOLAR |= 0x01 << 0;
    // Configuro a EINT3 sensible en flanco DESCENDENTE
    //Registro & 111...110111 --> Pone en 0 el bit 3  dejando al resto como estaba
    EXTPOLAR &= ~(0x01 << 3);

    // Habilito las int. externas
    ISER0 |= 0x01 << 18; // EINT0
    ISER0 |= 0x01 << 21; // EINT3
}
```