Field	Description of fields within Sub-Register 0x24:08 EC_GOLP
OFFSET_EXT reg:24:08 bits: 5:0	This register contains the 1 GHz count from the arrival of the RMARKER and the next edge of the external clock. See section *6.1.3 – One Shot Receive Synchronisation (OSRS) Mode* for details of its use.

7.2.38 Register file: 0x25 – Accumulator CIR memory

ID	Length (octets)	Type	Mnemonic	Description
0x25	4064	RO	ACC_MEM	Read access to accumulator data memory

Register map register file 0x25 is a large bank of memory that holds the accumulated channel impulse response (CIR) data. To accurately determine this timestamp the DW1000 incorporates an internal (LDE) algorithm to adjust the RMARKER receive timestamp as reported in Register file: 0x15 – Receive Time Stamp. A main component of the LDE algorithm is a search of the channel impulse response in the ACC_MEM to find the "leading edge" defining the first arriving ray.

The host system does not need to access the ACC_MEM in normal operation, however it may be of interest to the system design engineers to visualise the radio channel for diagnostic purposes.

The accumulator contains complex values, a 16-bit real integer and a 16-bit imaginary integer, for each tap of the accumulator, each of which represents a 1 ns sample interval (or more precisely half a period of the 499.2 MHz fundamental frequency). The span of the accumulator is one symbol time. This is 992 samples for the nominal 16 MHz mean PRF, or, 1016 samples for the nominal 64 MHz mean PRF. These numbers are calculated from Table 58 given that there are two samples per chip time.

NB: Because of an internal memory access delay when reading the accumulator the first octet output is a dummy octet that should be discarded. This is true no matter what sub-index the read begins at.

Sub-Index	Field	Description of fields within Register file: 0x25 – Accumulator CIR memory
0 reg:25:000	CIR[0].real.lo8	Low 8 bits of real part of accumulator sample 0
1 reg:25:001	CIR[0].real.hi8	High 8 bits of real part of accumulator sample 0
2 reg:25:002	CIR[0].imag.lo8	Low 8 bits of imaginary part of accumulator sample 0
3 reg:25:003	CIR[0].imag.lo8	High 8 bits of imaginary part of accumulator sample 0
4 reg:25:004	CIR[1].real.lo8	Low 8 bits of real part of accumulator sample 1
5 reg:25:005	CIR[1].real.hi8	High 8 bits of real part of accumulator sample 1
6 reg:25:006	CIR[1].imag.lo8	Low 8 bits of imaginary part of accumulator sample 1
7 reg:25:007	CIR[1].imag.lo8	High 8 bits of imaginary part of accumulator sample 1
: :	: :	: :
4060 reg:25:FDC	CIR[1015].real.lo8	Low 8 bits of real part of accumulator sample 1015 (1016th and last sample of CIR for the nominal 64 MHz mean PRF)

Sub-Index	Field	Description of fields within Register file: 0x25 – Accumulator CIR memory
4061 reg:25:FDD	CIR[1015].real.hi8	High 8 bits of real part of accumulator sample 1015 (1016th and last sample of CIR for the nominal 64 MHz mean PRF)
4062 reg:25:FDE	CIR[1015].imag.lo8	Low 8 bits of imaginary part of accumulator sample 1015 (1016th and last sample of CIR for the nominal 64 MHz mean PRF)
4063 reg:25:FDF	CIR[1015].imag.lo8	High 8 bits of imaginary part of accumulator sample 1015 (1016th and last sample of CIR for the nominal 64 MHz mean PRF)

NB: Because of an internal memory access delay when reading the accumulator the first octet output is a dummy octet that should be discarded. This is true no matter what sub-index the read begins at.

7.2.39 Register file: 0x26 – GPIO control and status

ID	Length (octets)	Type	Mnemonic	Description
0x26	44	RW	GPIO_CTRL	Peripheral register bus 1 access - GPIO control

Register map register file 0x26 is concerned with the use of the GPIO. It contains a number of sub-registers. An overview of these is given by Table 27. Each of these sub-registers is separately described in the sub-sections below.

Table 27: Register file: 0x26 – GPIO control and status overview

OFFSET in Register 0x26	Mnemonic	Description
0x00	GPIO_MODE	GPIO Mode Control Register
0x04	-	reserved
0x08	GPIO_DIR	GPIO Direction Control Register
0x0C	GPIO_DOUT	GPIO Data Output register
0x10	GPIO_IRQE	GPIO Interrupt Enable
0x14	GPIO_ISEN	GPIO Interrupt Sense Selection
0x18	GPIO_IMODE	GPIO Interrupt Mode (Level / Edge)
0x1C	GPIO_IBES	GPIO Interrupt “Both Edge” Select
0x20	GPIO_ICLR	GPIO Interrupt Latch Clear
0x24	GPIO_IDBE	GPIO Interrupt De-bounce Enable
0x28	GPIO_RAW	GPIO raw state

7.2.39.1 Sub-Register 0x26:00 – GPIO_MODE

ID	Length (octets)	Type	Mnemonic	Description
26:00	4	RW	GPIO_MODE	GPIO Mode Control Register

Register file: 0x26 – GPIO control and status, sub-register 0x00 is the GPIO Mode Control Register, GPIO_MODE. The GPIO_MODE register is used to select whether the GPIO is operating as a GPIO or has another special function. The GPIO_MODE register contains the following sub-fields: