<html class="gr__faculty_cs_niu_edu"><head></head><body data-gr-c-s-loaded="true"><pre
style="word-wrap: break-word; white-space: pre-wrap;">Final Spring 2017 Name

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Name the signal protocol that uses one voltage level to represent a one and another to represent a zero.

Name the signal protocol that uses a change in voltage level to represent a one and a lack of change in a given time period to represent a zero.

Name the signal protocol that uses two different frequencies to represent the 2 different values, zero and one.

Name the signal protocol that uses a sharp change in the carrier's wave form to represent a one.

Name the signal protocol that imposed the data on a clock signal. A one is transmitted when the carrier transistion is low to high or stays high and a zero when transition is high to low or stays low.

Name the signal protocol that imposed the data on a clock signal. If the next bit is a one, there is not transition in signal level at the end of the current clock cycle. If the next bit is zero, there is a transition in the signal level at the end of the current clock cycle.

Name the technique that encodes a series of sequential bits in a select longer sequence of bits so that the number of sequential zeros is limited.

Buses True/false

T/F GPIB interface bus uses packet based communication.

T/F Legacy system bus, ISA/EISA, uses packet based communication.

T/F PCI expansion bus uses packet based communication.

T/F PCI-e expansion bus uses packet based communication.

T/F USB2 bus uses packet based communication.

T/F GPIB, general purpose interface bus uses NRZ signaling.

T/F Legacy system bus, ISA/EISA, uses NRZ signaling.

T/F PCI expansion bus uses uses NRZ signaling.

T/F PCI-e expansion bus uses NRZ signaling.

T/F USB2 bus uses NRZ signaling.

T/F GPIB general purpose interface bus supports burst mode transactions.

T/F Legacy system bus, ISA/EISA, supports burst mode transactions.

T/F PCI expansion bus supports burst mode transactions.

T/F PCI-e expansion bus supports burst mode transactions.

T/F USB2 bus supports burst mode transactions.

T/F GPIB general purpose interface bus uses RLL encoding.

T/F Legacy system bus, ISA/EISA, uses RLL encoding.

T/F PCI expansion bus uses RLL encoding.

T/F PCI-e expansion bus uses RLL encoding.

T/F USB2 bus uses RLL encoding.

T/F GPIB general purpose interface bus supports bus mastering.

T/F Legacy system bus, ISA/EISA, supports bus mastering.

T/F PCI expansion bus supports bus mastering.

T/F PCI-e expansion bus supports bus mastering.

T/F USB2 bus supports bus mastering.

T/F GPIB general purpose interface bus supports polled interrupts.

T/F Legacy system bus, ISA/EISA, supports polled interrupts.

T/F PCI expansion bus supports polled interrupts.

T/F PCI-e expansion bus supports polled interrupts.

T/F USB bus supports polled interrupts.

T/F GPIB general purpose interface bus multiplexes both address and data over same lines.

T/F Legacy system bus, ISA/EISA, multiplexes both address and data over same lines.

T/F PCI expansion bus multiplexes both address and data over same lines.

T/F PCI-e expansion bus multiplexes both address and data over same lines.

T/F USB bus multiplexes both address and data over same lines.
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