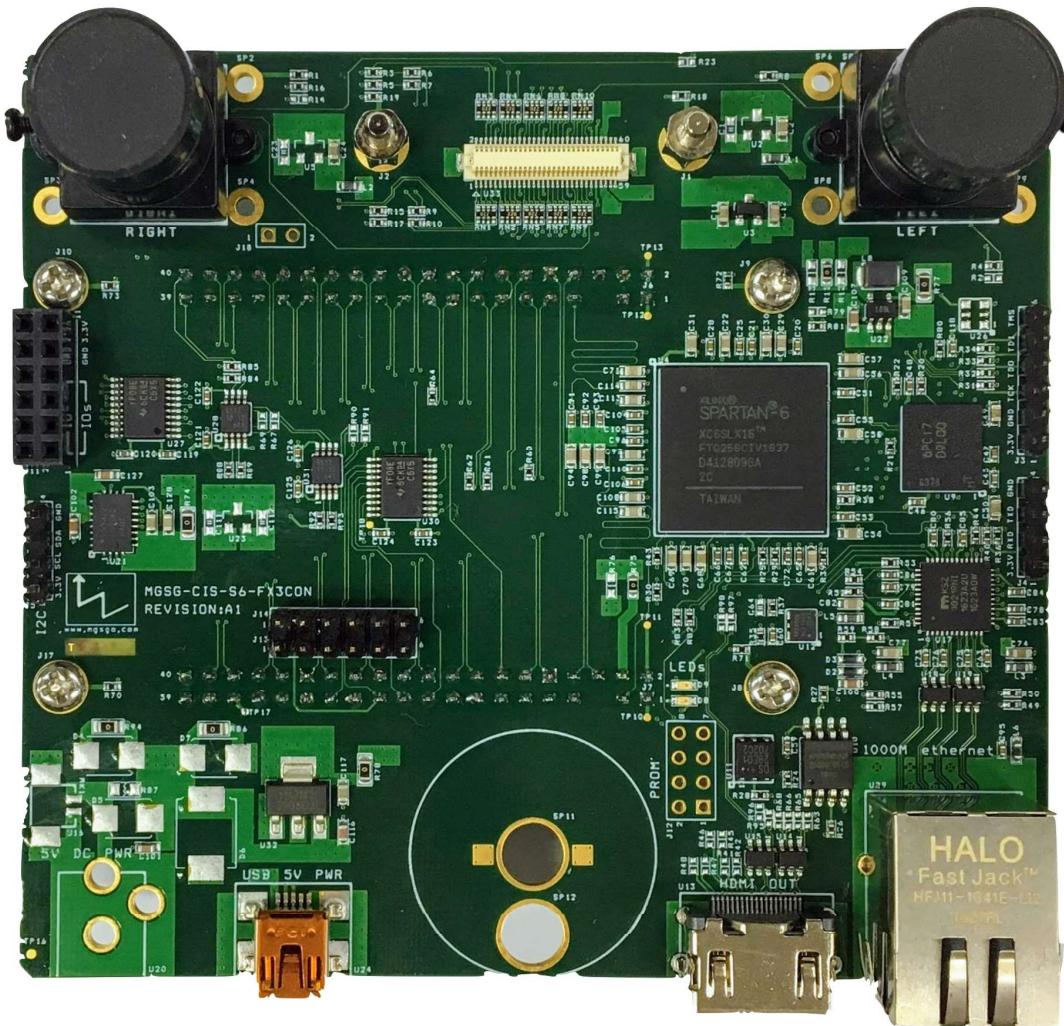


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## M-CIS-S6-FX3CON USER MANUAL



# M-CIS-S6-FX3CON user manual ENG

REVISION 1.0.0

MGSG CO., LTD

## Revision history

Revision	Date	Description	Update by
1.0.0	2019.02.23	Initial creation	jhyoo
	2019.04.27	Update	jhyoo

## Table of Contents

- 1. Package**
- 2. Overview**
- 3. Examples**
- 4. Support**

## 1. Package

### 1.1 Package contents



- 2.54mm jumper 6EA
- Tripod and nut
- PCB board
- USB power cable(USB A to USB mini B)
- Not included CYUSB3KIT-003 board.
- Not included Xilinx JTAG cable

Figure 1.1.1 M-CIS-S6-FX3CON package and contents

## 1.2 Tripod and but assembly



Figure 1.2.1 M-CIS-S6-FX3CON assembled tripod

## 2. Overview

The M-CIS-S6-FX3CON is a FPGA development board for image sensor, USB3.0, Gigabit ethernet,HDMI. It provides various examples and can also be used for image processing.

### 2.1 Layout

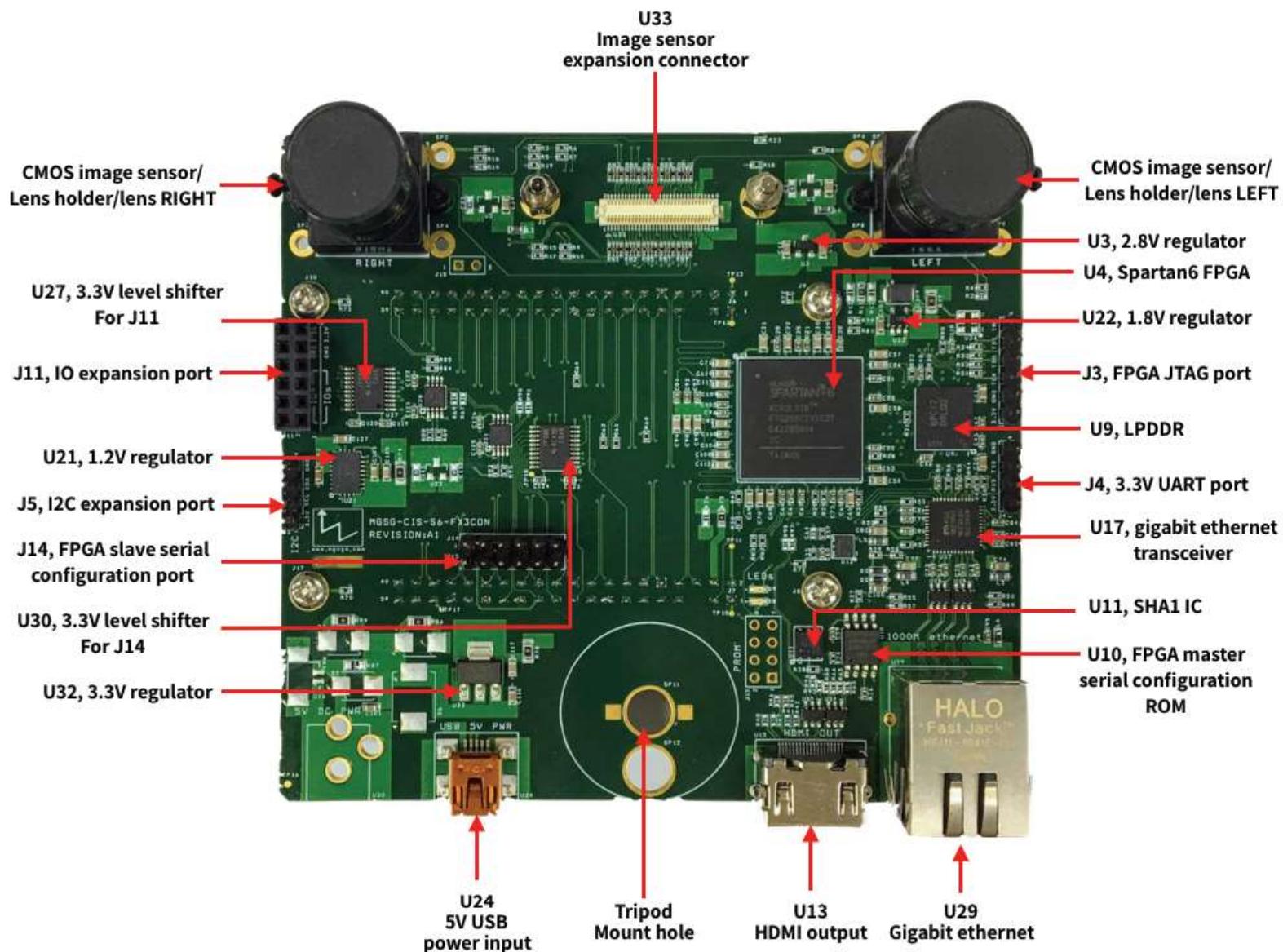


Figure 2.1.1 M-CIS-S6-FX3CON top side layout

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## M-CIS-S6-FX3CON USER MANUAL

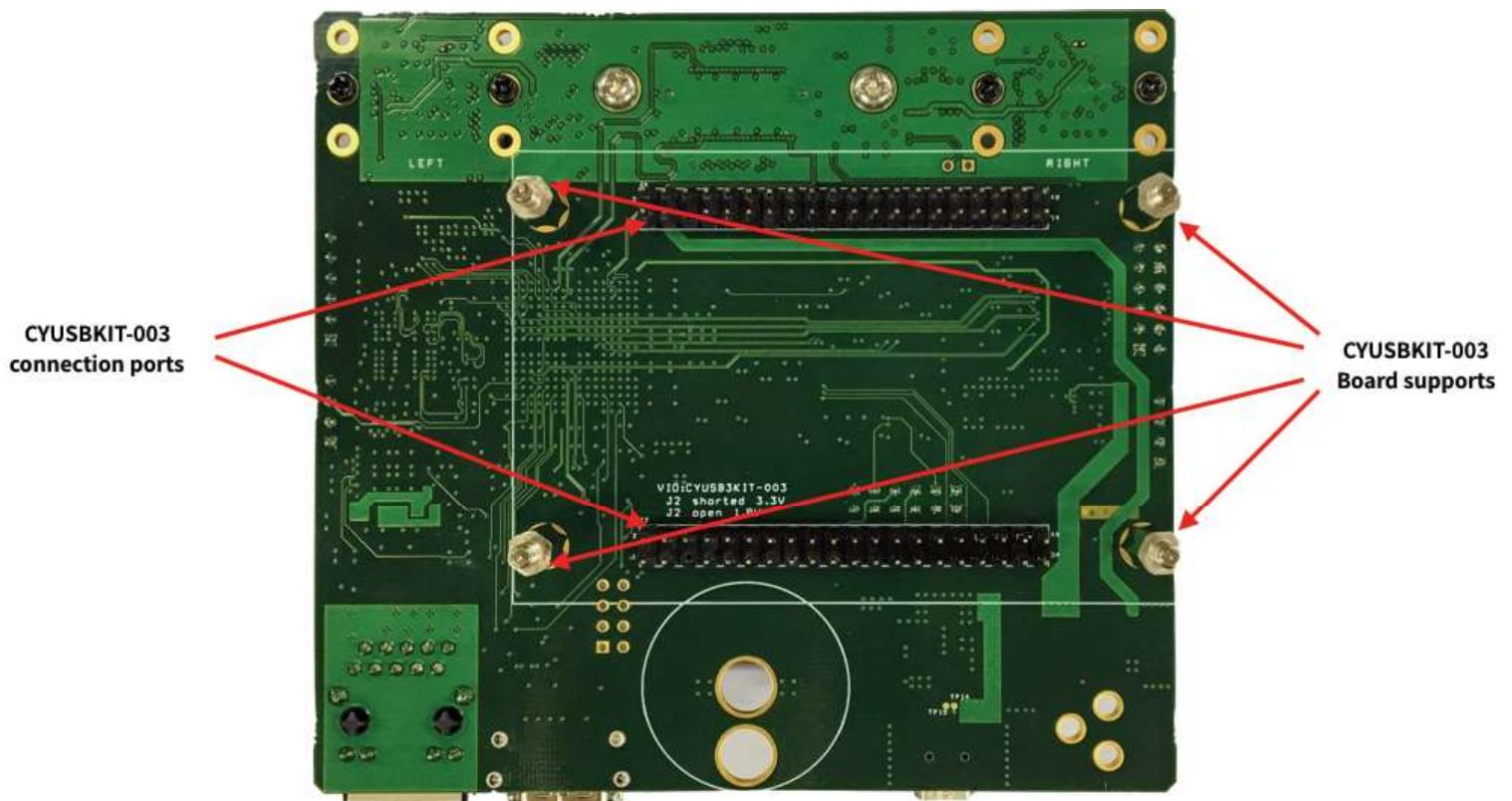


Figure 2.1.2 M-CIS-S6-FX3CON bottom side layout

## 2.2 Dimension

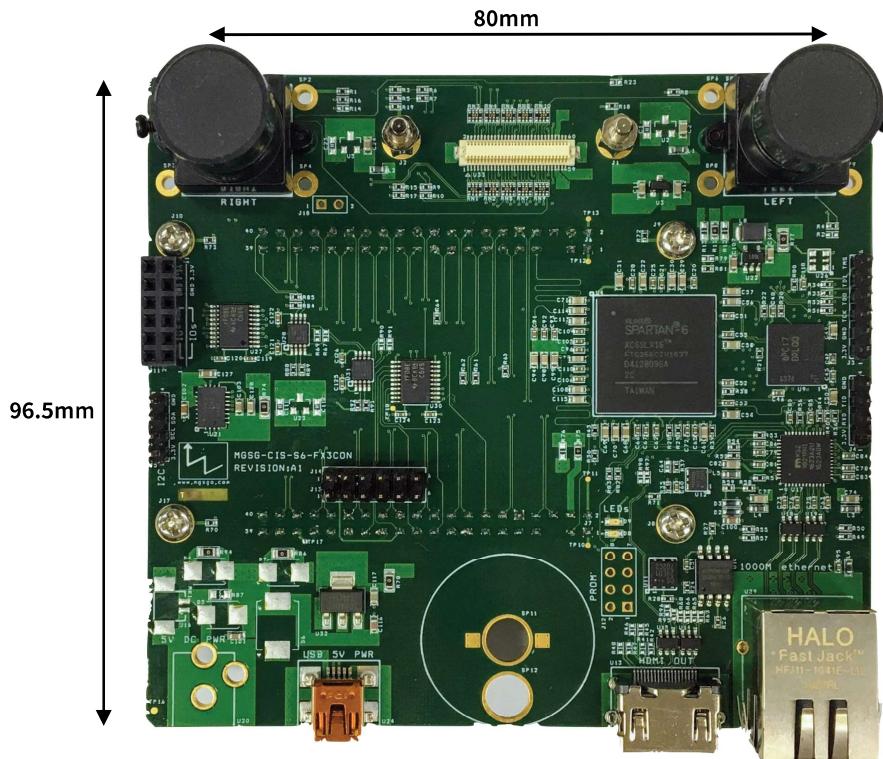


Figure 2.2.1 M-CIS-S6-FX3CON top side dimension

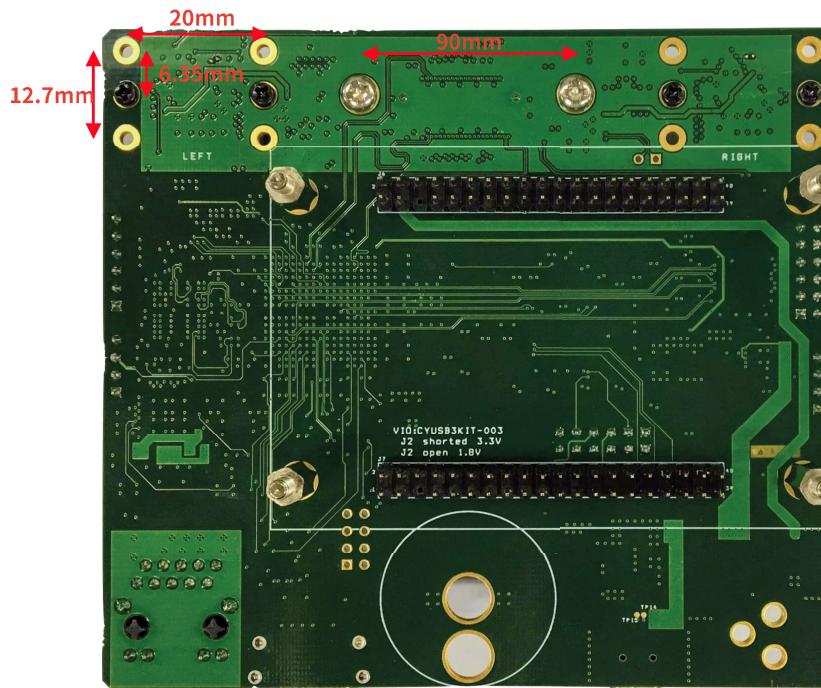


Figure 2.2.2 M-CIS-S6-FX3CON bottom side dimension

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## 2.3 Specifications

- Power input
  - DC 5V 1A maximum
  - USB mini-B port
- FPGA
  - XC6SLX16-2FTG256C
  - Xilinx Spartan6
- Two CIS(CMOS image sensor)s
  - MT9M114EBLSTCZ-CR1
  - ONSEMI(Aptina) 1280x960 CIS
- Two M12 lens holders
- Two M12 lenses
  - Focal length 3.6mm or similar
  - No IR cut filter
- LPDDR DRAM
  - MT46H32M16LFBF-5 IT:C
  - Micron LPDDR
- Gigabit ethernet PHY
  - KSZ9021RNI
  - MICREL Gigabit ethernet PHY
- CYUSB3KIT-003(Cypress FX3 board) connection ports
  - Two 2.54mm pitch 40pin connectors
  - **Not included CYUSB3KIT-003 board**
- HDMI port
  - Only TMDS signal output through Spartan6 use TMDS\_33 IO
  - No support HDMI HOT plug detect voltage output
  - No HDMI CEC/I2C(DDC) controls

## 3. Examples

### 3.1 System requirements and basics

- DC 5V USB power cable connect(cable included, power source not included)

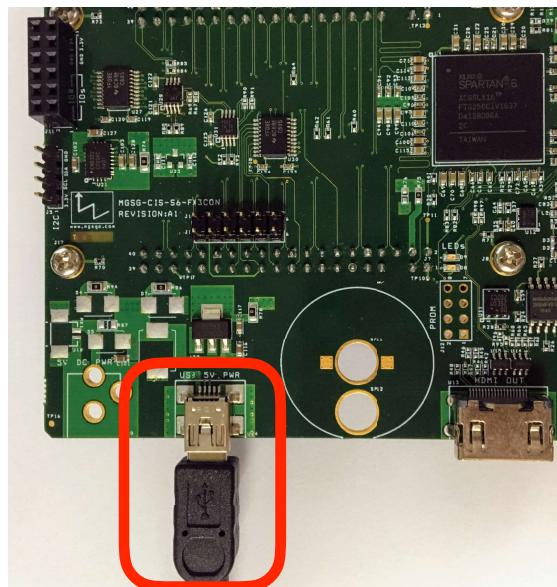


Figure 3.1.1 M-CIS-S6-FX3CON USB power cable connection

- Xilinx JTAG(for FPGA configuration) cable : 3.3V IOs



Figure 3.1.2 M-CIS-S6-FX3CON Xilinx JTAG cable(**not included**) connection

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## M-CIS-S6-FX3CON USER MANUAL

- Xilinx Spartan6/Cypress FX3 development tool
  - Xilinx ISE 14.7
    - [https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/v2012\\_4---14\\_7.html](https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/v2012_4---14_7.html)
    - [https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/14\\_7-windows.html](https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/14_7-windows.html)
  - Cypress FX3 SDK 1.3.4
    - <https://www.cypress.com/documentation/software-and-drivers/ez-usb-fx3-software-development-kit>
- Bit file generate using Xilinx ISE14.7

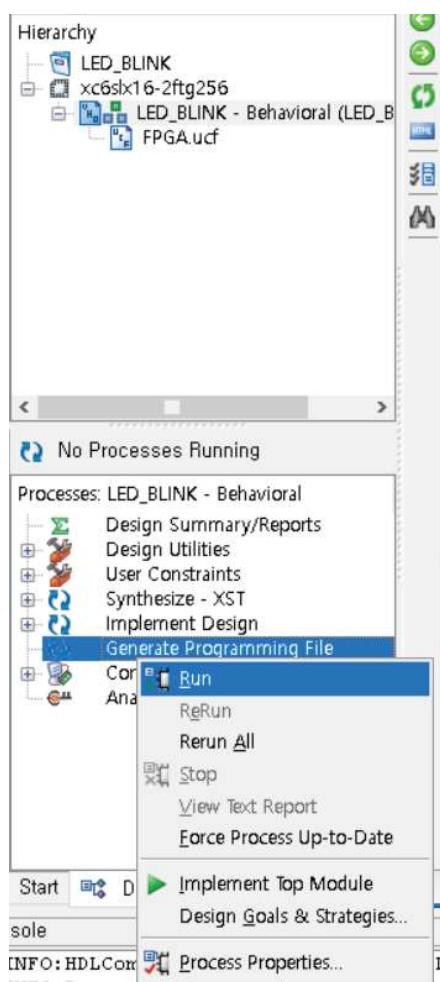


Figure 3.1.3 Bit file generate use Xilinx ISE14.7

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## M-CIS-S6-FX3CON USER MANUAL

- Bit file download to Spartan6 FPGA using Xilinx JTAG and iMPACT

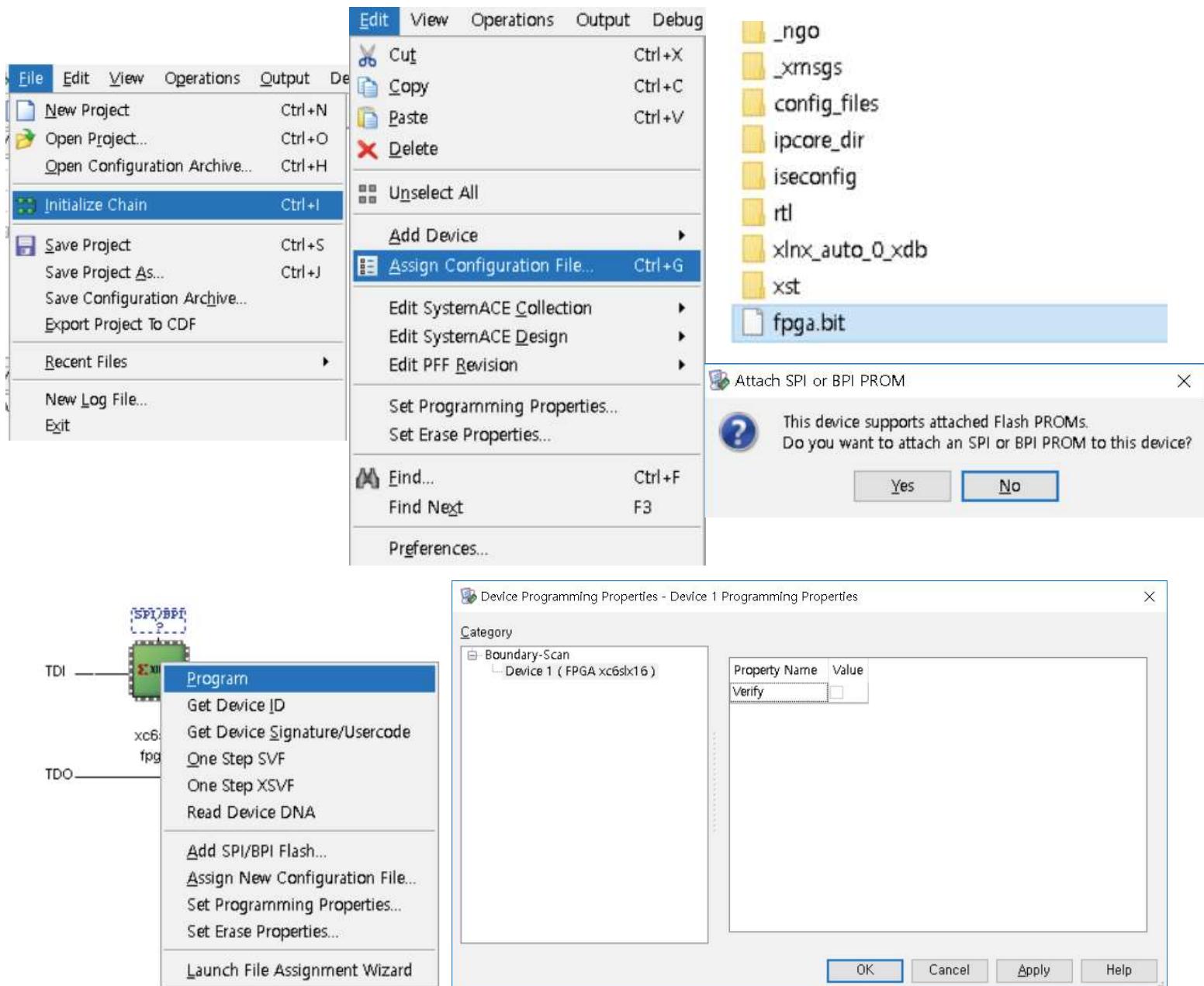


Figure 3.1.4 Bit file download to Spartan6 FPGA use Xilinx JTAG and iMPACT

## M-CIS-S6-FX3CON USER MANUAL

- Flash(MCS) file generate for 64MB FPGA boot flash(W25Q64FVSSIG) using iMPACT

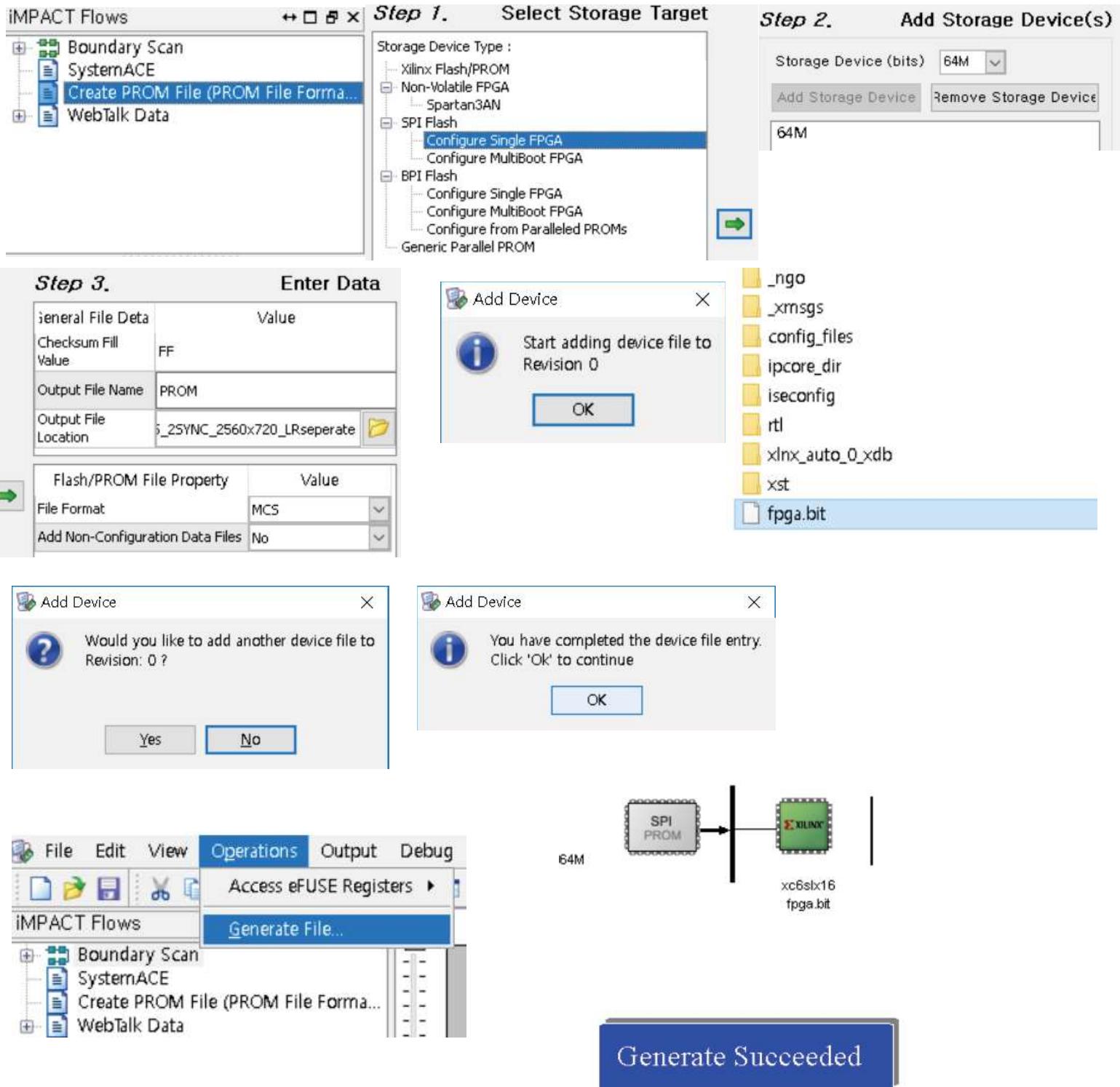
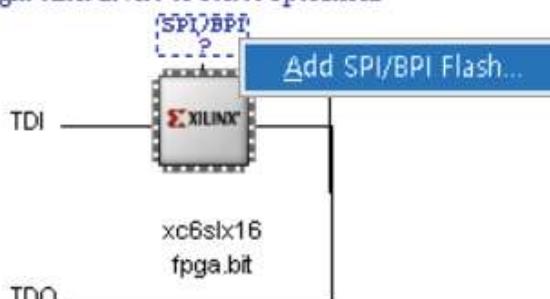


Figure 3.1.5 Flash(MCS) file generate for 64MB FPGA boot flash(W25Q64FVSSIG) use iMPACT

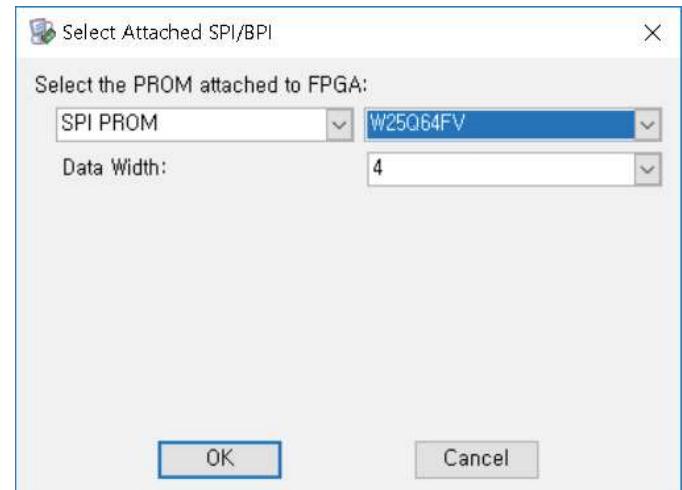
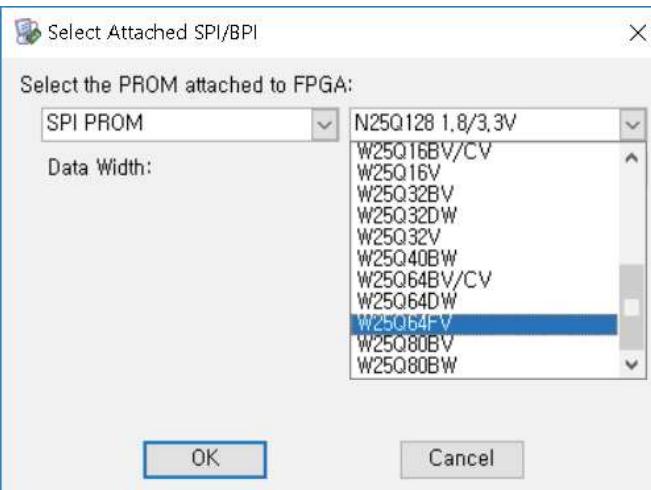
## M-CIS-S6-FX3CON USER MANUAL

- Flash(MCS) file download to 64MB FPGA boot flash(W25Q64FVSSIG) using iMPACT

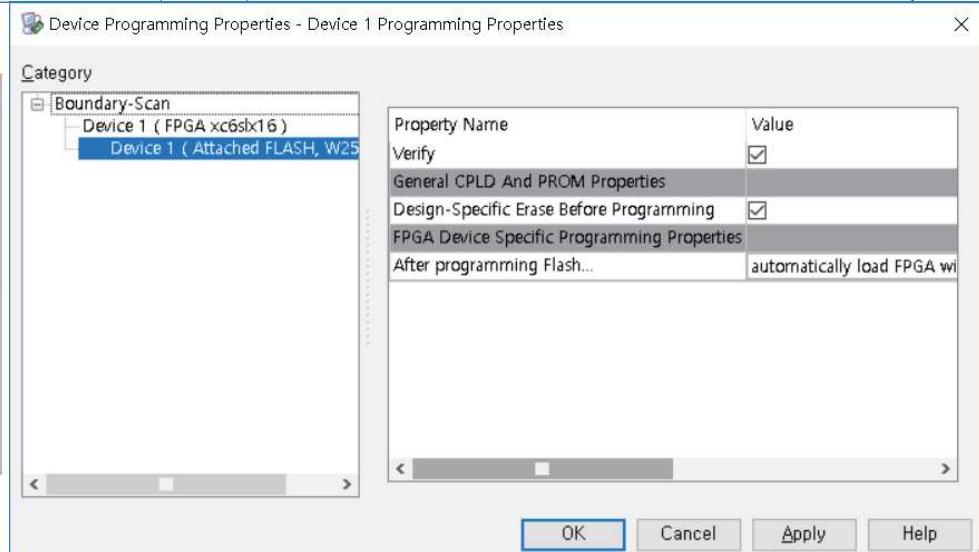
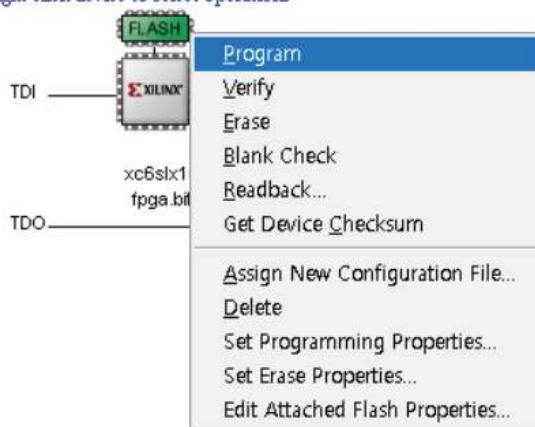
Right click device to select operations



- \_ngo
- \_msgs
- config\_files
- ipcore\_dir
- iseconfig
- rtl
- xlnx\_auto\_0\_xdb
- xst
- PROM.mcs



Right click device to select operations



Program Succeeded

Figure 3.1.6 Flash(MCS) file download to 64MB FPGA boot flash(W25Q64FVSSIG) use iMPACT

### 3.2 LED blink example

- LED\_BLINK : Example of LEDs D8 and D9 turning on alternately
- FPGA N11 pin output is low(0V), D8 LED ON
- FPGA T11 pin output is high(3.3V), D9 LED ON

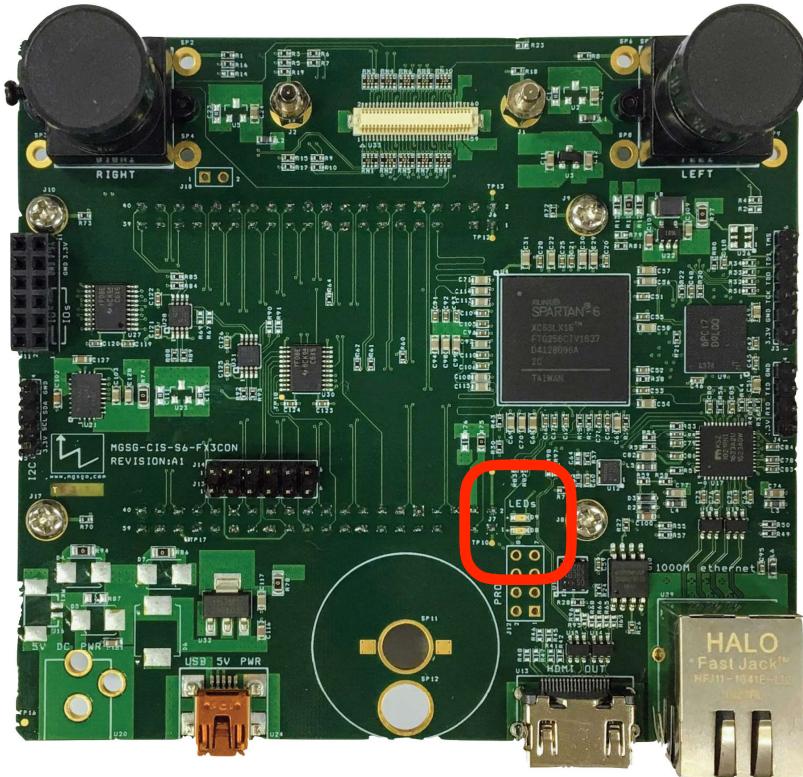


Figure 3.2.1 LED D8 and D9 on M-CIS-S6-FX3CON board

### 3.3 USB3.0 UVC single CIS (AN75779, 1280x720@30fps) example

- UVC\_CIS\_BYPASS\_LEFT\_1280x720 : Example of UVC(Universal Video Class) camera using 1 image sensor
- In AN75779(Cypress FX3 UVC example), M-CIS-S6-FX3CON act likes MT9M114 sensor board
  - AN75779 : <https://www.cypress.com/documentation/application-notes/an75779-how-implement-image-sensor-interface-using-ez-usb-fx3-usb>
  - AN75779 firmware can be used without modification.
- CYUSB3KIT-003 board not included
  - CYUSBKIT-003 kit link : [https://www.cypress.com/products/ez-usb-fx3-superspeed-usb-30-peripheral-controller#tabs-0-bottom\\_side-3](https://www.cypress.com/products/ez-usb-fx3-superspeed-usb-30-peripheral-controller#tabs-0-bottom_side-3)

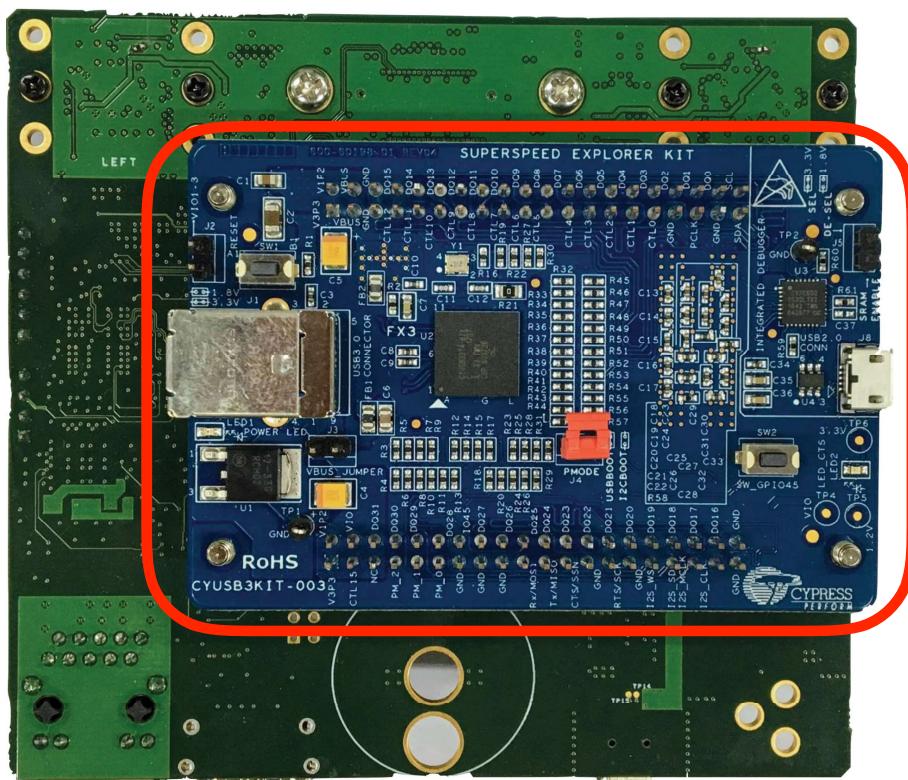


Figure 3.3.1 M-CIS-S6-FX3CON and CYUSBKIT-003(not included, all jumper OFF except PMODE J4)

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## M-CIS-S6-FX3CON USER MANUAL

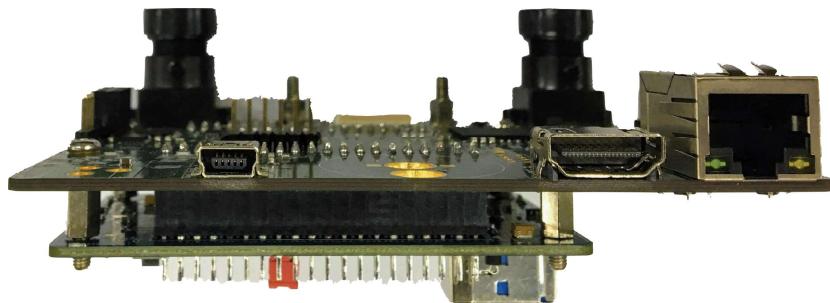


Figure 3.3.2 M-CIS-S6-FX3CON and CYUSBKIT-003(**not included**) connection

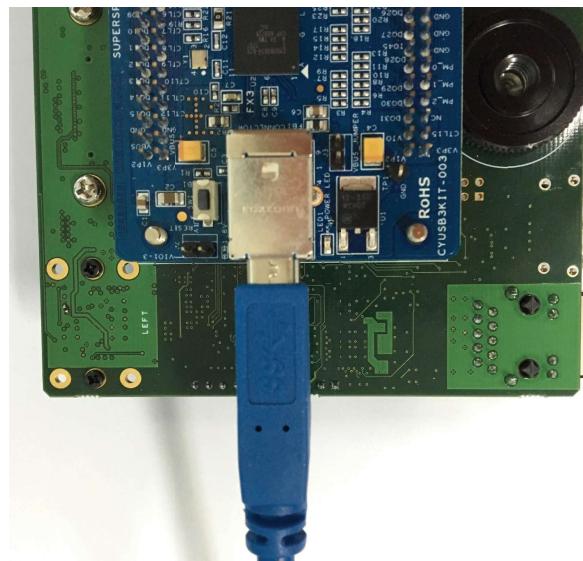


Figure 3.3.3 CYUSBKIT-003(**not included**) USB3.0 cable connection

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## M-CIS-S6-FX3CON USER MANUAL

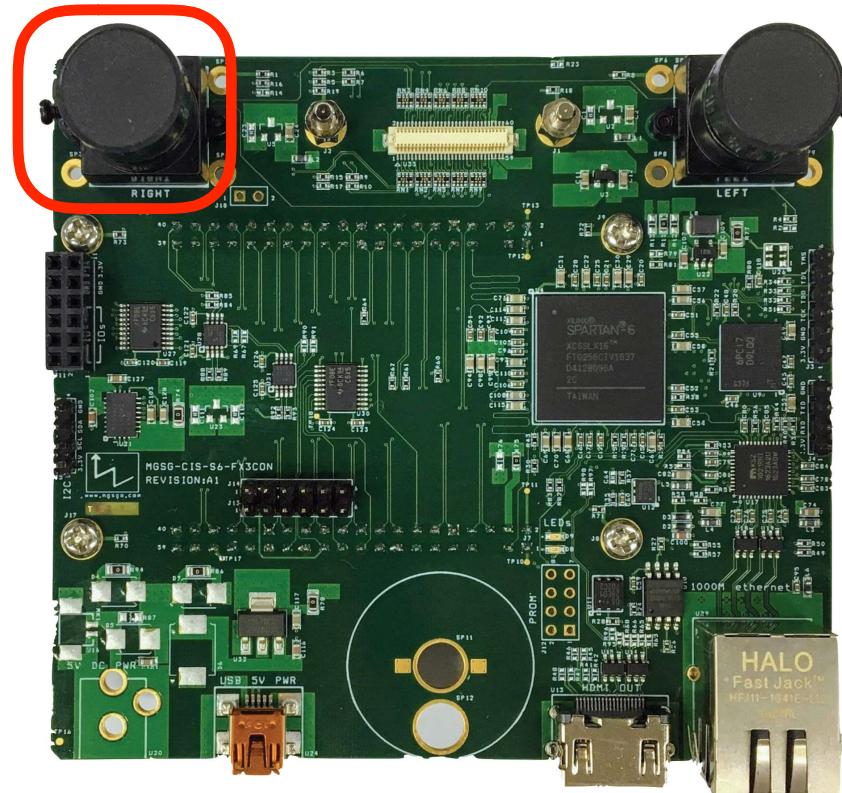


Figure 3.3.4 MT9M114 CMOS image sensor and lens

### 3.4 USB3.0 UVC dual CIS (AN75779, 2560x720@30fps) example

- UVC\_CIS\_LEFT\_RIGHT\_2560x720 : Example of UVC(Universal Video Class) camera using 2 image sensor
- In AN75779(Cypress FX3 UVC example), M-CIS-S6-FX3CON act likes MT9M114 sensor board
  - AN75779 : <https://www.cypress.com/documentation/application-notes/an75779-how-implement-image-sensor-interface-using-ez-usb-fx3-usb>
  - AN75779 firmware modifications.
    - GPIO bus width : 8bit ==> 16bit
    - Image resolution@frame rate : 1280x720@30fps ==> 2560x720@30fps
- CYUSB3KIT-003 board not included
  - CYUSBKIT-003 kit link : [https://www.cypress.com/products/ez-usb-fx3-superspeed-usb-30-peripheral-controller#tabs-0-bottom\\_side-3](https://www.cypress.com/products/ez-usb-fx3-superspeed-usb-30-peripheral-controller#tabs-0-bottom_side-3)

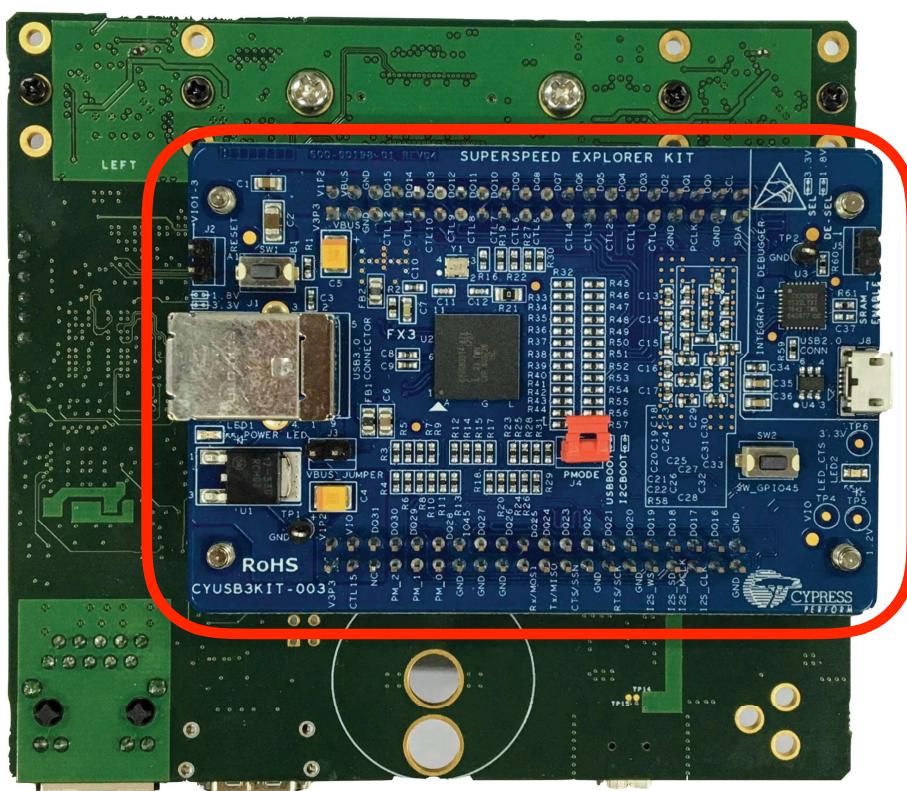


Figure 3.4.1 M-CIS-S6-FX3CON and CYUSBKIT-003(**not included**, all jumper OFF except PMODE J4)

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## M-CIS-S6-FX3CON USER MANUAL

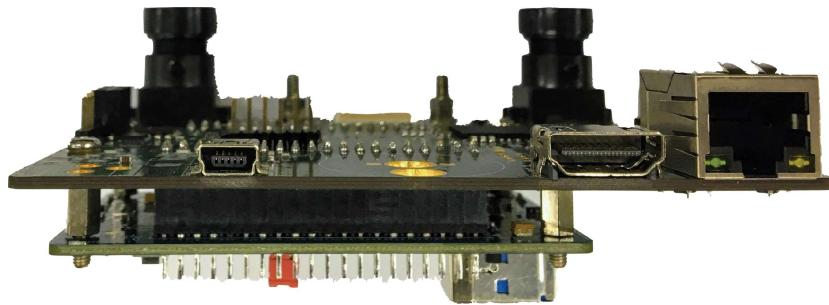


Figure 3.4.2 M-CIS-S6-FX3CON and CYUSBKIT-003(**not included**) connection

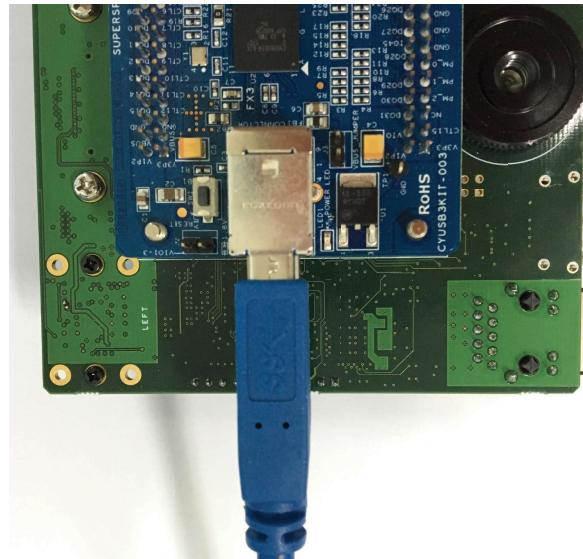


Figure 3.4.3 CYUSBKIT-003(**not included**) USB3.0 cable connection

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## M-CIS-S6-FX3CON USER MANUAL

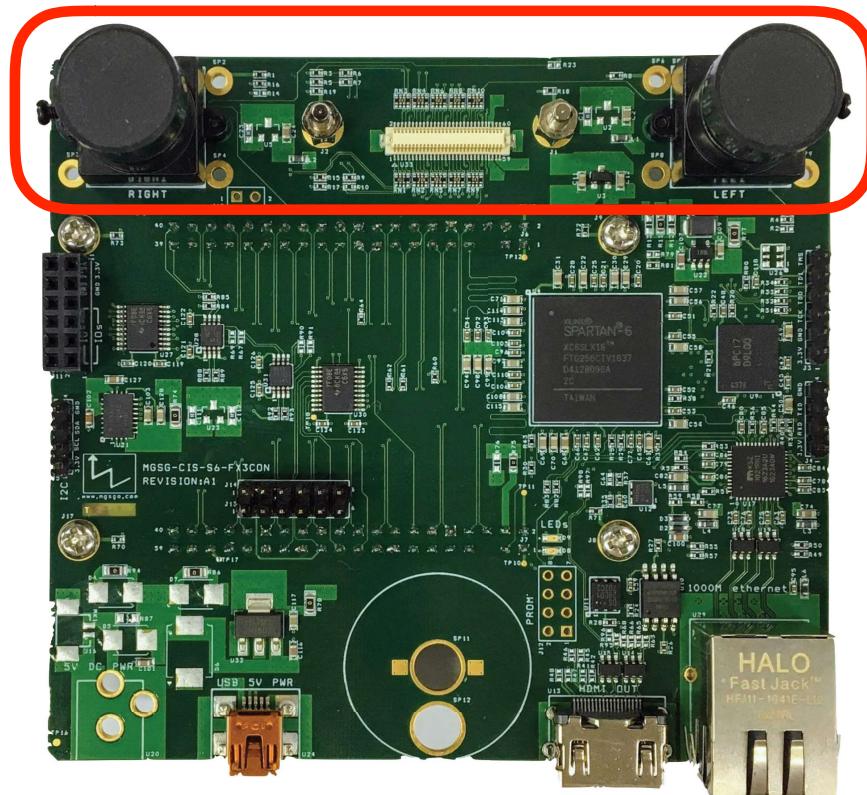


Figure 3.4.4 CMOS image sensors MT9M114 and lenses

### 3.5 Configuring an FPGA over FX3(use AN84868) example

- CONFIG\_FPGA\_OVER\_FX3 : Example of FX3 configure Spartan6 FPGA(slave serial mode) using AN84868(Configuring FPGA example)
- AN84868 : <https://www.cypress.com/documentation/application-notes/an84868-configuring-fpga-over-usb-using-cypress-ez-usb-fx3>
- FPGA binary file use LED blink example
- CYUSB3KIT-003 board not included
  - CYUSBKIT-003 kit link : [https://www.cypress.com/products/ez-usb-fx3-superspeed-usb-30-peripheral-controller#tabs-0-bottom\\_side-3](https://www.cypress.com/products/ez-usb-fx3-superspeed-usb-30-peripheral-controller#tabs-0-bottom_side-3)

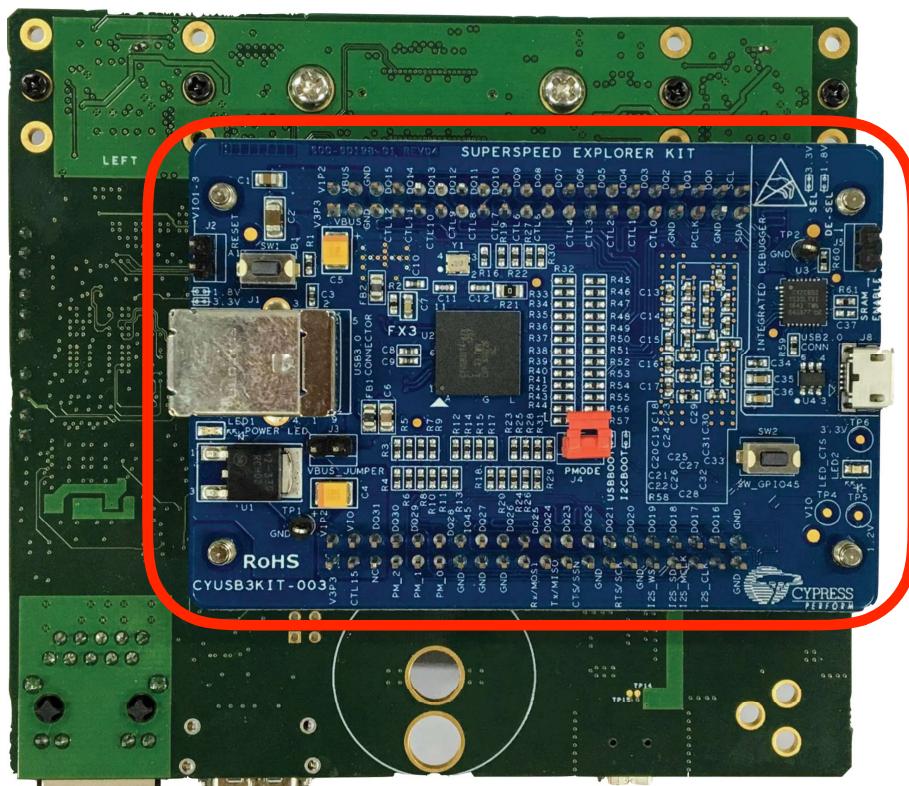


Figure 3.5.1 M-CIS-S6-FX3CON and CYUSBKIT-003(**not included**, all jumper OFF except PMODE J4)

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## M-CIS-S6-FX3CON USER MANUAL

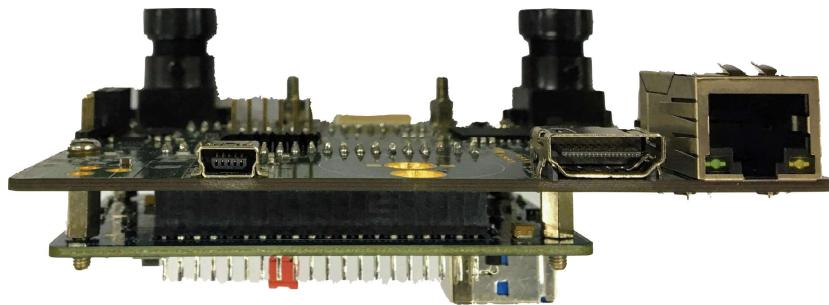


Figure 3.5.2 M-CIS-S6-FX3CON and CYUSBKIT-003(**not included**) connection

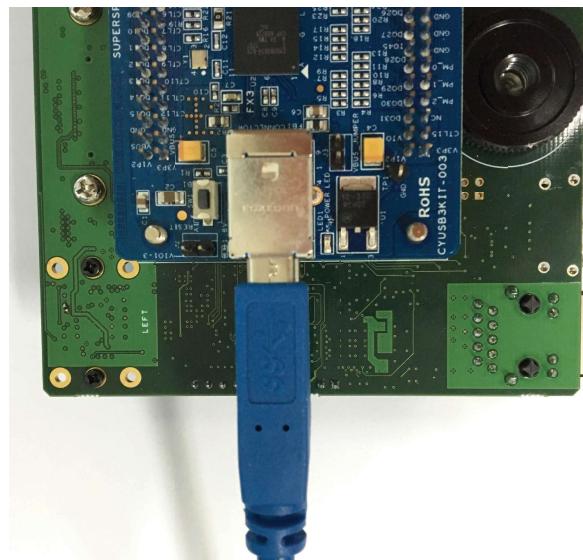


Figure 3.5.3 CYUSBKIT-003(**not included**) USB3.0 cable connection

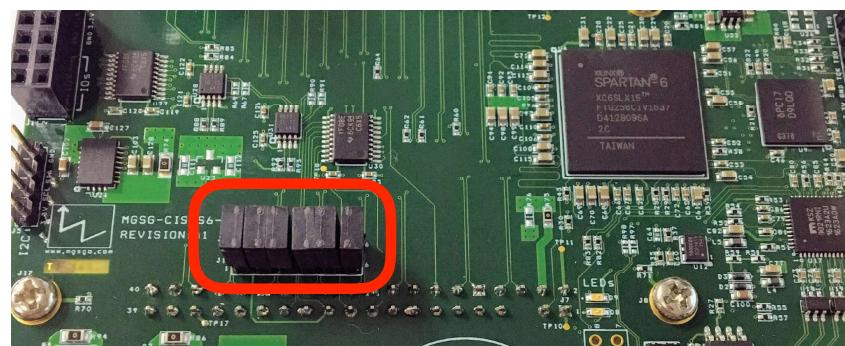


Figure 3.5.4 M-CIS-S6-FX3CON J14 jumper connections for AN84868

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### 3.6 HDMI(TMDS) video output example

- HDMI\_TMDS\_VIDEO\_OUT : Example of TMDS video signal output through HDMI connector using TMDS\_33 IO of Spartan6 FPGA
- Xilinx UG381([https://www.xilinx.com/support/documentation/user\\_guides/ug381.pdf](https://www.xilinx.com/support/documentation/user_guides/ug381.pdf))
- Up to 1280x720@60Hz or 1920x1080@30Hz TMDS signal output through HDMI connector
- No support HDMI HOT plug detect voltage output and HDMI CEC/I2C(DDC) controls
- HDMI cable is **not included**

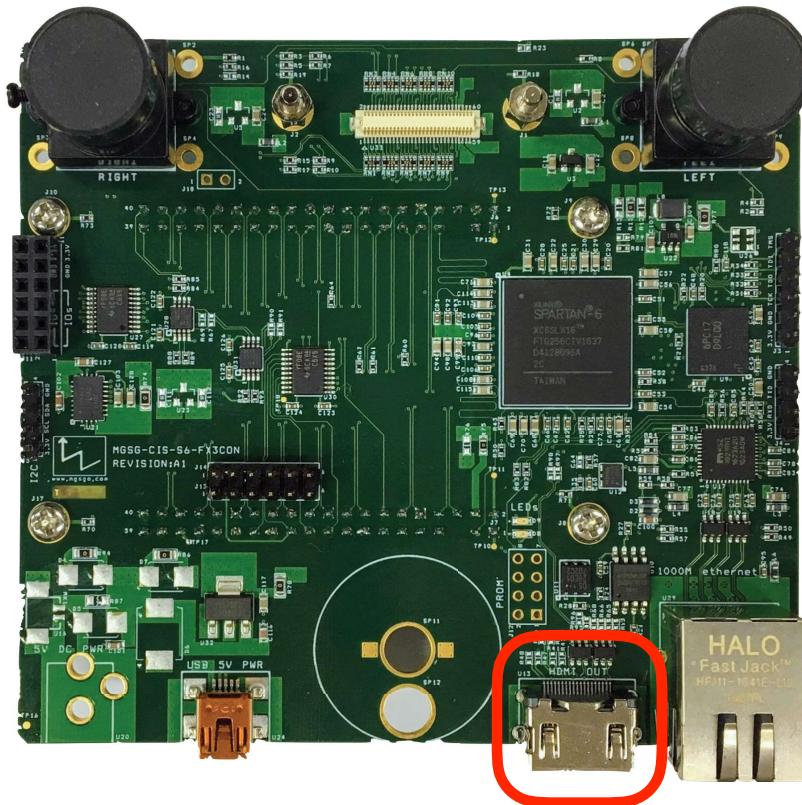


Figure 3.6.1 M-CIS-S6-FX3CON HDMI output port

### 3.7 Gigabit ethernet(1000M) UDP throughput test example

- GIGABIT\_UDP\_THROUGHPUT\_TEST\_BINARY : Example of UDP throughput test using gigabit ethernet MAC/UDP stack (bit file only)
- Gigabit ethernet(1000M) PHY : KSZ9021 IC
- Gigabit ethernet(1000M) MAC/UDP stack
  - COMBLOCK IP use(COM-5401SOFT, COM-5402SOFT)
  - <https://comblock.com/download/com5401soft.pdf>
  - <https://comblock.com/download/com5402soft.pdf>
- Ethernet cable is **not included**
  - CAT5E or higher cable use for 1Gbps connection
  - Use cross cable to connect direct PC LAN card

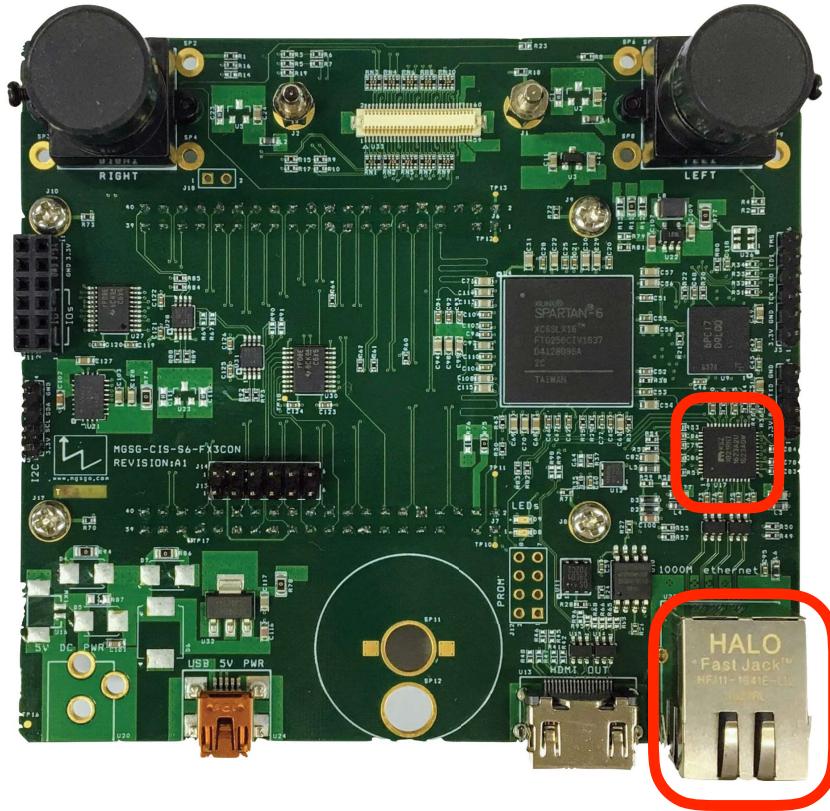


Figure 3.7.1 M-CIS-S6-FX3CON Ethernet port(RJ45) and PHY IC(KSZ9021)

### 3.8 LPDDR test use Xilinx MIG example

- LPDDR\_MIG\_TRAFFIC : Example of LPDDR write/read example at 200MHz use Xilinx MIG(UG388)
  - [https://www.xilinx.com/support/documentation/user\\_guides/ug388.pdf](https://www.xilinx.com/support/documentation/user_guides/ug388.pdf)
  - LPDDR part number : MT46H32M16LFBF-5 IT:C

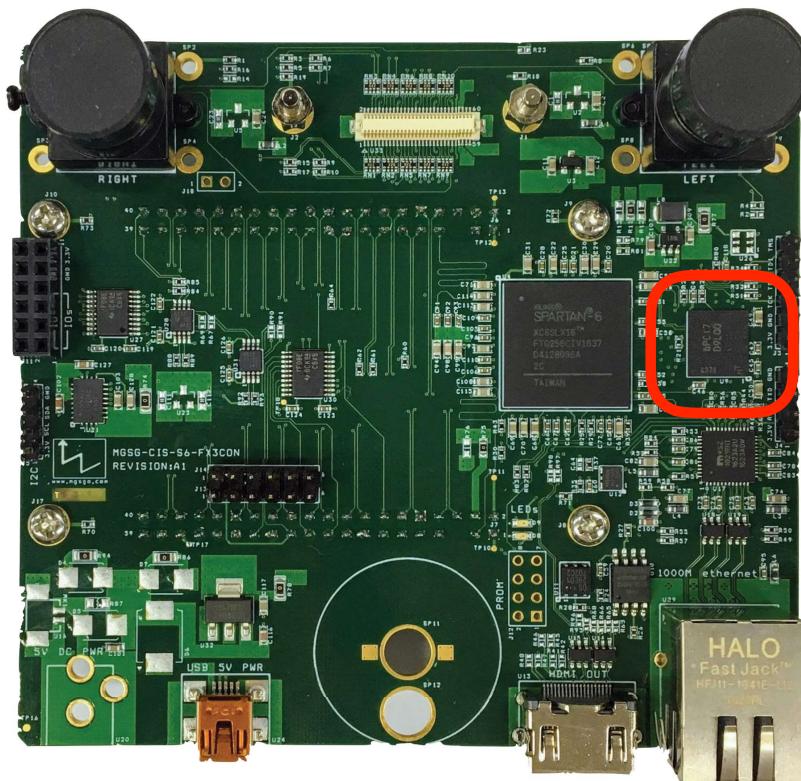


Figure 3.8.1 M-CIS-S6-FX3CON LPDDR memory

## 3.9 SHA-1 EEPROM control example

- SHA1\_AUTHENTICATION : Example of SHA-1 EEPROM control((AVNET reference design required)
  - DS28E01 reference design
    - <https://www.avnet.com/shop/us/products/avnet-engineering-services/aes-s6ev-lx16-g-3074457345630217084/>
    - XAPP780(for DS2432)
      - [https://www.xilinx.com/support/documentation/application\\_notes/xapp780.pdf](https://www.xilinx.com/support/documentation/application_notes/xapp780.pdf)

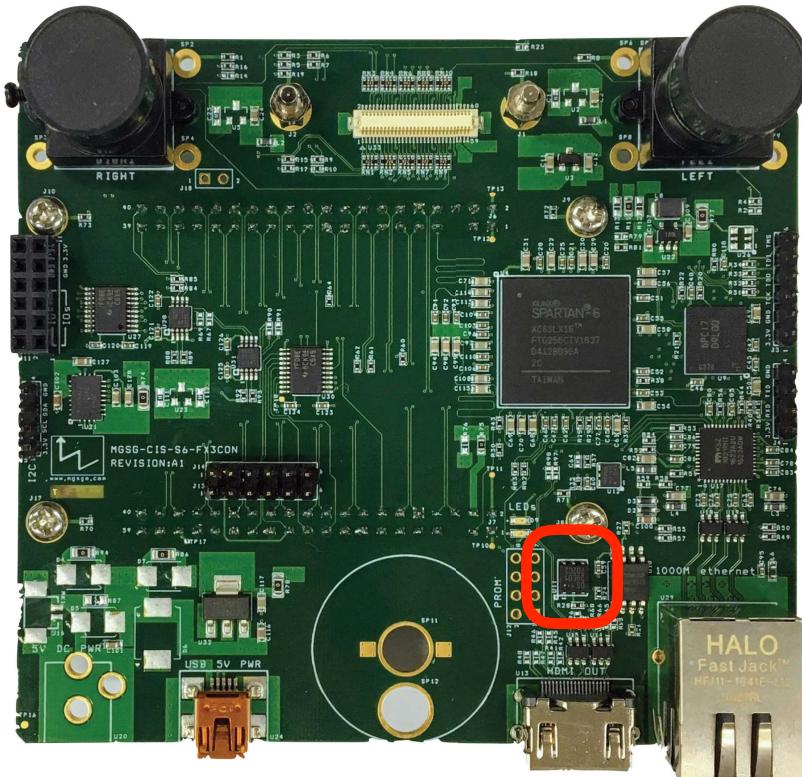


Figure 3.9.1 SHA-1 IC(DS28E01)

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## **4. Support**

### **4.1 Purchase support**

Contact to each distributor.

### **4.2 Technical support**

Contact to [msgg\\_opensource@gmail.com](mailto:msgg_opensource@gmail.com)

Github page [github.com/msggo/M-CIS-S6-FX3CON](https://github.com/msggo/M-CIS-S6-FX3CON)