Omozusi Guobadia

Email: oeguobadia@gmail.com
Phone: +1(281)748-8174
LinkedIn: www.linkedin.com/in/mozig

223 Charles Street
Cambridge, MA 02141

EDUCATION

Massachusetts Institute of Technology, Cambridge, MA
M.Eng, Neuroengineering, June 2025 GPA: x.xx/4
B.Sc, Electrical Engineering and Neuroscience, June 2023 GPA: 3.63/4

PROJECTS

SplitBit: RF Transponder Timing System (RF Project): Created a low-cost automatic RF transponder sports timing system prototype tailored for young high-school athletes to test their speed. Design featured a quadruple antenna circuit with op-amps for signal enhancement and a Vector Network Analyzer (VNA) as a signal generator.

100-Node Discrete Hopfield Network (Neural Computation Project): Designed a 100-Node, Asynchronous Hopfield Network in PYTHON and examined the effects of differing pattern weights on the retrieval probability of the system. Also created synchronous version and examined effects on the speed of convergence.

Color Organ and Light-Wave Communicator (Analog Design Project): Designed a color organ circuit that drove LEDs based on audio signal strength and frequency bands and a light-wave communicator circuit that utilized LED properties for signal transmission. Developed circuit schematics, conducted rigorous tests using various tools, and implemented an RC low-pass filter to improve signal quality.

Xilinx FPGA AR Card (Digital Design Project): Developed a system projecting interactive 3D figures onto an AR card's position on a monitor. Created a subprogram capable of detecting specific pixel RGB color concentrations in the camera frame, enabling the detection of the AR card's center of mass and angle deviation. Analyzed the FPGA's memory and signal processing utilization rates, implementing customized VERILOG code to meet project requirements.

SKILLS

Programming: Python, MATLAB, Julia Programming, C, Verilog LaTeX.
Engineering: CAD, Soldering and Test Equipment, Circuit Design, FPGA Digital Design, Data Analysis, Embedded Devices

EXPERIENCE

Hardware Developer Intern IBM
June 2022 - August 2022 Poughkeepsie, NY
Developed a comprehensive library of IC timers, SOICs, DIPs, temperature sensors, and other circuits utilized in industry-ready cards featured in the IBM Z Metis Mainframe through Cadence Allegro PCB Design software.

Undergraduate Research Assistant MIT Media Lab
December 2021 - May 2022 Cambridge, MA
Designed physical configuration of the AttentivU EEG headware through soldering and connectivity testing.

Hardware Developer Intern Signify
June 2021 - August 2021 Remote
Developed code that enabled the autonomous update function using Yocto-based operating software on Raspberry Pi 3+ microcontrollers

INTERESTS

Medical Device Development, Brain-Machine Interfaces

AFFILIATIONS

Track and Field, Engine Team, NSBE