



**TSMC 90nm CLN90G Process
SAGE-XTM v3.0
Standard Cell Library
Databook**

March 2005

Release 1.1

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Preface

Revision History

This document contains the release history for the TSMC 90nm CLN90G Process SAGE-X™ v3.0 Standard Cell Library Databook.

Part Number	Release Number	Date of Release	Updates
DB-SX-TSM032-1.0/90nm	1.0	April 2004	<ul style="list-style-type: none">Initial release
DB-SX3-TSM032-1.1/90nm	1.1	March 2005	<ul style="list-style-type: none">Remove HOLD and RFRD datasheets

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Artisan's SAGE-X™ standard cell library builds upon our SAGE architecture, producing the optimum combination of high-density with high-performance. The cell line-up is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results.

How This Book Is Organized

This introduction is organized into three sections:

- ***Global Parameters*** provides an overview of parameters specific to your SAGE-X library.
- ***Special Cells*** details the types of special cells included in the library.
- ***Reading the Standard Cell Datasheet*** describes the components of each datasheet.

Datasheets for each cell in this library are provided after the introduction. The datasheets are included in alphabetical order within the following categories:

- Base Cells
- Advanced Arithmetic Cells
- Register File Cells
- Synthesis Optimized Arithmetic Cells

Global Parameters

This section specifies global parameters for the TSMC 90nm CLN90G Process SAGE-X™ v3.0 Standard Cell Library. It covers physical specifications, electrical specifications, derating factors, propagation delay calculation, timing constraints, power calculation, and power-rail strapping.

Physical Specifications

Table 1 shows the physical design specifications of this library.

Table 1. Physical Specifications

Drawn Gate Length (μm)	0.1
Layers of Metal	4, 5, 6, 7, 8 and 9
Layout Grid (μm)	0.005
Vertical Pin Grid (μm)	0.28
Horizontal Pin Grid (μm)	0.28
Cell Power and Ground Rail Width (μm)	0.42
Cell Height (μm)	2.52

In this library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

The SAGE-X library also supports designs with four, five, six, seven, eight and nine layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement. See "TSMC 90nm CMOS Logic Design Rule" design rule manual. You must define these rules correctly for the place-and-route tool.

Table 2 describes the electrical specifications for this library.

Table 2. Electrical Specifications

Parameter	Minimum	Typical	Maximum
DC Supply Voltage (Vdd)	0.9V	1.0V	1.1V
Junction Temperature	-40°C	25°C	125°C

Table 3 shows the derating factors for this SAGE-X Standard Cell Library.

Table 3. Derating Factors

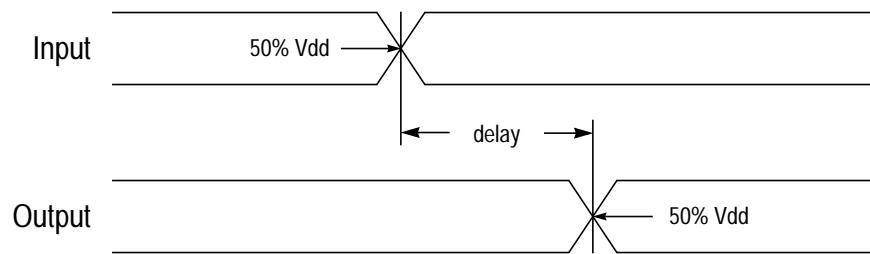
K_{Process} (slow)	1.321
K_{Process} (typical)	1.000 (by definition)
K_{Process} (fast)	0.757

Table 3. Derating Factors

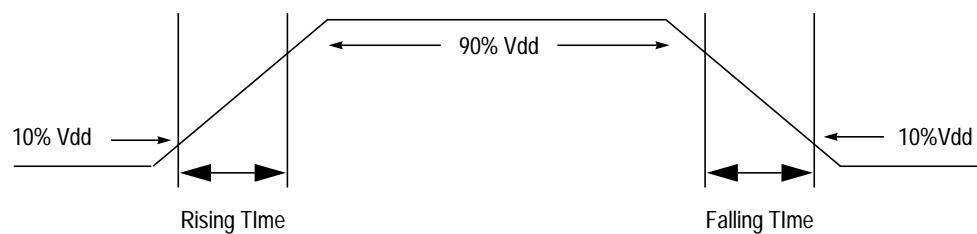
K_{Volt} (1.0V to 0.9V)	-1.85/V
K_{Volt} (1.0V to 1.1V)	-1.22/V
K_{Temp} (25°C to -40°C)	0.00093/°C
K_{Temp} (25°C to 125°C)	0.00101/°C

Propagation Delay and Transition Time

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates the propagation delay.

Figure 1. Propagation Delay

The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 illustrates transition time measurements for rising and falling signals.

Figure 2. Transition Time

Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.018ns and a linearized load factor, K_{load} , which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.28 μ m horizontal pitch) and metal3 (0.28 μ m vertical pitch) routing grid across the entire cell layout.

The SAGE-X Standard Cell Library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Derating Factors

Derating factors are coefficients that the typical process characterization data is multiplied by to arrive at timing data that reflects appropriate operating conditions. Table 3 on page 12 provides derating factors for variations in process case, temperature, and voltage.

Derating factors are derived by averaging the performance of many different cells in the library. A particular combination of cells may perform better or worse than indicated by these derating factors.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load} , and C_{load}) and the delay derating factors, the estimated total propagation delay is calculated as such:

$$t_{TPD} = (K_{Process}) \cdot [1 + (K_{Volt} \cdot \Delta V_{dd})] \cdot [1 + (K_{Temp} \cdot \Delta T)] \cdot t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} \cdot C_{load})$$

where:

t_{TPD} = total propagation delay (ns);

$t_{typical}$ = delay at typical corner—1.0V, 25°C, typical process (ns);

$t_{intrinsic}$ = delay through the cell when there is no output load (ns);

K_{load} = load delay multiplier (ns/pF);

C_{load} = total output load capacitance (pF);

$K_{Process}$ = process derating factor, where process is slow, typical, or fast;
 K_{Volt} = voltage derating factor (/V);
 ΔV_{dd} = $V_{dd} - 1.0V$;
 K_{Temp} = temperature derating factor (/°C);
 ΔT = junction temperature - 25°C.

Timing Constraints

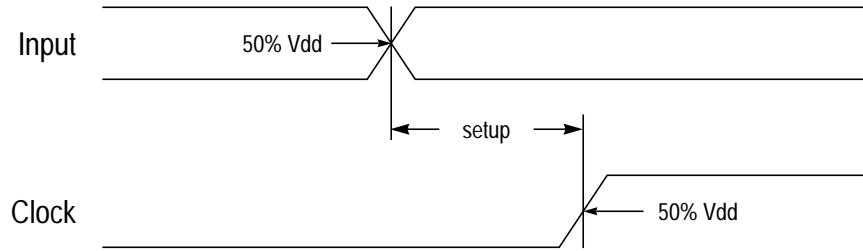
Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.018ns data slew and 0.018ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.28μm horizontal pitch) and metal3 (0.28μm vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup constraint values are measured as the interval between the data signal crossing 50% of V_{dd} and the clock signal crossing 50% of V_{dd} . For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

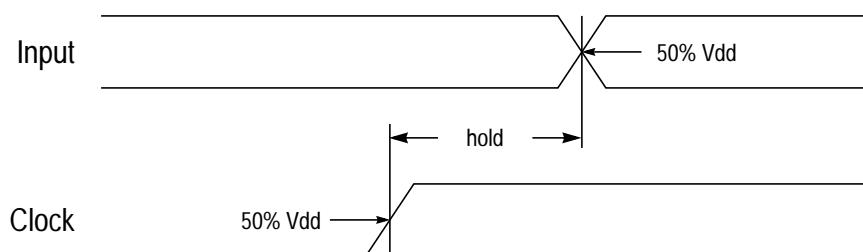
Figure 3. Setup Time

Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

NOTE: Artisan does not incorporate any hold time margins in the Synopsys, TLF, StarDC, or any other timing models. Chip designers should develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

Figure 4. Hold Time

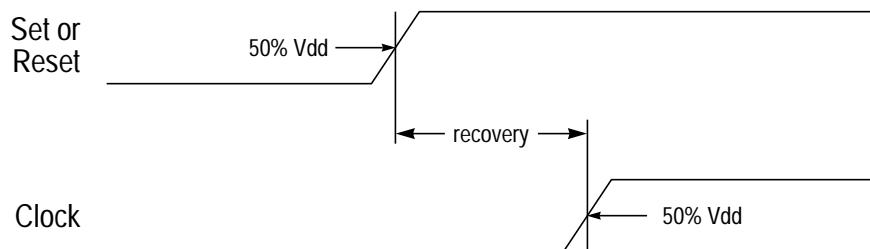
Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%.

Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time.

Figure 5 illustrates recovery time.

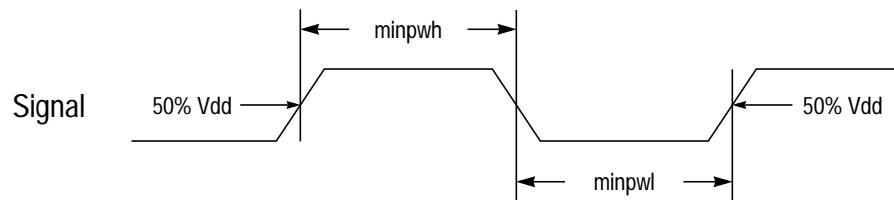
Figure 5. Recovery Time



Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 6 illustrates minimum pulse width.

Figure 6. Minimum Pulse Width



Minimum pulse width is defined as 0.171 ns for all set/reset pins (SN, RN) and 0.161 ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Power Dissipation

The SAGE-X Standard Cell Library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits.

The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The SAGE-X library datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input-pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design.

The AC power tables specify the amount of energy consumed within a cell ($\mu\text{W}/\text{MHz}$) when the corresponding pin changes state at 25°C, 1.0V, and typical process. The energy data in the tables were measured for an input slew of 0.018ns and no loading at the outputs.

For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which *do not* result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^x (E_{in} \bullet f_{in}) + \sum_{n=1}^y \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

where:

- P_{avg} = average power (μW);
- x = number of input pins;
- E_{in} = energy associated with the n th input pin ($\mu\text{W}/\text{MHz}$);
- f_{in} = frequency at which the n th input pin changes state during the normal operation of the design (MHz);
- y = number of output pins;
- C_{on} = external capacitive loading on the n th output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);
- Vdd = operating voltage = 1.0V;
- f_{on} = frequency at which the n th output pin changes state during the normal operation of the design (MHz);
- E_{os} = energy associated with the output pin for sequential cells only ($\mu\text{W}/\text{MHz}$).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator (e.g. Verilog) by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

EXAMPLE: Calculating Power for a DFFXL Cell

For this exercise, assume that a DFFXL cell has clock switching at 133MHz (clock frequency = 66.5MHz), input and output pins switching at 20MHz, and an external capacitive loading on the output pin of 0.02pF. Using the AC Power table provided in the sample DFF datasheet on page 28, the power dissipated by the DFFXL can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^x (E_{in} \bullet f_{in}) + \sum_{n=1}^y \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

Given:

$$x = 2;$$

$$E_{i1} = 0.0056 \mu\text{W}/\text{MHz};$$

$$E_{i2} = 0.0063 \mu\text{W}/\text{MHz};$$

$$f_{i1} = 20 \text{ MHz};$$

$$f_{i2} = 133 \text{ MHz};$$

$$y = 2;$$

$$C_{o1} = 0.02 \text{ pF};$$

$$C_{o2} = 0.02 \text{ pF};$$

$$Vdd = 1.0\text{V};$$

$$f_{o1} = 20 \text{ MHz};$$

$$f_{o2} = 20 \text{ MHz};$$

$$E_{os} = 0.0060 \mu\text{W}/\text{MHz},$$

we have:

$$P_{avg} = \sum_{n=1}^2 (E_{in} \bullet f_{in}) + \sum_{n=1}^2 \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

$$P_{avg} = (E_{i1} \bullet f_{i1}) + (E_{i2} \bullet f_{i2})$$

$$\left(C_{o1} \bullet VDD^2 \bullet \frac{1}{2} f_{o1} \right) + \left(C_{o2} \bullet VDD^2 \bullet \frac{1}{2} f_{o2} \right)$$

$$+ (E_{os} \bullet f_{o1})$$

$$P_{avg} = (0.0056 \bullet 20) + (0.0063 \bullet 133)$$

$$+ \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20) \right) + \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20) \right)$$

$$+ (0.0060 \bullet 20)$$

$$P_{avg} = 1.46 \mu\text{W}$$

Power-Rail Strapping

You must determine the required amount of vertical power-rail strapping to satisfy all requirements imposed by the design methodology for a given design. Power-rail strapping should be sized small enough to optimize standard cell height and maximize router efficiency, yet it must be large enough to provide sufficient power to the cells.

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Given:

- I_{avg} = total average current for the module, calculated from previous section (mA);
- w_{m1} = VSS/VDD metal1 wire width (μm), see Physical Specifications;
- r = number of rows in module;
- d_{m1} = maximum metal1 current density allowed for the process (mA/ μm);
- d_{m2} = maximum metal2 current density allowed for the process (mA/ μm);
- I_{m1} = maximum current that can be supported by all horizontal metal1 wires (mA);
- I_{strap} = total current that must be supported by the vertical metal2 strapping (mA);
- w_{m2} = metal2 wire width required for vertical strapping (μm);
- c = minimum number of metal2 straps;

we have:

$$I_{m1} = w_{m1} \cdot r \cdot 2 \cdot d_{m1},$$

where multiplying by 2 assumes metal1 wires are supplied from both ends;

$$I_{strap} = \frac{(I_{avg} - I_{m1})}{2},$$

where dividing by 2 assumes the metal2 vertical strap wires are supplied from both ends;

$$w_{m2} = \frac{I_{strap}}{d_{m2}},$$

It is recommended that the metal2 wire width, w_{m2} , be divided into c equal portions which are spaced equidistant across the module, where

$$c = \frac{I_{avg}}{I_{m1}}, \text{ rounded up to the next integer.}$$

The same consideration must be given to the number of vias used to connect the metal1 and metal2 straps.

Adding Routing Channels

In the SAGE-X Standard Cell Library, each cell is designed with a uniform cell height of $2.52\mu m$ (i.e., 9 tracks tall with $0.28\mu m$ per track). The cell layouts allow neighboring rows of cells to share common power or ground rails when cells abut each other at the top and bottom edges of the cell bounding box. The sea-of-cells layout with no channels between rows will usually yield the minimum area. In case of extremely congested areas, you may want to separate some rows of cells to increase the number of routing channels within a particular layout region. Because geometries must overlap cell boundaries, a particular spacing between the rows may result in DRC violations for layer spacing. It is recommended that you do not use spacings that cause DRC violations. If these spacings must be used, the DRC violations must be fixed manually by filling the void between the rows with the appropriate layer(s).

Table 4 indicates which DRC violations to expect and how to correct them for a separation between rows of cells.

Table 4. Correcting DRC Violations

Row Separation in Number of Grids	Expected DRC Violations	Action to Correct DRC Violations
0 (Rows Abut)	None	None
1	NP/PP space < 0.24 μ m	Draw NWELL layer between rows to merge NWELL regions above and below row separation.
2	NWELL space < 0.62 to 1.20 depending on the Nwell-Bias M1 space < 0.12 to 2.50 depending on the width of Metal1	Draw NWELL and Metal1 layers between rows to merge NWELL and Metal1 regions above and below row separation.
3	NWELL space < 0.62 to 1.20 depending on the Nwell-Bias μ m	Draw NWELL layer between rows to merge NWELL regions above and below row separation.
4	None	None
5 or more	None	None

Special Cells

This section discusses special cells in the SAGE-X Standard Cell Library.

Antenna-Fix Cell

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. The TSMC antenna effect prevention guideline, "TSMC 90nm CMOS Logic Design Rule," specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground. A diode can be added to either P or N.

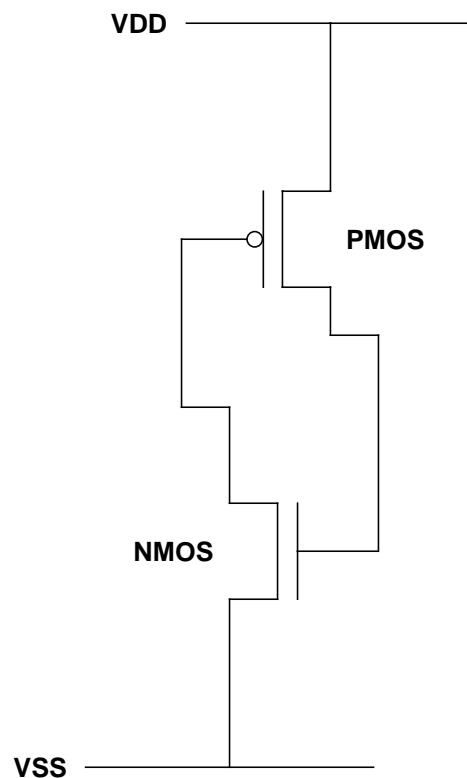
Fill Cells

The library contains several FILL cells: FILL1, FILL2, FILL4, FILL8, FILL16, FILL32, FILL64. The number appended to "FILL" in the cell name denotes the width of the cell in tracks.

During place and route, the FILL cells are used to connect power and ground rails across an area containing no cells. The FILL cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

FILLCAP Cells

FILLCAPs function as FILL cells. Inside the FILLCAP, PMOS and NMOS devices form decoupling capacitors between the VDD and VSS rails, reducing ground bounce in the power grids.



Low-Power (XL) Cells

The library contains a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

TIEHI/LO Cells

The library contains a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

Delay Cells

The library contains delay cells that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

Reading the Standard Cell Datasheet

Please refer to the sample datasheet for DFF on pages 28 and 29 for the arrangement of each of the following datasheet sections. Datasheet titles reference standard Artisan cell names. Cell names for your specific library are reflected in the cell size table on each datasheet.

NOTE: This datasheet contains sample characterization values.

1. Base Cell Name

The cell name field contains the cell name. The datasheets are presented alphabetically by cell name. The cell name presented here is the base cell name. The Cell Size table displays cell names for your specific library.

2. Cell Description

The cell description gives the function of the cell. When applicable, the equation(s) for the output pins are provided.

3. Functions

The function table gives all possible combinations of input and output signals for the cell. Table 5 defines the symbols used in datasheet function tables.

Table 5. Functions Key

Symbol	Description
0	Logic Low
1	Logic High
	High to Low Transition
	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

4. Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

5. Cell Size

This cell size table gives the height and width (um) for each drive strength of the cell.

6. Functional Schematic

The functional schematic provides a functional representation of the cell.

7. Drive Strength

The drive strength of each cell is indicated by an “X” followed by the unit strength.

8. AC Power

The AC power table shows the amount of energy consumed ($\mu\text{W}/\text{MHz}$) within the cell when the corresponding pin changes state. The energy data for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C , 1.0V, typical process, input slew of 0.018ns, and no external load at the output pins.

9. Delay

The delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF). The delays and load multiplier for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C, 1.0V, typical process, and input slew of 0.018ns.

10. Timing Constraints

The timing constraints table in the sample DFF datasheet shows the timing conditions (ns) required at 25°C, 1.0V, and typical process to maintain proper functionality. Setup constraint values are measured for 0.018ns data slew and 0.018ns clock slew. Hold constraint values are measured for 0.018ns data slew and 0.018ns clock slew. Minimum pulse width is defined to be 0.171 ns for all set/reset pins and 0.161 ns for all clock pins. These are the largest minimum pulse widths measured from all the cells in the library.

11. Pin Capacitance

The pin capacitance table shows the typical loading at the input pins of the cell (pF) for each drive strength of the cell.

▼ This datasheet contains sample characterization values. ▼

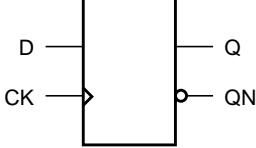


Cell Description
The DFF cell is a positive-edge-triggered, static D-type flip-flop.

Function

D	CK	Q[n+1]	QN[n+1]
0	—	0	1
1	—	1	0
x	—	Q[n]	QN[n]

Logic Symbol



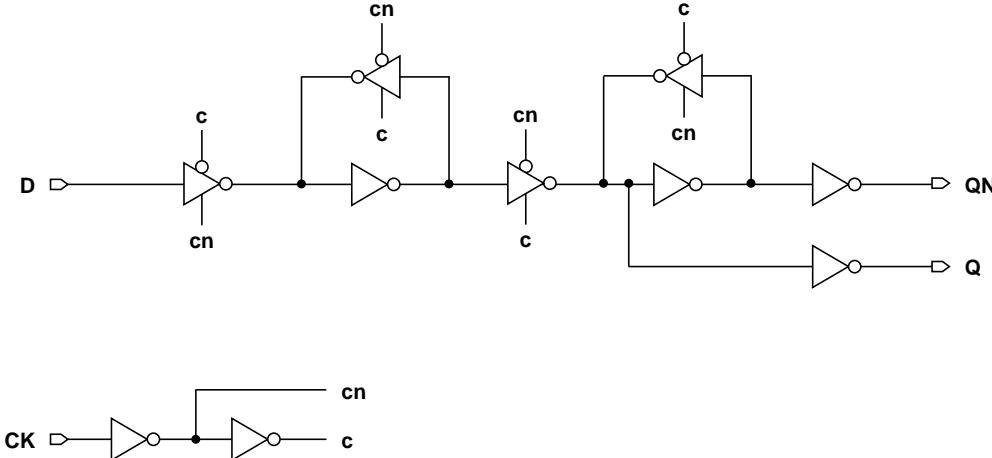
Cell Size

Drive Strength	Height (um)	Width (um)
DFFXL	3.69	7.36
DFFX1	3.69	7.36
DFFX2	3.69	8.74
DFFX4	3.69	11.50

(1) DFF
(4) 1, 4
(5) 5

(2) 2
(3) 3
(6) 6
(7) 7

Functional Schematic



Artisan SAGE-X™ Standard Cell Library Databook

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▼ This datasheet contains sample characterization values. ▼

**DFF**

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AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0056	0.0063	0.0081	0.0133
CK	0.0063	0.0068	0.0087	0.0128
Q	0.0060	0.0080	0.0124	0.0223

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0013	0.0013	0.0015	0.0023
CK	0.0015	0.0019	0.0022	0.0035

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Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1662	0.1427	0.1287	0.1105	7.8830	4.2853	1.9344	0.9666
CK → Q↓	0.1357	0.1098	0.0983	0.0920	4.3787	2.4148	1.1764	0.5884
CK → QN↑	0.1828	0.1515	0.1342	0.1292	7.8631	4.2693	1.9226	0.9616
CK → QN↓	0.2156	0.1947	0.1789	0.1547	3.9375	2.1923	1.1262	0.5569

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Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0469	0.0547	0.0391	0.0391
	setup↓ → CK	0.1094	0.1250	0.1094	0.1016
	hold↑ → CK	-0.0312	-0.0312	-0.0234	-0.0234
	hold↓ → CK	-0.0312	-0.0469	-0.0312	-0.0312
CK	minpwh	0.0933	0.0835	0.0738	0.0641
	minpwl	0.1418	0.1224	0.1127	0.0835

Base Cells

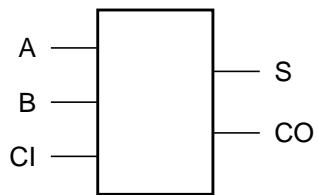
Cell Description

The ADDF cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



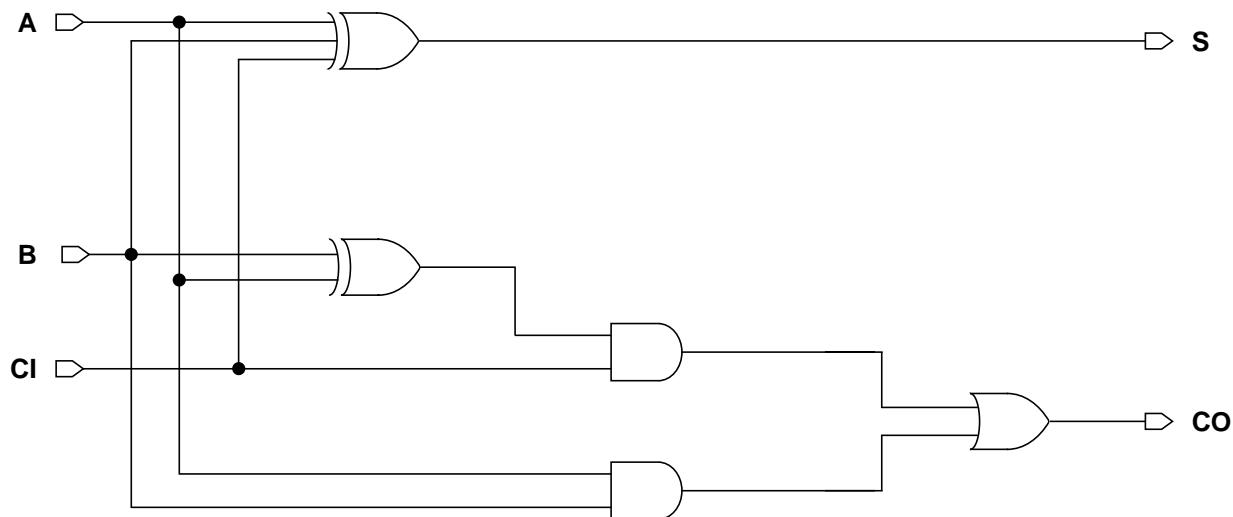
Functions

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDFXL	2.52	7.00
ADDFX1	2.52	7.00
ADDFX2	2.52	7.28
ADDFX4	2.52	7.84

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A	0.0147	0.0157	0.0177	0.0247
B	0.0181	0.0193	0.0221	0.0298
Cl	0.0085	0.0096	0.0119	0.0195

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0025	0.0025	0.0024	0.0024
B	0.0025	0.0025	0.0025	0.0024
Cl	0.0026	0.0026	0.0027	0.0027

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.1004	0.1027	0.1106	0.1285	5.7972	3.9079	2.7092	1.4091
A → S↓	0.1349	0.1418	0.1481	0.1696	5.2732	3.4988	1.8099	0.9614
B → S↑	0.1189	0.1212	0.1281	0.1428	5.8000	3.9103	2.7114	1.4143
B → S↓	0.1523	0.1592	0.1649	0.1867	5.2747	3.4999	1.8105	0.9618
Cl → S↑	0.0799	0.0833	0.0938	0.1135	5.7589	3.8945	2.7068	1.4156
Cl → S↓	0.0678	0.0742	0.0792	0.0995	5.2313	3.4929	1.8198	0.9788
A → CO↑	0.1293	0.1330	0.1429	0.1660	5.6734	3.6427	2.6720	1.3837
A → CO↓	0.1199	0.1269	0.1335	0.1535	4.9018	3.3202	1.7289	0.9197
B → CO↑	0.1466	0.1504	0.1596	0.1829	5.6727	3.6424	2.6719	1.3838
B → CO↓	0.1373	0.1432	0.1480	0.1673	4.6361	3.1647	1.6271	0.8529
Cl → CO↑	0.0674	0.0709	0.0801	0.1029	5.7862	3.7031	2.7060	1.4077
Cl → CO↓	0.0834	0.0904	0.0967	0.1146	4.9959	3.3622	1.7516	0.9333

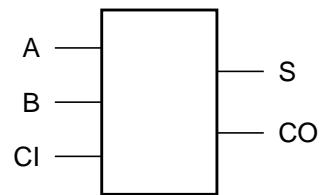
Cell Description

The ADDFH cell is a high-speed cell providing the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



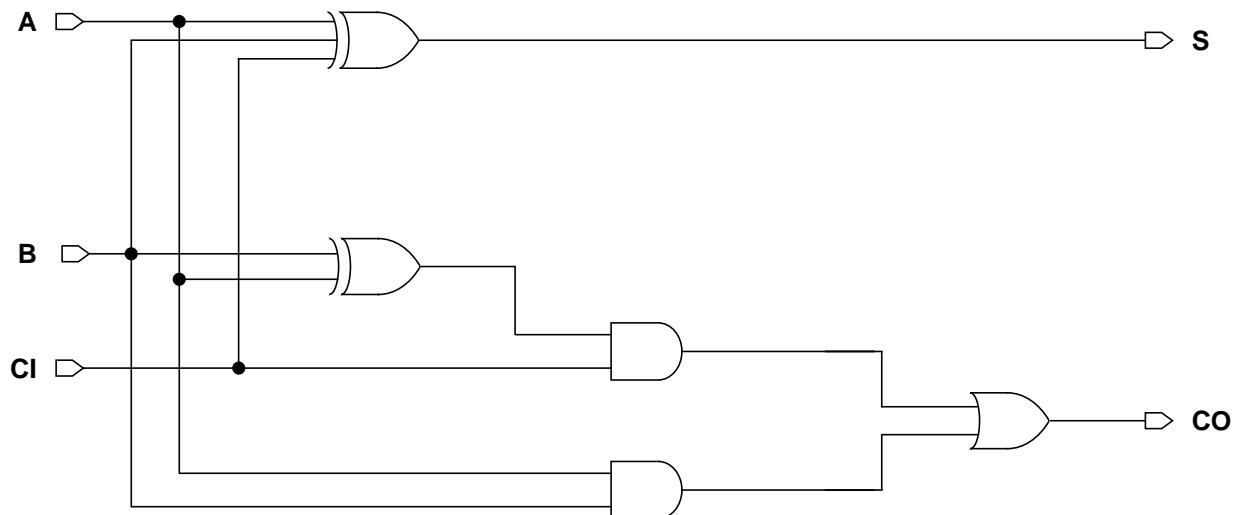
Functions

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDFHXL	2.52	7.56
ADDFHX1	2.52	8.12
ADDFHX2	2.52	10.92
ADDFHX4	2.52	17.64

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A	0.0166	0.0206	0.0308	0.0546
B	0.0145	0.0184	0.0270	0.0488
Cl	0.0091	0.0115	0.0157	0.0308

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0025	0.0030	0.0042	0.0080
B	0.0045	0.0061	0.0086	0.0157
Cl	0.0015	0.0019	0.0025	0.0046

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.1258	0.1083	0.1078	0.0973	5.7389	3.7644	2.6512	1.3655
A → S↓	0.1314	0.1190	0.1178	0.1035	4.9277	3.1873	1.5847	0.7765
B → S↑	0.0956	0.0803	0.0766	0.0754	5.7782	3.7730	2.6554	1.3679
B → S↓	0.1123	0.0968	0.0913	0.0853	4.9337	3.1882	1.5879	0.7777
Cl → S↑	0.1029	0.0876	0.0828	0.0817	5.7714	3.7760	2.6573	1.3683
Cl → S↓	0.1064	0.0929	0.0831	0.0816	4.9763	3.2047	1.5943	0.7814
A → CO↑	0.1251	0.1084	0.1097	0.0964	5.7113	3.6388	2.6511	1.3740
A → CO↓	0.1302	0.1196	0.1163	0.1045	4.7370	3.1485	1.5998	0.7834
B → CO↑	0.0839	0.0724	0.0705	0.0646	5.7228	3.6442	2.6501	1.3750
B → CO↓	0.1050	0.0937	0.0872	0.0831	4.6646	3.1116	1.5682	0.7720
Cl → CO↑	0.0563	0.0493	0.0478	0.0456	5.7443	3.6569	2.6593	1.3778
Cl → CO↓	0.0796	0.0723	0.0679	0.0639	5.1013	3.2640	1.6452	0.8073

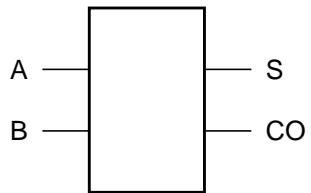
Cell Description

The ADDH cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$$S = (\bar{A} \bullet B) + (A \bullet \bar{B})$$

$$CO = A \bullet B$$

Logic Symbol



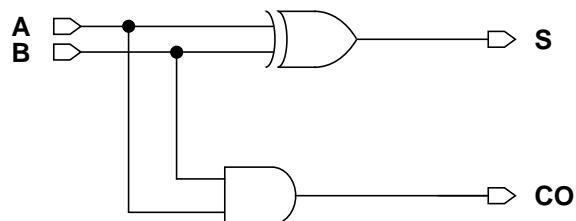
Functions

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDHXL	2.52	4.20
ADDHX1	2.52	4.20
ADDHX2	2.52	5.04
ADDHX4	2.52	7.00

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A	0.0077	0.0097	0.0164	0.0290
B	0.0051	0.0060	0.0082	0.0146

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0019	0.0028	0.0064	0.0114
B	0.0023	0.0024	0.0028	0.0042

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.0569	0.0426	0.0369	0.0332	8.3470	5.9216	3.5721	1.8224
A → S↓	0.0668	0.0591	0.0403	0.0357	6.4076	4.7370	2.3365	1.1620
B → S↑	0.0271	0.0247	0.0231	0.0245	8.3944	5.8719	3.6109	1.8267
B → S↓	0.0299	0.0316	0.0359	0.0341	6.1003	4.5589	2.2413	1.1193
A → CO↑	0.0364	0.0401	0.0361	0.0356	5.4715	3.5919	2.5932	1.3218
A → CO↓	0.0503	0.0581	0.0493	0.0453	4.5367	3.0813	1.5666	0.7688
B → CO↑	0.0362	0.0395	0.0358	0.0351	5.4861	3.5925	2.5900	1.3209
B → CO↓	0.0464	0.0533	0.0455	0.0414	4.5295	3.0676	1.5559	0.7635

Cell Description

The AND2 cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B)$$

Logic Symbol



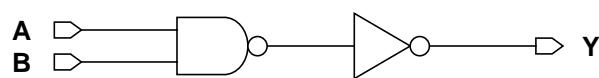
Functions

A	B	Y
0	x	0
x	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND2XL	2.52	1.40
AND2X1	2.52	1.40
AND2X2	2.52	1.40
AND2X4	2.52	2.24
AND2X6	2.52	2.80
AND2X8	2.52	3.92

Functional Schematic



AC Power

Pin	Power (μ W/MHz)					
	XL	X1	X2	X4	X6	X8
A	0.0025	0.0030	0.0041	0.0071	0.0104	0.0141
B	0.0029	0.0034	0.0047	0.0082	0.0119	0.0162

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0010	0.0011	0.0014	0.0024	0.0033	0.0047
B	0.0011	0.0011	0.0014	0.0025	0.0036	0.0046

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0373	0.0400	0.0366	0.0328	0.0328	0.0326
A → Y↓	0.0452	0.0522	0.0458	0.0414	0.0412	0.0410
B → Y↑	0.0398	0.0423	0.0388	0.0347	0.0348	0.0343
B → Y↓	0.0518	0.0588	0.0520	0.0456	0.0455	0.0464

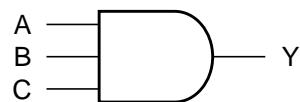
Description	K _{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	5.5570	3.5844	2.6358	1.3542	0.9128	0.6915
A → Y↓	4.0776	3.0595	1.5330	0.7542	0.4970	0.3713
B → Y↑	5.5594	3.5860	2.6348	1.3545	0.9130	0.6917
B → Y↓	4.1135	3.0774	1.5423	0.7561	0.4982	0.3735

Cell Description

The AND3 cell provides the logical AND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B \bullet C)$$

Logic Symbol



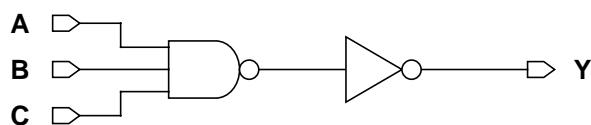
Functions

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND3XL	2.52	1.68
AND3X1	2.52	1.68
AND3X2	2.52	1.68
AND3X4	2.52	3.08
AND3X6	2.52	3.64
AND3X8	2.52	5.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X4	X6	X8
A	0.0030	0.0035	0.0046	0.0079	0.0113	0.0154
B	0.0033	0.0039	0.0053	0.0092	0.0133	0.0180
C	0.0037	0.0044	0.0060	0.0107	0.0152	0.0205

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0010	0.0011	0.0015	0.0026	0.0035	0.0057
B	0.0011	0.0011	0.0014	0.0027	0.0039	0.0051
C	0.0011	0.0011	0.0015	0.0032	0.0040	0.0050

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0559	0.0508	0.0459	0.0393	0.0391	0.0395
A → Y↓	0.0574	0.0626	0.0522	0.0468	0.0454	0.0446
B → Y↑	0.0593	0.0541	0.0489	0.0428	0.0433	0.0428
B → Y↓	0.0600	0.0682	0.0593	0.0527	0.0515	0.0531
C → Y↑	0.0616	0.0563	0.0511	0.0455	0.0458	0.0444
C → Y↓	0.0648	0.0742	0.0652	0.0575	0.0562	0.0583

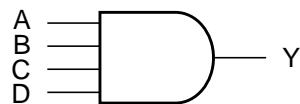
Description	K _{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	5.7513	3.6360	2.6536	1.3645	0.9186	0.6921
A → Y↓	4.2060	3.1014	1.5476	0.7602	0.4996	0.3738
B → Y↑	5.7526	3.6363	2.6546	1.3645	0.9182	0.6921
B → Y↓	4.2122	3.1197	1.5626	0.7648	0.5021	0.3784
C → Y↑	5.7539	3.6370	2.6542	1.3646	0.9187	0.6922
C → Y↓	4.2501	3.1405	1.5730	0.7671	0.5044	0.3812

Cell Description

The AND4 cell provides the logical AND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B \bullet C \bullet D)$$

Logic Symbol



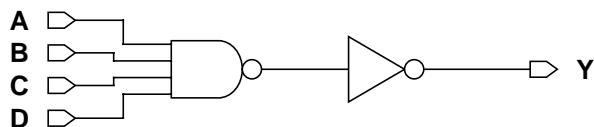
Functions

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND4XL	2.52	2.24
AND4X1	2.52	2.24
AND4X2	2.52	2.24
AND4X4	2.52	3.64
AND4X6	2.52	5.04
AND4X8	2.52	6.44

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X4	X6	X8
A	0.0031	0.0036	0.0049	0.0084	0.0132	0.0170
B	0.0034	0.0041	0.0056	0.0101	0.0154	0.0199
C	0.0037	0.0046	0.0064	0.0116	0.0178	0.0231
D	0.0042	0.0052	0.0073	0.0133	0.0203	0.0265

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0011	0.0012	0.0016	0.0027	0.0049	0.0060
B	0.0010	0.0012	0.0015	0.0030	0.0047	0.0059
C	0.0010	0.0011	0.0015	0.0031	0.0046	0.0063
D	0.0012	0.0013	0.0017	0.0034	0.0050	0.0069

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0678	0.0552	0.0506	0.0436	0.0457	0.0443
A → Y↓	0.0558	0.0628	0.0550	0.0482	0.0524	0.0508
B → Y↑	0.0714	0.0595	0.0553	0.0496	0.0506	0.0492
B → Y↓	0.0606	0.0704	0.0627	0.0568	0.0578	0.0563
C → Y↑	0.0745	0.0628	0.0586	0.0528	0.0539	0.0528
C → Y↓	0.0648	0.0767	0.0690	0.0629	0.0653	0.0638
D → Y↑	0.0804	0.0673	0.0621	0.0555	0.0568	0.0557
D → Y↓	0.0715	0.0849	0.0761	0.0697	0.0709	0.0699

Delays at 25°C, 1.0V, Typical Process

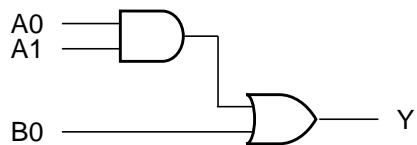
Description	K _{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	5.9564	3.6965	2.6632	1.3760	0.9235	0.7030
A → Y↓	4.1783	3.0908	1.5504	0.7606	0.5087	0.3811
B → Y↑	5.9569	3.6968	2.6633	1.3760	0.9235	0.7030
B → Y↓	4.2308	3.1203	1.5657	0.7680	0.5103	0.3824
C → Y↑	5.9572	3.6968	2.6635	1.3760	0.9233	0.7029
C → Y↓	4.2709	3.1449	1.5791	0.7746	0.5162	0.3866
D → Y↑	5.9597	3.6976	2.6639	1.3762	0.9236	0.7032
D → Y↓	4.3050	3.1678	1.5916	0.7824	0.5197	0.3898

Cell Description

The AO21 cell provides the logical OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet A1) + B0$$

Logic Symbol



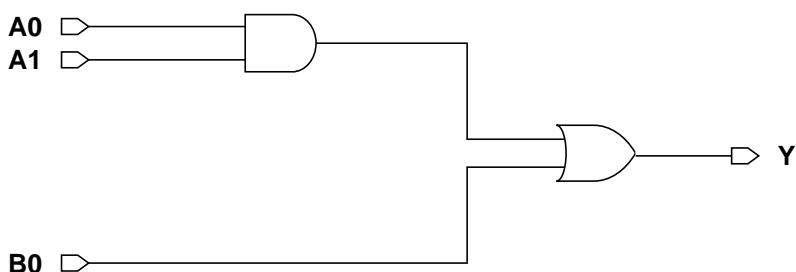
Functions

A0	A1	B0	Y
0	x	0	0
x	0	0	0
x	x	1	1
1	1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO21XL	2.52	1.96
AO21X1	2.52	1.96
AO21X2	2.52	1.96
AO21X4	2.52	2.52

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0031	0.0037	0.0051	0.0092
A1	0.0034	0.0041	0.0056	0.0101
B0	0.0031	0.0037	0.0051	0.0089

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0010	0.0011	0.0014	0.0023
A1	0.0009	0.0010	0.0013	0.0022
B0	0.0010	0.0011	0.0015	0.0023

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0417	0.0464	0.0421	0.0409	5.5369	3.5666	2.5933	1.3341
A0 → Y↓	0.0935	0.0895	0.0760	0.0675	4.8861	3.2327	1.6056	0.8100
A1 → Y↑	0.0430	0.0477	0.0436	0.0426	5.5381	3.5669	2.5931	1.3340
A1 → Y↓	0.1001	0.0943	0.0814	0.0729	4.9170	3.2410	1.6113	0.8137
B0 → Y↑	0.0285	0.0301	0.0279	0.0277	5.4141	3.4968	2.5710	1.3234
B0 → Y↓	0.0866	0.0822	0.0713	0.0635	4.9161	3.2415	1.6113	0.8137

Cell Description

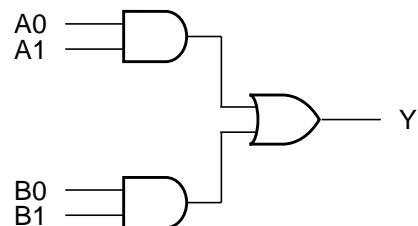
The AO22 cell provides the logical OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = (A_0 \bullet A_1) + (B_0 \bullet B_1)$$

Functions

A0	A1	B0	B1	Y
0	x	0	x	0
0	x	x	0	0
x	0	0	x	0
x	0	x	0	0
x	x	1	1	1
1	1	x	x	1

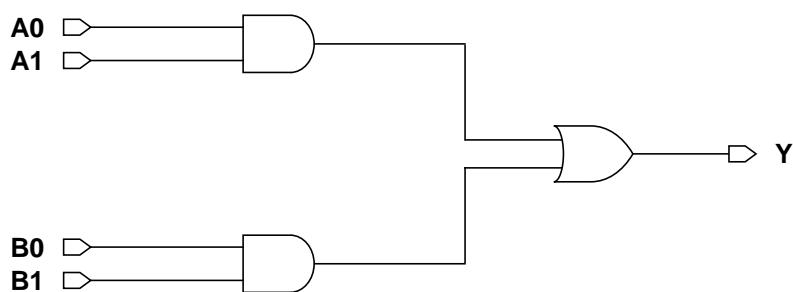
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AO22XL	2.52	2.24
AO22X1	2.52	2.24
AO22X2	2.52	2.24
AO22X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0034	0.0041	0.0054	0.0094
A1	0.0038	0.0045	0.0060	0.0104
B0	0.0040	0.0045	0.0061	0.0111
B1	0.0044	0.0048	0.0067	0.0120

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0010	0.0011	0.0014	0.0024
A1	0.0011	0.0010	0.0014	0.0024
B0	0.0010	0.0011	0.0015	0.0024
B1	0.0010	0.0009	0.0013	0.0023

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0421	0.0429	0.0401	0.0394	5.5554	3.5343	2.5749	1.3359
A0 → Y↓	0.0958	0.1036	0.0768	0.0667	5.0673	3.4147	1.7430	0.8244
A1 → Y↑	0.0444	0.0451	0.0424	0.0412	5.5567	3.5348	2.5754	1.3365
A1 → Y↓	0.1061	0.1124	0.0842	0.0721	5.1148	3.4331	1.7509	0.8280
B0 → Y↑	0.0486	0.0510	0.0484	0.0478	5.6409	3.5837	2.5938	1.3440
B0 → Y↓	0.1156	0.1282	0.0933	0.0811	5.0779	3.4221	1.7442	0.8253
B1 → Y↑	0.0502	0.0523	0.0500	0.0495	5.6430	3.5841	2.5937	1.3441
B1 → Y↓	0.1224	0.1330	0.0986	0.0856	5.1192	3.4328	1.7510	0.8280

Cell Description

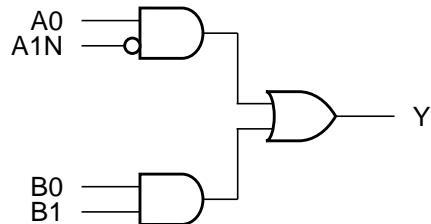
The AO2B2 cell provides the logical OR of two AND group consisting of two inputs each: (A0, A1N) and (B0, B1). The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet \overline{A1N}) + (B0 \bullet B1)$$

Functions

A0	A1N	B0	B1	Y
1	0	x	x	1
x	x	1	1	1
0	x	0	x	0
x	1	0	x	0
0	x	x	0	0
x	1	x	0	0

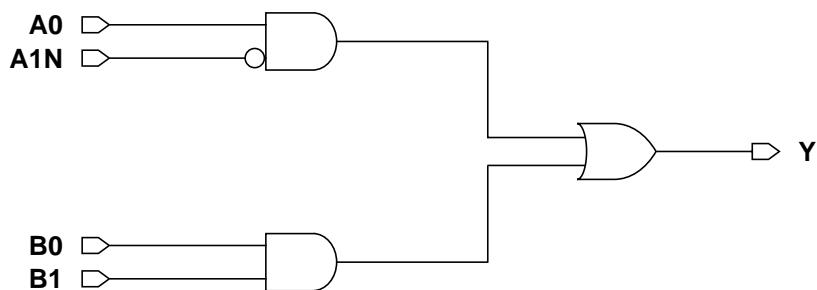
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AO2B2XL	2.52	2.80
AO2B2X1	2.52	2.80
AO2B2X2	2.52	2.80
AO2B2X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0035	0.0042	0.0056	0.0097
A1N	0.0040	0.0047	0.0063	0.0109
B0	0.0041	0.0048	0.0065	0.0115
B1	0.0044	0.0051	0.0070	0.0124

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0007	0.0007	0.0009	0.0016
A1N	0.0009	0.0009	0.0012	0.0013
B0	0.0010	0.0010	0.0014	0.0024
B1	0.0009	0.0009	0.0013	0.0023

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0436	0.0461	0.0434	0.0417	5.6508	3.6180	2.6322	1.3401
A0 → Y↓	0.0961	0.1093	0.0783	0.0685	5.2163	3.5049	1.6676	0.8098
A1N → Y↑	0.0753	0.0779	0.0725	0.0766	5.6541	3.6191	2.6327	1.3409
A1N → Y↓	0.1171	0.1303	0.0957	0.0882	5.2609	3.5263	1.6760	0.8131
B0 → Y↑	0.0516	0.0544	0.0518	0.0493	5.7556	3.6693	2.6494	1.3464
B0 → Y↓	0.1252	0.1384	0.0973	0.0831	5.2389	3.5187	1.6727	0.8108
B1 → Y↑	0.0530	0.0558	0.0533	0.0510	5.7556	3.6691	2.6494	1.3465
B1 → Y↓	0.1302	0.1432	0.1014	0.0876	5.2631	3.5269	1.6766	0.8133

Cell Description

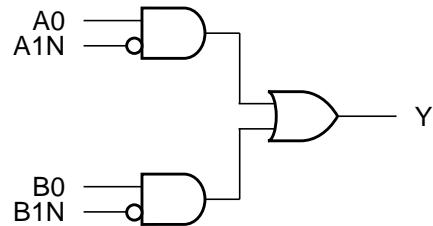
The AO2B2B cell provides the logical OR of two AND group consisting of two inputs each: (A0, A1N) and (B0, B1N). The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet \overline{A1N}) + (B0 \bullet \overline{B1N})$$

Functions

A0	A1N	B0	B1N	Y
0	x	0	x	0
0	x	x	1	0
x	1	0	x	0
x	1	x	1	0
x	x	1	0	1
1	0	x	x	1

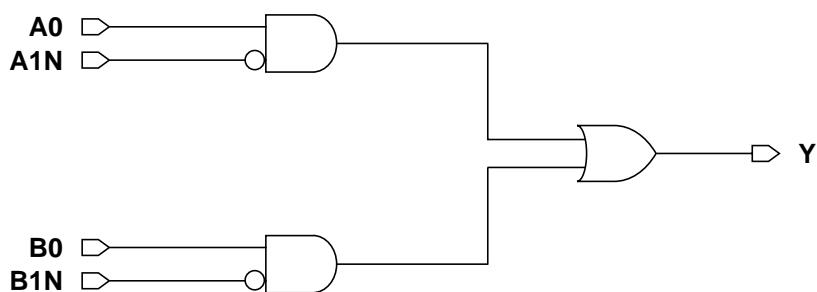
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AO2B2BXL	2.52	3.36
AO2B2BX1	2.52	3.36
AO2B2BX2	2.52	3.36
AO2B2BX4	2.52	3.92

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0035	0.0042	0.0056	0.0096
A1N	0.0040	0.0047	0.0064	0.0109
B0	0.0041	0.0049	0.0066	0.0115
B1N	0.0044	0.0051	0.0070	0.0125

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0010	0.0010	0.0015	0.0024
A1N	0.0009	0.0009	0.0012	0.0012
B0	0.0010	0.0010	0.0015	0.0024
B1N	0.0011	0.0010	0.0013	0.0014

Delays at 25°C, 1.0V, Typical Process

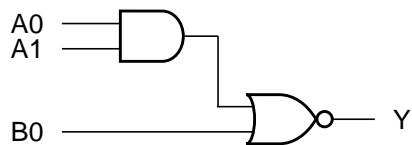
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0434	0.0460	0.0437	0.0414	5.6496	3.6174	2.6314	1.3525
A0 → Y↓	0.0954	0.1086	0.0782	0.0683	5.2030	3.4983	1.6649	0.8069
A1N → Y↑	0.0751	0.0778	0.0733	0.0758	5.6540	3.6187	2.6312	1.3526
A1N → Y↓	0.1161	0.1291	0.0955	0.0876	5.2451	3.5164	1.6726	0.8102
B0 → Y↑	0.0503	0.0530	0.0510	0.0487	5.7465	3.6641	2.6471	1.3583
B0 → Y↓	0.1235	0.1367	0.0966	0.0829	5.2191	3.5063	1.6681	0.8074
B1N → Y↑	0.0805	0.0832	0.0789	0.0816	5.7440	3.6634	2.6471	1.3584
B1N → Y↓	0.1408	0.1537	0.1117	0.1016	5.2441	3.5166	1.6722	0.8101

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0}$$

Logic Symbol



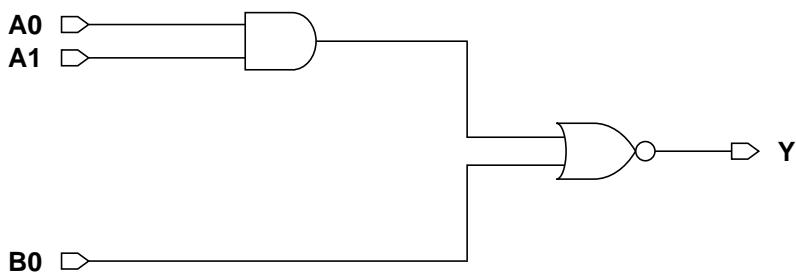
Functions

A0	A1	B0	Y
0	x	0	1
x	0	0	1
x	x	1	0
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21XL	2.52	1.40
AOI21X1	2.52	1.40
AOI21X2	2.52	1.68
AOI21X3	2.52	2.52
AOI21X4	2.52	2.52
AOI21X6	2.52	3.64
AOI21X8	2.52	4.76

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)						
	XL	X1	X2	X3	X4	X6	X8
A0	0.0021	0.0030	0.0043	0.0067	0.0085	0.0125	0.0161
A1	0.0024	0.0034	0.0052	0.0079	0.0102	0.0150	0.0196
B0	0.0019	0.0026	0.0039	0.0061	0.0076	0.0114	0.0146

Pin Capacitance

Pin	Capacitance (pF)						
	XL	X1	X2	X3	X4	X6	X8
A0	0.0013	0.0017	0.0024	0.0038	0.0049	0.0069	0.0090
A1	0.0012	0.0016	0.0023	0.0034	0.0043	0.0068	0.0092
B0	0.0013	0.0018	0.0024	0.0036	0.0044	0.0064	0.0086

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	XL	X1	X2	X3	X4	X6	X8
A0 → Y↑	0.0331	0.0285	0.0300	0.0320	0.0297	0.0296	0.0289
A0 → Y↓	0.0235	0.0226	0.0168	0.0165	0.0162	0.0156	0.0150
A1 → Y↑	0.0360	0.0325	0.0348	0.0378	0.0350	0.0357	0.0348
A1 → Y↓	0.0248	0.0243	0.0184	0.0178	0.0175	0.0172	0.0167
B0 → Y↑	0.0250	0.0235	0.0257	0.0281	0.0254	0.0264	0.0254
B0 → Y↓	0.0119	0.0117	0.0098	0.0095	0.0098	0.0094	0.0091

Description	K _{load} (ns/pF)						
	XL	X1	X2	X3	X4	X6	X8
A0 → Y↑	11.1928	7.1809	5.2865	3.7357	2.6914	1.8822	1.4239
A0 → Y↓	7.1340	4.9488	2.4697	1.6044	1.2192	0.8075	0.6027
A1 → Y↑	10.9548	7.2769	5.2153	3.7967	2.7285	1.8910	1.4122
A1 → Y↓	7.1325	4.9484	2.4693	1.6052	1.2189	0.8071	0.6029
B0 → Y↑	11.0036	7.2958	5.2248	3.8041	2.7332	1.8938	1.4146
B0 → Y↓	4.1821	2.9170	1.5471	0.9494	0.8131	0.5173	0.3792

Cell Description

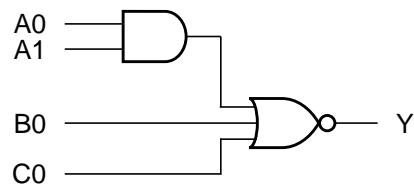
The AOI211 cell provides the logical inverted OR of one AND group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1)} + B_0 + C_0$$

Functions

A0	A1	B0	C0	Y
0	x	0	0	1
x	0	0	0	1
x	x	x	1	0
x	x	1	x	0
1	1	x	x	0

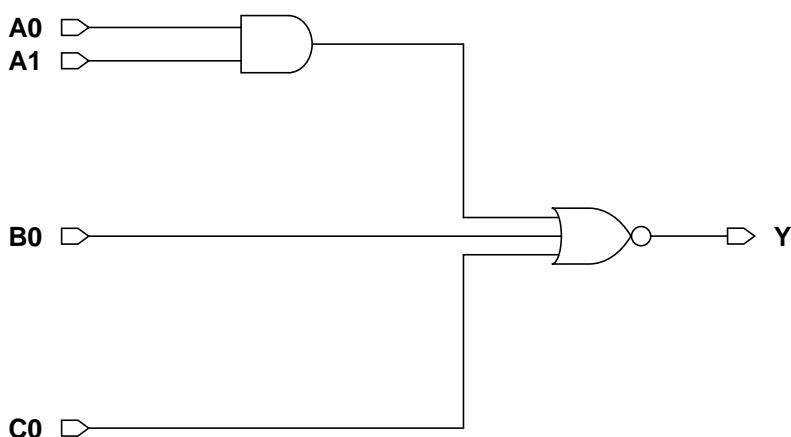
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AOI211XL	2.52	1.68
AOI211X1	2.52	1.68
AOI211X2	2.52	1.68
AOI211X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0031	0.0042	0.0059	0.0114
A1	0.0034	0.0046	0.0067	0.0130
B0	0.0024	0.0030	0.0047	0.0090
C0	0.0028	0.0036	0.0055	0.0106

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0014	0.0018	0.0025	0.0048
A1	0.0012	0.0016	0.0022	0.0043
B0	0.0013	0.0017	0.0024	0.0045
C0	0.0013	0.0017	0.0024	0.0046

Delays at 25°C, 1.0V, Typical Process

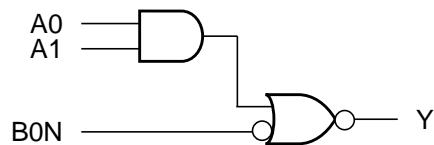
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0578	0.0506	0.0530	0.0527	16.9468	10.9107	8.0132	4.2321
A0 → Y↓	0.0253	0.0271	0.0195	0.0183	6.6292	4.9971	2.4905	1.2294
A1 → Y↑	0.0627	0.0548	0.0599	0.0611	16.7121	10.7740	7.9194	4.2703
A1 → Y↓	0.0265	0.0285	0.0210	0.0195	6.6266	4.9971	2.4903	1.2294
B0 → Y↑	0.0435	0.0360	0.0418	0.0413	16.7909	10.8048	7.9376	4.2781
B0 → Y↓	0.0139	0.0131	0.0108	0.0100	4.1865	2.9169	1.4609	0.7140
C0 → Y↑	0.0544	0.0466	0.0523	0.0535	16.7590	10.7929	7.9294	4.2750
C0 → Y↓	0.0158	0.0151	0.0120	0.0115	4.1406	2.8805	1.4425	0.7219

Cell Description

The AOI21B cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1)} + \overline{B_{0N}}$$

Logic Symbol



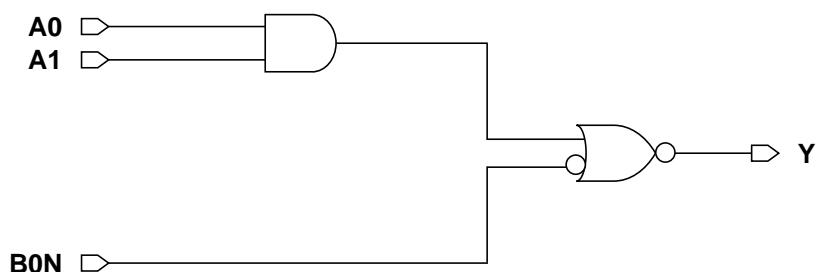
Functions

A0	A1	B0N	Y
x	x	0	0
x	0	1	1
0	x	1	1
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21BXL	2.52	2.24
AOI21BX1	2.52	2.24
AOI21BX2	2.52	2.24
AOI21BX4	2.52	2.52

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0039	0.0044	0.0058	0.0088
A1	0.0036	0.0041	0.0054	0.0083
B0N	0.0024	0.0028	0.0039	0.0069

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0010	0.0010	0.0013	0.0013
A1	0.0011	0.0011	0.0014	0.0013
B0N	0.0010	0.0010	0.0013	0.0021

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0786	0.0814	0.0727	0.0794	5.6276	3.6069	2.6494	1.3626
A0 → Y↓	0.0754	0.0799	0.0683	0.0683	4.5904	3.1507	1.5673	0.7645
A1 → Y↑	0.0725	0.0752	0.0668	0.0731	5.6253	3.6058	2.6498	1.3622
A1 → Y↓	0.0742	0.0787	0.0670	0.0670	4.5903	3.1507	1.5673	0.7646
B0N → Y↑	0.0374	0.0397	0.0373	0.0373	5.6206	3.6040	2.6495	1.3626
B0N → Y↓	0.0531	0.0572	0.0497	0.0435	4.6119	3.1602	1.5723	0.7646

Cell Description

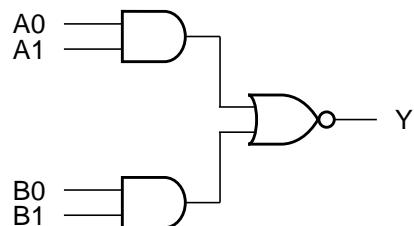
The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1)}$$

Functions

A0	A1	B0	B1	Y
0	x	0	x	1
0	x	x	0	1
x	0	0	x	1
x	0	x	0	1
x	x	1	1	0
1	1	x	x	0

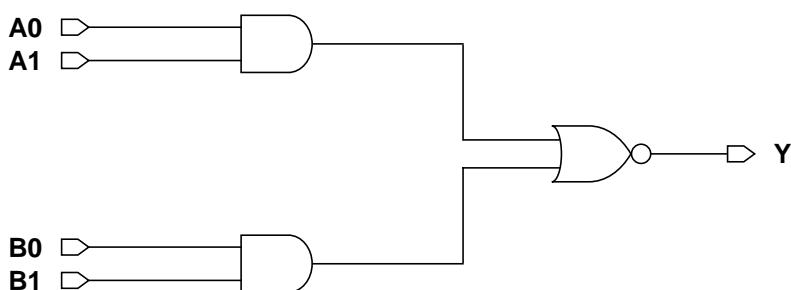
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AOI22XL	2.52	1.68
AOI22X1	2.52	1.96
AOI22X2	2.52	1.96
AOI22X4	2.52	3.36

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0021	0.0029	0.0043	0.0082
A1	0.0025	0.0033	0.0051	0.0098
B0	0.0028	0.0042	0.0059	0.0112
B1	0.0031	0.0046	0.0067	0.0129

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0018	0.0025	0.0045
A1	0.0012	0.0017	0.0024	0.0045
B0	0.0013	0.0017	0.0024	0.0044
B1	0.0012	0.0016	0.0023	0.0047

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0279	0.0264	0.0290	0.0286	11.1529	7.2503	5.3299	2.7422
A0 → Y↓	0.0191	0.0190	0.0143	0.0142	7.0202	4.8817	2.4531	1.2925
A1 → Y↑	0.0318	0.0299	0.0340	0.0354	10.9721	7.1515	5.2526	2.8311
A1 → Y↓	0.0210	0.0209	0.0162	0.0162	7.0234	4.8830	2.4535	1.2924
B0 → Y↑	0.0465	0.0407	0.0424	0.0421	11.2370	7.2951	5.3598	2.8714
B0 → Y↓	0.0325	0.0312	0.0217	0.0203	7.1087	4.9182	2.4615	1.2152
B1 → Y↑	0.0488	0.0431	0.0466	0.0477	10.9482	7.1425	5.2486	2.8297
B1 → Y↓	0.0338	0.0327	0.0233	0.0221	7.1045	4.9189	2.4617	1.2155

Cell Description

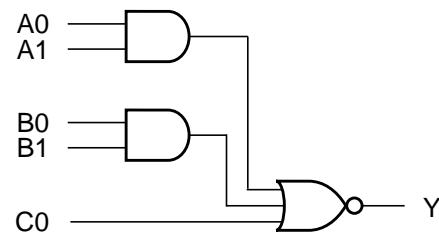
The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1) + (B_0 \bullet B_1) + C_0}$$

Functions

A0	A1	B0	B1	C0	Y
0	x	0	x	0	1
0	x	x	0	0	1
x	0	0	x	0	1
x	0	x	0	0	1
x	x	x	x	1	0
x	x	1	1	x	0
1	1	x	x	x	0

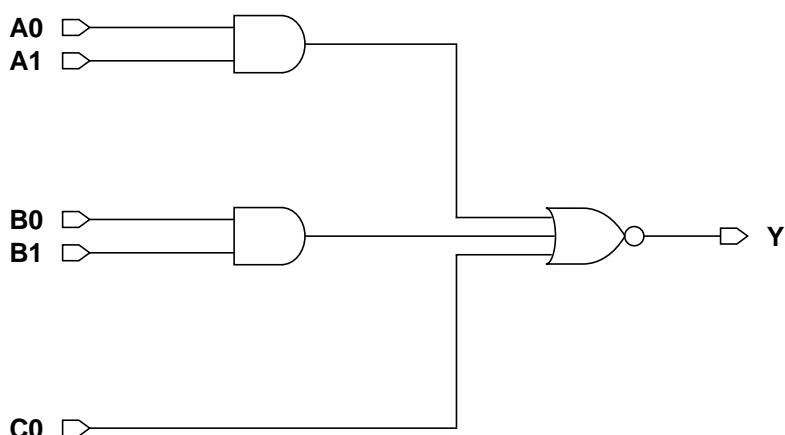
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AOI221XL	2.52	2.24
AOI221X1	2.52	2.52
AOI221X2	2.52	2.52
AOI221X4	2.52	4.48

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0031	0.0043	0.0063	0.0114
A1	0.0033	0.0047	0.0071	0.0132
B0	0.0038	0.0054	0.0077	0.0142
B1	0.0041	0.0058	0.0086	0.0160
C0	0.0028	0.0037	0.0059	0.0107

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0044
A1	0.0013	0.0017	0.0023	0.0045
B0	0.0013	0.0017	0.0023	0.0043
B1	0.0012	0.0016	0.0023	0.0046
C0	0.0014	0.0017	0.0024	0.0044

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0621	0.0563	0.0613	0.0581	16.1696	10.6560	7.8132	4.1704
A0 → Y↓	0.0279	0.0271	0.0200	0.0176	7.0334	4.8431	2.4371	1.2028
A1 → Y↑	0.0687	0.0625	0.0694	0.0660	16.4002	10.7279	7.8771	4.1210
A1 → Y↓	0.0293	0.0289	0.0215	0.0191	7.0327	4.8429	2.4370	1.2028
B0 → Y↑	0.0747	0.0676	0.0720	0.0690	16.4228	10.7135	7.8694	4.1804
B0 → Y↓	0.0321	0.0325	0.0226	0.0197	7.3295	5.0330	2.5185	1.2427
B1 → Y↑	0.0800	0.0725	0.0798	0.0770	16.3925	10.7220	7.8758	4.1213
B1 → Y↓	0.0333	0.0339	0.0242	0.0215	7.3308	5.0326	2.5188	1.2428
C0 → Y↑	0.0454	0.0405	0.0497	0.0468	16.4657	10.7468	7.8915	4.1294
C0 → Y↓	0.0143	0.0137	0.0112	0.0101	4.2699	2.9178	1.4641	0.7221

Cell Description

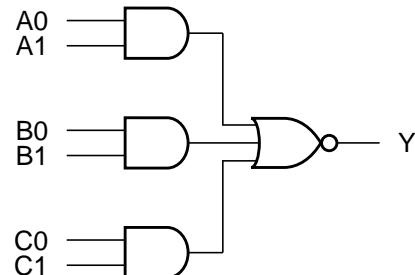
The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1) + (B_0 \bullet B_1) + (C_0 \bullet C_1)}$$

Functions

A0	A1	B0	B1	C0	C1	Y
0	x	0	x	0	x	1
0	x	0	x	x	0	1
0	x	x	0	0	x	1
0	x	x	0	x	0	1
x	0	0	x	0	x	1
x	0	0	x	x	0	1
x	0	x	0	0	x	1
x	0	x	0	x	0	1
x	x	x	x	1	1	0
x	x	1	1	x	x	0
1	1	x	x	x	x	0

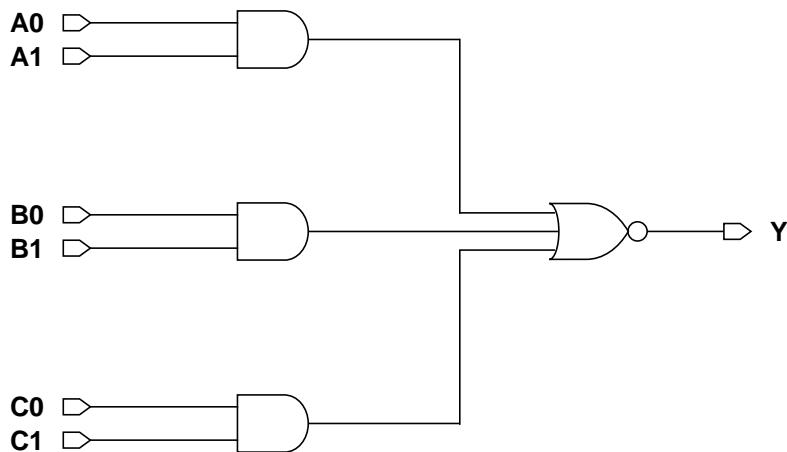
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AOI222XL	2.52	2.52
AOI222X1	2.52	2.80
AOI222X2	2.52	2.80
AOI222X4	2.52	5.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0031	0.0041	0.0062	0.0118
A1	0.0035	0.0045	0.0069	0.0134
B0	0.0039	0.0053	0.0077	0.0145
B1	0.0042	0.0057	0.0085	0.0164
C0	0.0047	0.0065	0.0091	0.0174
C1	0.0050	0.0069	0.0099	0.0191

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0045
A1	0.0013	0.0017	0.0021	0.0047
B0	0.0014	0.0017	0.0023	0.0044
B1	0.0013	0.0016	0.0023	0.0047
C0	0.0013	0.0016	0.0023	0.0044
C1	0.0013	0.0016	0.0023	0.0047

Delays at 25°C, 1.0V, Typical Process

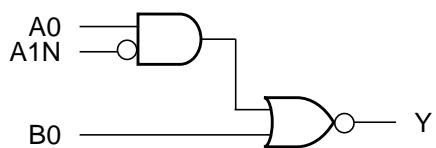
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0492	0.0437	0.0520	0.0508	16.3732	10.6598	7.8646	4.0563
A0 → Y↓	0.0240	0.0225	0.0188	0.0159	7.0250	4.8757	2.8215	1.2109
A1 → Y↑	0.0551	0.0485	0.0584	0.0613	16.1330	10.5671	7.7863	4.1439
A1 → Y↓	0.0262	0.0243	0.0213	0.0176	7.0283	4.8762	2.8215	1.2110
B0 → Y↑	0.0853	0.0727	0.0783	0.0778	16.4410	10.7337	7.9049	4.1876
B0 → Y↓	0.0363	0.0336	0.0235	0.0218	7.0106	4.8229	2.4251	1.2023
B1 → Y↑	0.0890	0.0770	0.0850	0.0861	16.1171	10.5600	7.7827	4.1423
B1 → Y↓	0.0377	0.0353	0.0251	0.0235	7.0093	4.8226	2.4251	1.2023
C0 → Y↑	0.0961	0.0829	0.0879	0.0890	16.1379	10.6127	7.8086	4.1992
C0 → Y↓	0.0456	0.0429	0.0288	0.0266	7.2981	4.9934	2.4934	1.2325
C1 → Y↑	0.1018	0.0881	0.0959	0.0967	16.1128	10.5576	7.7837	4.1410
C1 → Y↓	0.0471	0.0446	0.0305	0.0285	7.2948	4.9934	2.4933	1.2323

Cell Description

The AOI2B1 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_{1N})} + B_0$$

Logic Symbol



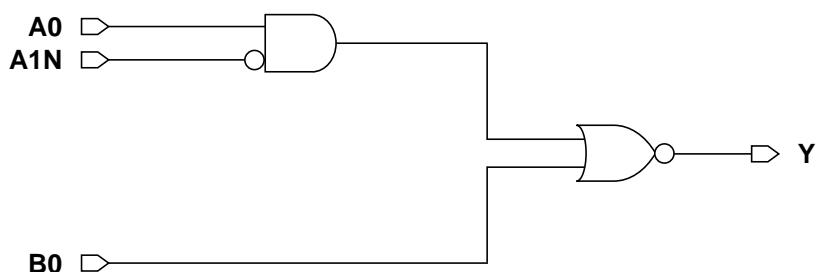
Functions

A0	A1N	B0	Y
0	x	0	1
x	1	0	1
x	x	1	0
1	0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2B1XL	2.52	1.96
AOI2B1X1	2.52	1.96
AOI2B1X2	2.52	2.24
AOI2B1X4	2.52	3.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0023	0.0030	0.0042	0.0084
A1N	0.0027	0.0035	0.0052	0.0106
B0	0.0019	0.0025	0.0039	0.0078

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0048
A1N	0.0011	0.0011	0.0013	0.0020
B0	0.0013	0.0017	0.0024	0.0046

Delays at 25°C, 1.0V, Typical Process

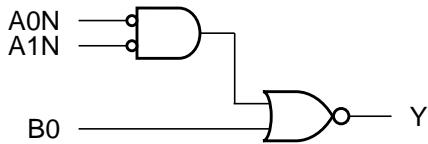
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0318	0.0286	0.0299	0.0301	11.1434	7.1665	5.2873	2.6984
A0 → Y↓	0.0222	0.0223	0.0164	0.0162	6.9909	4.8774	2.4392	1.2207
A1N → Y↑	0.0486	0.0473	0.0490	0.0538	10.9258	7.1632	5.2151	2.7344
A1N → Y↓	0.0561	0.0596	0.0501	0.0468	7.0149	4.8912	2.4481	1.2238
B0 → Y↑	0.0251	0.0226	0.0254	0.0259	10.9846	7.1791	5.2264	2.7396
B0 → Y↓	0.0119	0.0115	0.0095	0.0093	4.1784	2.9115	1.4599	0.7212

Cell Description

The AOI2BB1 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N})} + B0$$

Logic Symbol



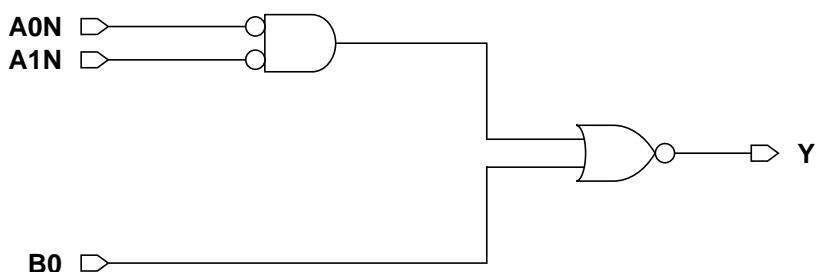
Functions

A0N	A1N	B0	Y
1	x	0	1
x	1	0	1
x	x	1	0
0	0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2BB1XL	2.52	1.68
AOI2BB1X1	2.52	1.68
AOI2BB1X2	2.52	1.68
AOI2BB1X4	2.52	2.52

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0N	0.0029	0.0034	0.0046	0.0076
A1N	0.0032	0.0038	0.0050	0.0084
B0	0.0018	0.0025	0.0036	0.0071

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0012	0.0012	0.0015	0.0022
A1N	0.0012	0.0012	0.0014	0.0021
B0	0.0012	0.0016	0.0023	0.0046

Delays at 25°C, 1.0V, Typical Process

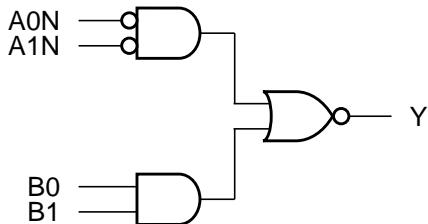
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0389	0.0381	0.0368	0.0369	11.2549	7.1641	5.2613	2.7041
A0N → Y↓	0.0589	0.0661	0.0688	0.0582	4.5989	3.1637	1.5984	0.7693
A1N → Y↑	0.0406	0.0398	0.0380	0.0388	11.2639	7.1691	5.2634	2.7062
A1N → Y↓	0.0639	0.0710	0.0736	0.0629	4.5988	3.1637	1.5977	0.7692
B0 → Y↑	0.0262	0.0238	0.0251	0.0245	11.2240	7.1482	5.2541	2.7023
B0 → Y↓	0.0130	0.0130	0.0105	0.0101	4.1296	2.9056	1.4578	0.7239

Cell Description

The AOI2BB2 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and one AND group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(A0N \bullet A1N)} + (B0 \bullet B1)$$

Logic Symbol



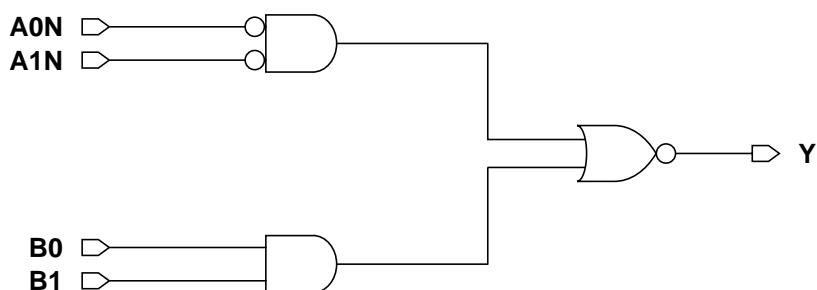
Functions

A0N	A1N	B0	B1	Y
1	x	0	x	1
1	x	x	0	1
x	1	0	x	1
x	1	x	0	1
x	x	1	1	0
0	0	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2BB2XL	2.52	2.24
AOI2BB2X1	2.52	2.24
AOI2BB2X2	2.52	2.24
AOI2BB2X4	2.52	3.64

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0N	0.0029	0.0033	0.0045	0.0077
A1N	0.0031	0.0036	0.0048	0.0085
B0	0.0023	0.0031	0.0042	0.0082
B1	0.0026	0.0035	0.0050	0.0099

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0013	0.0013	0.0015	0.0022
A1N	0.0011	0.0011	0.0013	0.0022
B0	0.0013	0.0017	0.0023	0.0044
B1	0.0012	0.0016	0.0023	0.0044

Delays at 25°C, 1.0V, Typical Process

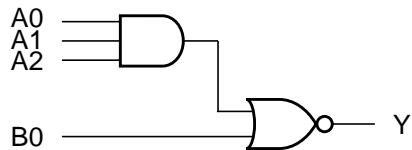
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0349	0.0344	0.0322	0.0338	8.2284	5.2901	3.8870	2.0390
A0N → Y↓	0.0579	0.0639	0.0658	0.0566	4.5160	3.0955	1.5782	0.7620
A1N → Y↑	0.0372	0.0369	0.0341	0.0359	8.2405	5.2958	3.8897	2.0404
A1N → Y↓	0.0615	0.0675	0.0695	0.0614	4.5164	3.0953	1.5781	0.7618
B0 → Y↑	0.0332	0.0296	0.0297	0.0293	11.1617	7.1800	5.2782	2.7223
B0 → Y↓	0.0230	0.0225	0.0161	0.0154	7.0340	4.8752	2.4390	1.2143
B1 → Y↑	0.0360	0.0322	0.0343	0.0363	10.9368	7.0342	5.1796	2.8153
B1 → Y↓	0.0241	0.0237	0.0177	0.0171	7.0328	4.8763	2.4389	1.2146

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1 \bullet A_2) + B_0}$$

Logic Symbol



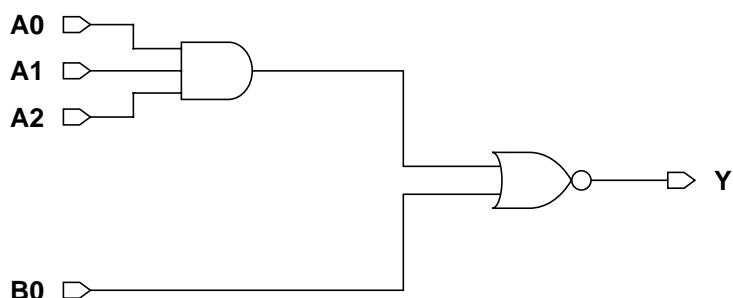
Functions

A0	A1	A2	B0	Y
0	x	x	0	1
x	0	x	0	1
x	x	0	0	1
x	x	x	1	0
1	1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI31XL	2.52	1.68
AOI31X1	2.52	1.68
AOI31X2	2.52	1.96
AOI31X4	2.52	3.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0023	0.0032	0.0045	0.0092
A1	0.0026	0.0036	0.0054	0.0108
A2	0.0029	0.0041	0.0063	0.0125
B0	0.0022	0.0030	0.0048	0.0095

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0023	0.0051
A1	0.0013	0.0017	0.0023	0.0047
A2	0.0012	0.0016	0.0023	0.0042
B0	0.0013	0.0017	0.0024	0.0042

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0336	0.0305	0.0319	0.0331	11.2493	7.2288	5.3396	2.8129
A0 → Y↓	0.0321	0.0321	0.0227	0.0224	9.9408	6.9379	3.4737	1.7118
A1 → Y↑	0.0376	0.0349	0.0375	0.0395	11.2504	7.3841	5.3548	2.8515
A1 → Y↓	0.0351	0.0353	0.0261	0.0254	9.9427	6.9368	3.4741	1.7127
A2 → Y↑	0.0400	0.0373	0.0420	0.0443	10.9863	7.2024	5.2532	2.8627
A2 → Y↓	0.0367	0.0370	0.0280	0.0265	9.9441	6.9372	3.4746	1.7125
B0 → Y↑	0.0289	0.0261	0.0310	0.0324	11.0317	7.2196	5.2648	2.8688
B0 → Y↓	0.0117	0.0114	0.0095	0.0097	4.1909	2.9169	1.4627	0.8121

Cell Description

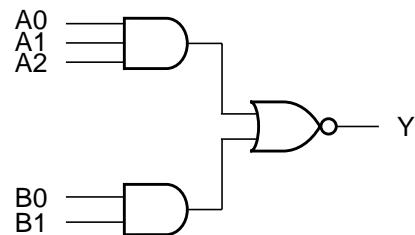
The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1 \bullet A_2) + (B_0 \bullet B_1)}$$

Functions

A0	A1	A2	B0	B1	Y
0	x	x	0	x	1
0	x	x	x	0	1
x	0	x	0	x	1
x	0	x	x	0	1
x	x	0	0	x	1
x	x	0	x	0	1
x	x	x	1	1	0
1	1	1	x	x	0

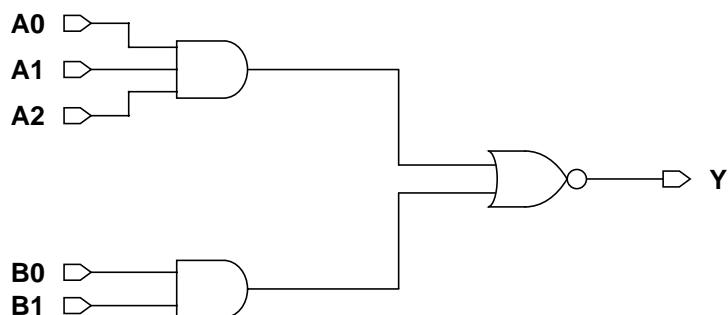
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AOI32XL	2.52	1.96
AOI32X1	2.52	2.24
AOI32X2	2.52	2.24
AOI32X4	2.52	4.20

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0030	0.0044	0.0060	0.0120
A1	0.0033	0.0048	0.0068	0.0138
A2	0.0036	0.0052	0.0077	0.0156
B0	0.0025	0.0034	0.0052	0.0104
B1	0.0028	0.0038	0.0059	0.0120

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0014	0.0017	0.0024	0.0044
A1	0.0013	0.0016	0.0023	0.0048
A2	0.0012	0.0016	0.0022	0.0049
B0	0.0013	0.0018	0.0024	0.0045
B1	0.0013	0.0017	0.0022	0.0045

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0480	0.0425	0.0464	0.0457	11.2641	7.3567	5.9135	2.8898
A0 → Y↓	0.0459	0.0442	0.0291	0.0288	9.9042	6.8846	3.4527	1.7023
A1 → Y↑	0.0513	0.0458	0.0522	0.0523	11.2272	7.3274	5.8930	2.8808
A1 → Y↓	0.0485	0.0472	0.0323	0.0326	9.8983	6.8817	3.4517	1.7026
A2 → Y↑	0.0538	0.0484	0.0570	0.0573	11.0109	7.1807	5.7837	2.8458
A2 → Y↓	0.0501	0.0492	0.0343	0.0346	9.8994	6.8819	3.4522	1.7020
B0 → Y↑	0.0325	0.0299	0.0344	0.0351	11.2877	7.2893	5.3399	2.7606
B0 → Y↓	0.0190	0.0187	0.0140	0.0145	7.0325	4.8864	2.4556	1.2967
B1 → Y↑	0.0363	0.0334	0.0434	0.0424	11.0389	7.1866	5.7895	2.8483
B1 → Y↓	0.0211	0.0207	0.0157	0.0166	7.0369	4.8878	2.4552	1.2967

Cell Description

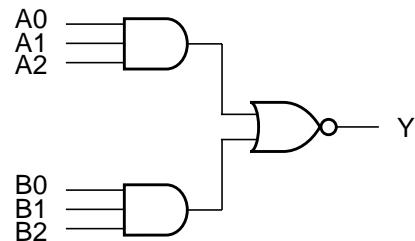
The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1 \bullet A_2) + (B_0 \bullet B_1 \bullet B_2)}$$

Functions

A0	A1	A2	B0	B1	B2	Y
0	x	x	0	x	x	1
0	x	x	x	0	x	1
0	x	x	x	x	0	1
x	0	x	0	x	x	1
x	0	x	x	0	x	1
x	0	x	x	x	0	1
x	x	0	0	x	x	1
x	x	0	x	0	x	1
x	x	x	1	1	1	0
1	1	1	x	x	x	0

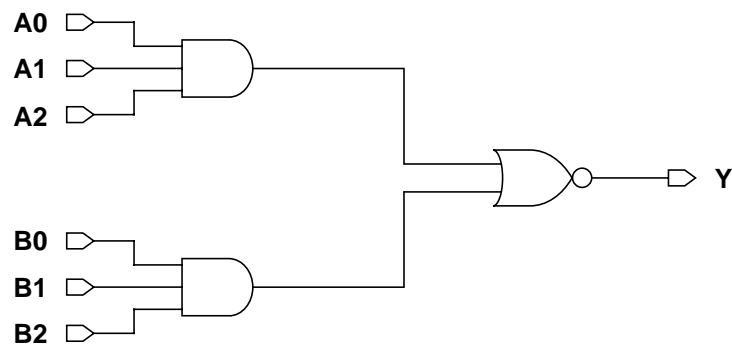
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AOI33XL	2.52	2.52
AOI33X1	2.52	2.52
AOI33X2	2.52	2.52
AOI33X4	2.52	4.76

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0029	0.0039	0.0057	0.0112
A1	0.0032	0.0043	0.0065	0.0130
A2	0.0035	0.0047	0.0073	0.0146
B0	0.0041	0.0054	0.0076	0.0151
B1	0.0043	0.0058	0.0084	0.0169
B2	0.0047	0.0063	0.0093	0.0187

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0014	0.0018	0.0024	0.0045
A1	0.0013	0.0017	0.0024	0.0049
A2	0.0013	0.0017	0.0022	0.0047
B0	0.0013	0.0017	0.0024	0.0044
B1	0.0012	0.0016	0.0023	0.0047
B2	0.0012	0.0016	0.0022	0.0049

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0404	0.0354	0.0390	0.0384	11.4014	7.3316	5.3835	2.7713
A0 → Y↓	0.0313	0.0297	0.0206	0.0203	9.8057	6.8494	3.4429	1.7847
A1 → Y↑	0.0447	0.0394	0.0446	0.0449	11.3457	7.3152	5.3472	2.7581
A1 → Y↓	0.0351	0.0334	0.0243	0.0245	9.8063	6.8493	3.4429	1.7850
A2 → Y↑	0.0482	0.0424	0.0542	0.0524	11.1634	7.1987	5.7933	2.8594
A2 → Y↓	0.0372	0.0355	0.0258	0.0266	9.8088	6.8504	3.4420	1.7849
B0 → Y↑	0.0605	0.0538	0.0597	0.0584	11.4589	7.3933	5.9366	2.9033
B0 → Y↓	0.0563	0.0555	0.0362	0.0356	9.8264	6.8648	3.4416	1.6998
B1 → Y↑	0.0638	0.0571	0.0654	0.0650	11.3903	7.3501	5.9073	2.8939
B1 → Y↓	0.0591	0.0586	0.0394	0.0394	9.8259	6.8642	3.4415	1.7001
B2 → Y↑	0.0664	0.0594	0.0699	0.0698	11.1506	7.1974	5.7927	2.8580
B2 → Y↓	0.0611	0.0605	0.0412	0.0414	9.8285	6.8636	3.4418	1.7003

Cell Description

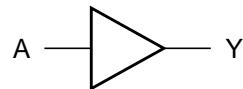
The BUF cell provides the logical buffer of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

A	Y
0	0
1	1

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
BUFX2	2.52	1.12
BUFX3	2.52	1.40
BUFX4	2.52	1.68
BUFX5	2.52	1.96
BUFX6	2.52	2.24
BUFX8	2.52	2.52
BUFX10	2.52	3.08
BUFX12	2.52	3.36
BUFX14	2.52	3.92
BUFX16	2.52	4.48
BUFX18	2.52	4.76
BUFX20	2.52	5.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)											
	X2	X3	X4	X5	X6	X8	X10	X12	X14	X16	X18	X20
A	0.0038	0.0051	0.0065	0.0090	0.0094	0.0119	0.0151	0.0173	0.0206	0.0238	0.0248	0.0273

Pin Capacitance

Pin	Capacitance (pF)											
	X2	X3	X4	X5	X6	X8	X10	X12	X14	X16	X18	X20
A	0.0014	0.0017	0.0020	0.0025	0.0030	0.0034	0.0044	0.0042	0.0063	0.0064	0.0081	0.0086

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)											
	X2	X3	X4	X5	X6	X8	X10	X12	X14	X16	X18	X20
A → Y↑	0.0262	0.0282	0.0275	0.0285	0.0262	0.0272	0.0254	0.0289	0.0253	0.0271	0.0245	0.0251
A → Y↓	0.0426	0.0396	0.0377	0.0396	0.0366	0.0378	0.0370	0.0401	0.0356	0.0379	0.0346	0.0346

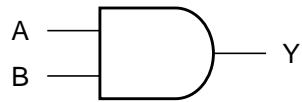
Description	K_{load} (ns/pF)											
	X2	X3	X4	X5	X6	X8	X10	X12	X14	X16	X18	X20
A → Y↑	2.6037	1.7875	1.3465	0.9643	0.9088	0.6885	0.5560	0.4657	0.4179	0.3522	0.3519	0.3136
A → Y↓	1.5267	0.9896	0.7468	0.5386	0.4938	0.3704	0.2937	0.2464	0.2214	0.1832	0.1812	0.1610

Cell Description

The CLKAND2 cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = A \bullet B$$

Logic Symbol



Functions

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
CLKAND2X2	2.52	1.40
CLKAND2X3	2.52	1.68
CLKAND2X4	2.52	1.96
CLKAND2X6	2.52	2.24
CLKAND2X8	2.52	3.36
CLKAND2X12	2.52	4.20

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	X2	X3	X4	X6	X8	X12
A	0.0033	0.0045	0.0056	0.0075	0.0106	0.0145
B	0.0036	0.0050	0.0061	0.0082	0.0117	0.0159

Pin Capacitance

Pin	Capacitance (pF)					
	X2	X3	X4	X6	X8	X12
A	0.0013	0.0016	0.0018	0.0022	0.0033	0.0042
B	0.0013	0.0015	0.0019	0.0022	0.0037	0.0045

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	X2	X3	X4	X6	X8	X12
A → Y↑	0.0427	0.0471	0.0431	0.0462	0.0409	0.0426
A → Y↓	0.0403	0.0425	0.0396	0.0410	0.0401	0.0413
B → Y↑	0.0442	0.0491	0.0451	0.0481	0.0429	0.0446
B → Y↓	0.0439	0.0466	0.0433	0.0445	0.0425	0.0435

Delays at 25°C, 1.0V, Typical Process

Description	K _{load} (ns/pF)					
	X2	X3	X4	X6	X8	X12
A → Y↑	2.6303	1.8130	1.3681	1.0236	0.6964	0.4835
A → Y↓	2.9499	1.9040	1.4485	1.0287	0.7174	0.4891
B → Y↑	2.6300	1.8123	1.3679	1.0235	0.6965	0.4837
B → Y↓	2.9539	1.9068	1.4504	1.0298	0.7174	0.4891

Cell Description

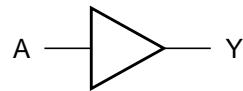
The CLKBUF cell provides the logical buffer of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

A	Y
0	0
1	1

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
CLKBUFX1	2.52	1.12
CLKBUFX2	2.52	1.12
CLKBUFX3	2.52	1.40
CLKBUFX4	2.52	1.40
CLKBUFX6	2.52	1.96
CLKBUFX8	2.52	2.52
CLKBUFX12	2.52	3.36
CLKBUFX16	2.52	3.92
CLKBUFX20	2.52	5.04
CLKBUFX24	2.52	6.16
CLKBUFX32	2.52	8.12
CLKBUFX40	2.52	9.80

Functional Schematic



AC Power

Pin	Power (μ W/MHz)											
	X1	X2	X3	X4	X6	X8	X12	X16	X20	X24	X32	X40
A	0.0031	0.0037	0.0043	0.0051	0.0071	0.0092	0.0127	0.0163	0.0216	0.0258	0.0345	0.0434

Pin Capacitance

Pin	Capacitance (pF)											
	X1	X2	X3	X4	X6	X8	X12	X16	X20	X24	X32	X40
A	0.0016	0.0018	0.0017	0.0017	0.0020	0.0025	0.0033	0.0046	0.0054	0.0067	0.0090	0.0109

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)											
	X1	X2	X3	X4	X6	X8	X12	X16	X20	X24	X32	X40
A → Y↑	0.0301	0.0255	0.0280	0.0300	0.0398	0.0385	0.0346	0.0356	0.0368	0.0364	0.0359	0.0342
A → Y↓	0.0307	0.0322	0.0360	0.0399	0.0406	0.0420	0.0398	0.0367	0.0389	0.0382	0.0389	0.0404

Description	K _{load} (ns/pF)											
	X1	X2	X3	X4	X6	X8	X12	X16	X20	X24	X32	X40
A → Y↑	3.8729	2.6309	1.8879	1.3387	0.9138	0.6891	0.4909	0.4006	0.2880	0.2371	0.1805	0.1446
A → Y↓	4.2077	2.8357	1.9043	1.4099	0.9832	0.6797	0.4823	0.3584	0.2765	0.2367	0.1799	0.1377

Cell Description

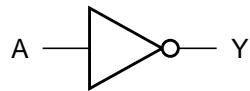
The CLKINV cell provides the logical inversion of a single input A, with balanced delays for clock signals. The output Y is represented by the logic equation:

$$Y = \bar{A}$$

Functions

A	Y
0	1
1	0

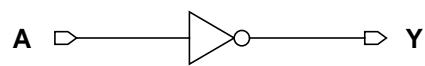
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
CLKINVX1	2.52	0.84
CLKINVX2	2.52	0.84
CLKINVX3	2.52	1.12
CLKINVX4	2.52	1.12
CLKINVX6	2.52	1.68
CLKINVX8	2.52	1.96
CLKINVX12	2.52	2.52
CLKINVX16	2.52	3.36
CLKINVX20	2.52	3.92
CLKINVX24	2.52	4.76
CLKINVX32	2.52	6.16
CLKINVX40	2.52	7.00

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	X1	X2	X3	X4	X6	X8
A	0.0015	0.0020	0.0028	0.0036	0.0053	0.0070
Pin	Power ($\mu\text{W}/\text{MHz}$)					
	X12	X16	X20	X24	X32	X40
A	0.0102	0.0138	0.0167	0.0206	0.0273	0.0334

Pin Capacitance

Pin	Capacitance (pF)					
	X1	X2	X3	X4	X6	X8
A	0.0015	0.0020	0.0029	0.0037	0.0054	0.0070
Pin	Capacitance (pF)					
	X12	X16	X20	X24	X32	X40
A	0.0104	0.0141	0.0173	0.0212	0.0279	0.0343

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	X1	X2	X3	X4	X6	X8
A → Y↑	0.0109	0.0103	0.0098	0.0095	0.0096	0.0097
A → Y↓	0.0119	0.0112	0.0108	0.0102	0.0104	0.0101
Description	Intrinsic Delay (ns)					
	X12	X16	X20	X24	X32	X40
A → Y↑	0.0097	0.0098	0.0099	0.0100	0.0106	0.0108
A → Y↓	0.0101	0.0101	0.0098	0.0102	0.0105	0.0101

Delays at 25°C, 1.0V, Typical Process

Description	K_{load} (ns/pF)					
	X1	X2	X3	X4	X6	X8
A → Y↑	3.7512	2.5748	1.7604	1.3213	0.8950	0.7044
A → Y↓	4.2711	2.8826	2.0094	1.4604	0.9861	0.7318

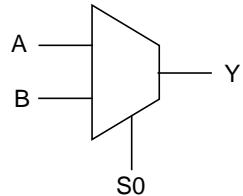
Description	K_{load} (ns/pF)					
	X12	X16	X20	X24	X32	X40
A → Y↑	0.4700	0.3531	0.2911	0.2307	0.1723	0.1418
A → Y↓	0.4844	0.3621	0.2768	0.2394	0.1800	0.1374

Cell Description

The CLKMX2 cell is a non-inverting 2 to 1 multiplexer with balanced delays for clock signals. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (S0 \bullet B) + (\overline{S0} \bullet A)$$

Logic Symbol



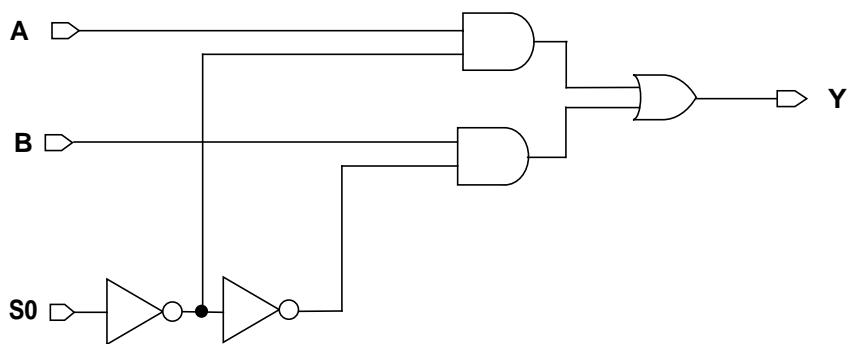
Functions

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
CLKMX2X2	2.52	2.80
CLKMX2X3	2.52	3.36
CLKMX2X4	2.52	3.36
CLKMX2X6	2.52	3.64
CLKMX2X8	2.52	3.92
CLKMX2X12	2.52	5.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	X2	X3	X4	X6	X8	X12
S0	0.0063	0.0078	0.0088	0.0111	0.0137	0.0204
B	0.0056	0.0066	0.0075	0.0099	0.0127	0.0197
A	0.0052	0.0062	0.0071	0.0095	0.0122	0.0192

Pin Capacitance

Pin	Capacitance (pF)					
	X2	X3	X4	X6	X8	X12
S0	0.0034	0.0035	0.0035	0.0035	0.0035	0.0035
B	0.0016	0.0018	0.0018	0.0018	0.0018	0.0018
A	0.0018	0.0021	0.0021	0.0021	0.0021	0.0021

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	X2	X3	X4	X6	X8	X12
S0 → Y↑	0.0549	0.0569	0.0608	0.0680	0.0751	0.0917
S0 → Y↓	0.0581	0.0606	0.0664	0.0742	0.0819	0.1019
B → Y↑	0.0541	0.0538	0.0585	0.0670	0.0759	0.0937
B → Y↓	0.0578	0.0583	0.0644	0.0731	0.0822	0.1031
A → Y↑	0.0562	0.0557	0.0589	0.0671	0.0750	0.0925
A → Y↓	0.0570	0.0572	0.0631	0.0719	0.0810	0.1019

Description	K _{load} (ns/pF)					
	X2	X3	X4	X6	X8	X12
S0 → Y↑	2.9826	1.8466	1.3931	0.9440	0.7195	0.4949
S0 → Y↓	3.3005	2.0346	1.6504	1.0176	0.7487	0.5174
B → Y↑	2.9824	1.8479	1.3946	0.9459	0.7216	0.4967
B → Y↓	3.3001	2.0342	1.6501	1.0176	0.7487	0.5174
A → Y↑	2.9821	1.8474	1.3933	0.9442	0.7197	0.4950
A → Y↓	3.2964	2.0326	1.6496	1.0171	0.7485	0.5174

Cell Description

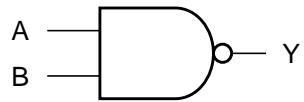
The CLKNAND2 cell provides the logical NAND of two inputs (A, B), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B)}$$

Functions

A	B	Y
0	x	1
x	0	1
1	1	0

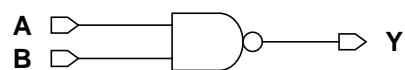
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
CLKNAND2X2	2.52	1.12
CLKNAND2X4	2.52	1.96
CLKNAND2X8	2.52	3.36
CLKNAND2X12	2.52	4.76

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X2	X4	X8	X12
A	0.0025	0.0048	0.0093	0.0136
B	0.0031	0.0061	0.0118	0.0171

Pin Capacitance

Pin	Capacitance (pF)			
	X2	X4	X8	X12
A	0.0022	0.0041	0.0080	0.0118
B	0.0021	0.0044	0.0083	0.0121

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X2	X4	X8	X12	X2	X4	X8	X12
A → Y↑	0.0126	0.0124	0.0127	0.0125	2.6388	1.3739	0.7431	0.4891
A → Y↓	0.0148	0.0138	0.0133	0.0141	3.3761	1.6526	0.8138	0.5942
B → Y↑	0.0141	0.0142	0.0148	0.0144	2.6410	1.3340	0.7348	0.4852
B → Y↓	0.0160	0.0158	0.0151	0.0159	3.3752	1.6536	0.8140	0.5941

Cell Description

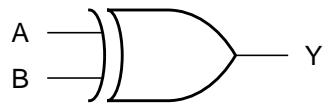
The CLKXOR2 cell provides a logical EXCLUSIVE OR of two inputs (A, B) with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = (A \bullet \bar{B}) + (\bar{A} \bullet B)$$

Functions

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

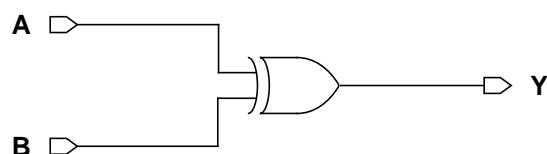
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
CLKXOR2X1	2.52	2.80
CLKXOR2X2	2.52	2.80
CLKXOR2X4	2.52	4.20
CLKXOR2X8	2.52	6.72
CLKXOR2X12	2.52	10.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)				
	X1	X2	X4	X8	X12
A	0.0064	0.0069	0.0099	0.0191	0.0275
B	0.0067	0.0072	0.0128	0.0252	0.0380

Pin Capacitance

Pin	Capacitance (pF)				
	X1	X2	X4	X8	X12
A	0.0031	0.0031	0.0039	0.0062	0.0083
B	0.0017	0.0017	0.0032	0.0056	0.0090

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					K_{load} (ns/pF)				
	X1	X2	X4	X8	X12	X1	X2	X4	X8	X12
A → Y↑	0.0557	0.0577	0.0547	0.0650	0.0641	3.9472	2.6897	1.3654	0.7034	0.4772
A → Y↓	0.0599	0.0630	0.0607	0.0678	0.0655	4.2911	2.8136	1.4695	0.7388	0.5006
B → Y↑	0.0776	0.0801	0.0733	0.0725	0.0721	3.9310	2.6820	1.3667	0.7040	0.4783
B → Y↓	0.0808	0.0846	0.0781	0.0792	0.0772	4.2895	2.8134	1.4694	0.7389	0.5006

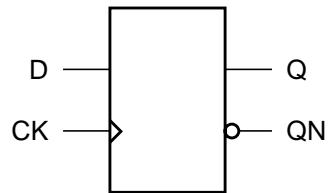
Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

Function Table

D	CK	Q[n+1]	QN[n+1]
0	/	0	1
1	/	1	0
x	\	Q[n]	QN[n]

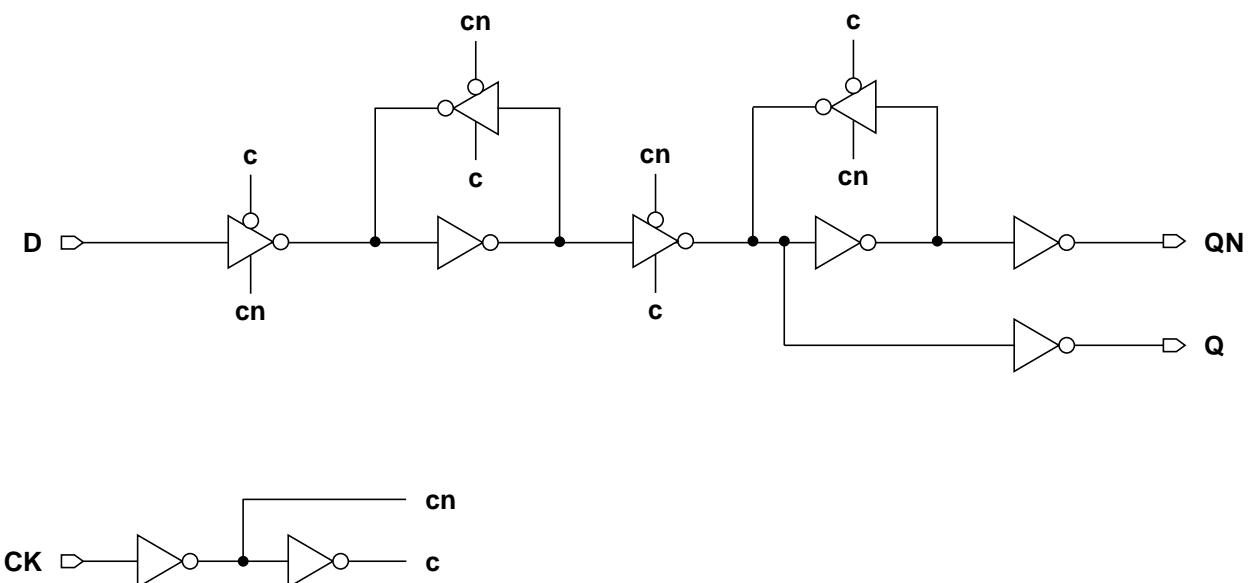
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFXL	2.52	6.16
DFFX1	2.52	6.16
DFFX2	2.52	6.16
DFFX4	2.52	7.84

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0047	0.0049	0.0050	0.0060
CK	0.0102	0.0103	0.0107	0.0124
Q	0.0050	0.0059	0.0077	0.0131

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0011	0.0011	0.0011	0.0011
CK	0.0015	0.0015	0.0015	0.0017

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1039	0.1012	0.0984	0.1009	5.7896	3.6848	2.6788	1.3760
CK → Q↓	0.1149	0.1119	0.1010	0.0980	5.2607	3.3700	1.6689	0.8127
CK → QN↑	0.1473	0.1432	0.1427	0.1429	5.6526	3.6316	2.6565	1.3643
CK → QN↓	0.1454	0.1479	0.1500	0.1503	4.4911	3.0788	1.5733	0.7718

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0312	0.0352	0.0312	0.0352
	setup↓ → CK	0.0469	0.0469	0.0664	0.0742
	hold↑ → CK	-0.0195	-0.0195	-0.0156	-0.0195
	hold↓ → CK	-0.0078	-0.0078	-0.0234	-0.0234
CK	minpwh	0.0979	0.0930	0.0882	0.0833
	minpwl	0.0638	0.0638	0.0638	0.0638

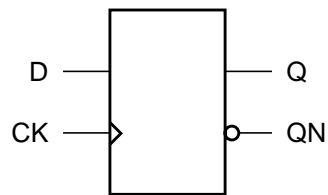
Cell Description

The DFFH cell is a positive-edge triggered, static D-type flip-flop and fast clock-to-Q-path.

Function Table

D	CK	Q[n+1]	QN[n+1]
0	/	0	1
1	/	1	0
x	\	Q[n]	QN[n]

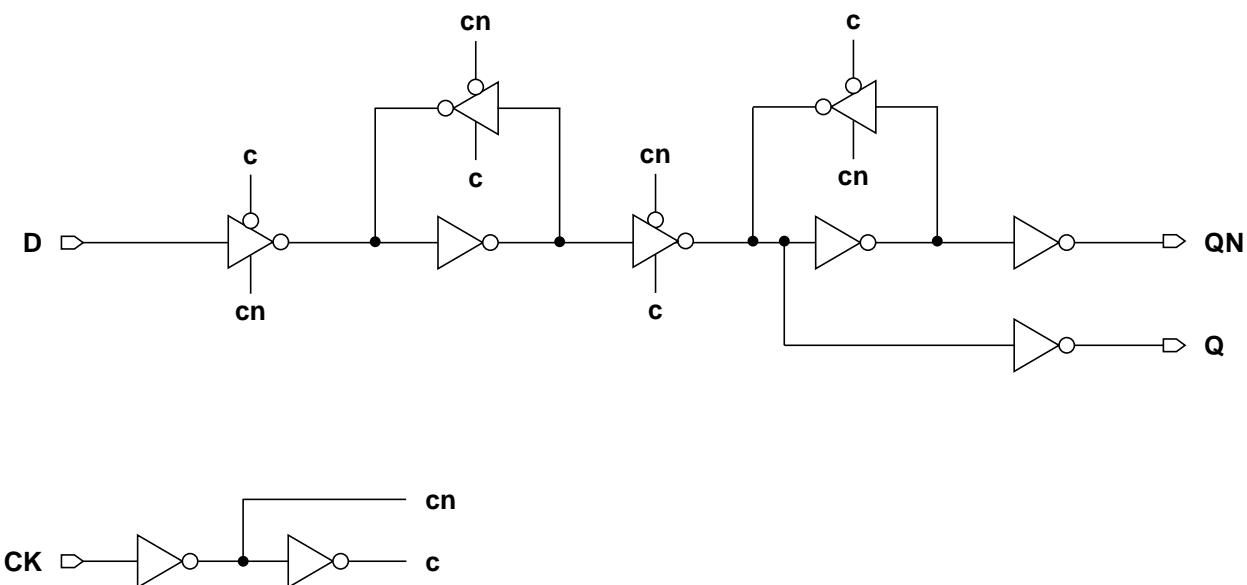
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFHX1	2.52	7.28
DFFHX2	2.52	7.84
DFFHX4	2.52	9.24
DFFHX8	2.52	9.80

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
D	0.0069	0.0088	0.0123	0.0126
CK	0.0146	0.0178	0.0221	0.0223
Q	0.0052	0.0074	0.0085	0.0146

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0011	0.0012	0.0024	0.0024
CK	0.0023	0.0024	0.0026	0.0026

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0720	0.0724	0.0655	0.0743	3.6118	2.6623	1.3465	0.6857
CK → Q↓	0.0779	0.0773	0.0764	0.0883	3.1530	1.5637	0.7852	0.4062
CK → QN↑	0.1032	0.1085	0.1134	0.1298	5.5564	2.6489	11.0711	11.0668
CK → QN↓	0.1114	0.1116	0.1168	0.1304	4.2759	1.5390	4.1720	4.1625

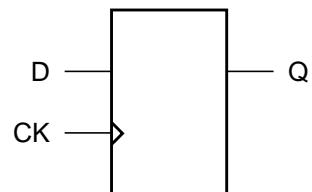
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CK	0.0469	0.0391	0.0391	0.0430
	setup↓ → CK	0.0469	0.0469	0.0352	0.0352
	hold↑ → CK	-0.0078	-0.0078	-0.0078	-0.0039
	hold↓ → CK	-0.0234	-0.0195	-0.0078	-0.0078
CK	minpwh	0.0492	0.0492	0.0444	0.0492
	minpwl	0.0979	0.0930	0.0882	0.0882

Cell Description

The DFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



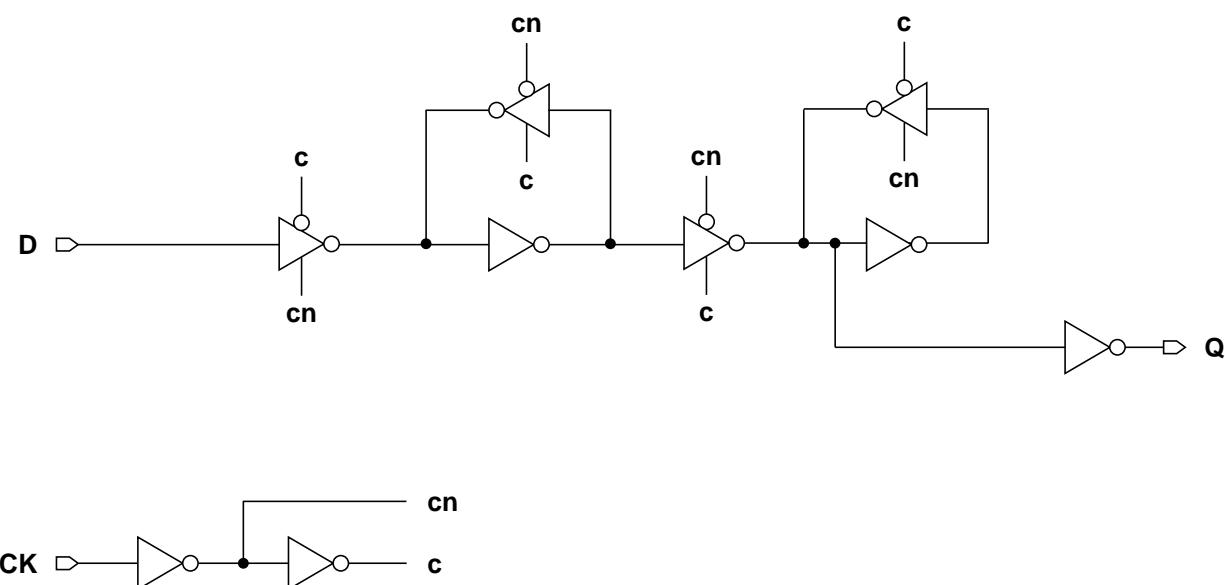
Functions

D	CK	Q[n+1]
0	/\	0
1	/\	1
x	\/\	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFHQX1	2.52	6.72
DFFHQX2	2.52	6.72
DFFHQX4	2.52	8.40
DFFHQX8	2.52	9.24

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
D	0.0069	0.0072	0.0121	0.0124
CK	0.0137	0.0155	0.0220	0.0222
Q	0.0038	0.0051	0.0072	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0015	0.0012	0.0020	0.0020
CK	0.0023	0.0022	0.0028	0.0028

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0746	0.0754	0.0663	0.0750	3.5293	2.6348	1.3460	0.6948
CK → Q↓	0.0815	0.0799	0.0697	0.0804	3.2312	1.6135	0.7742	0.3933

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CK	0.0508	0.0469	0.0391	0.0391
	setup↓ → CK	0.0352	0.0508	0.0391	0.0391
	hold↑ → CK	-0.0117	-0.0117	-0.0039	-0.0039
	hold↓ → CK	-0.0117	-0.0234	-0.0117	-0.0117
CK	minpwh	0.0492	0.0444	0.0444	0.0444
	minpwl	0.1028	0.1028	0.0882	0.0882

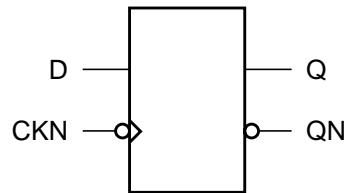
Cell Description

The DFFNH cell is a negative-edge triggered, static D-type flip-flop and fast clock-to-Q-path.

Functions

D	CKN	Q[n+1]	QN[n+1]
0	—	0	1
1	—	1	0
x	—	Q[n]	QN[n]

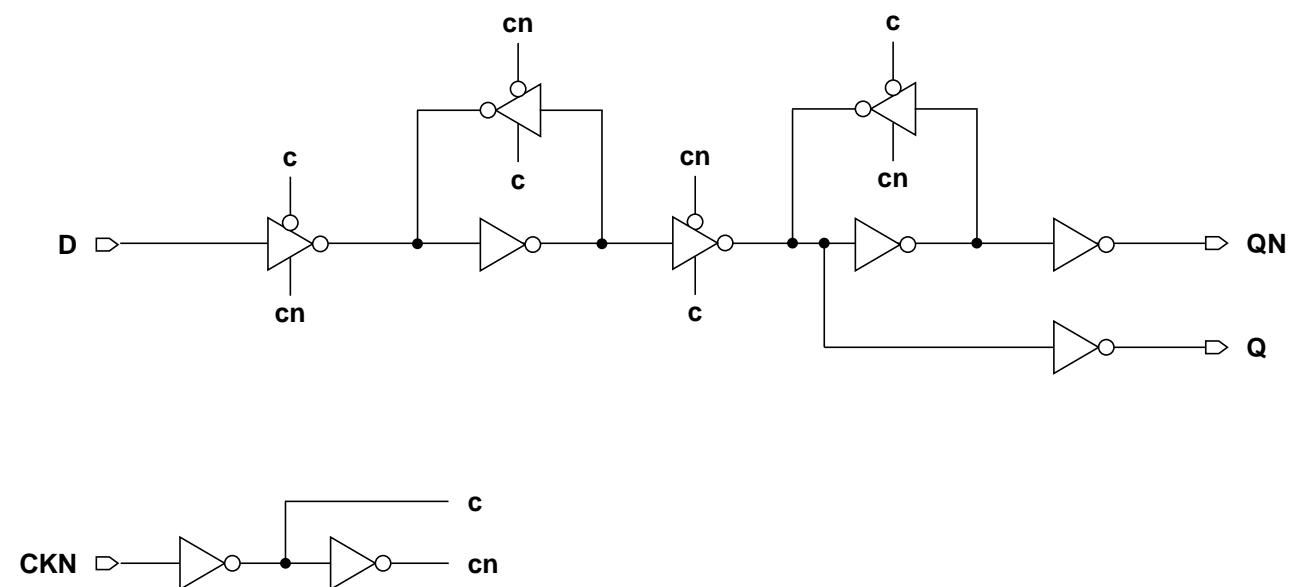
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFNHX1	2.52	7.00
DFFNHX2	2.52	7.00
DFFNHX4	2.52	9.24
DFFNHX8	2.52	10.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
D	0.0067	0.0065	0.0123	0.0126
CKN	0.0114	0.0111	0.0190	0.0192
Q	0.0054	0.0064	0.0093	0.0149

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0014	0.0013	0.0024	0.0024
CKN	0.0021	0.0021	0.0025	0.0025

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CKN → Q↑	0.1428	0.1464	0.1408	0.1511	3.6087	2.6366	1.3300	0.6863
CKN → Q↓	0.1260	0.1322	0.1107	0.1272	3.2206	1.6817	0.7774	0.4008
CKN → QN↑	0.1532	0.1726	0.1488	0.1702	5.3841	11.1177	11.1480	11.1336
CKN → QN↓	0.1833	0.1863	0.1949	0.2100	4.2956	4.1716	4.1718	4.1596

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CKN	-0.0156	-0.0039	-0.0312	-0.0312
	setup↓ → CKN	0.0117	0.0195	0.0117	0.0117
	hold↑ → CKN	0.0469	0.0430	0.0547	0.0586
	hold↓ → CKN	0.0117	0.0078	0.0117	0.0117
CKN	minpwl	0.1271	0.1320	0.1320	0.1368
	minpwh	0.0395	0.0444	0.0444	0.0444

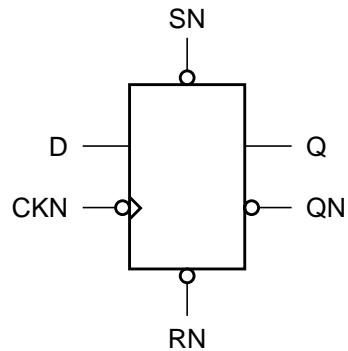
Cell Description

The DFFNSRH cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset, and fast clock-to-Q-path.

Functions

RN	SN	D	CKN	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	—	0	1
1	1	1	—	1	0
1	1	x	—	Q[n]	QN[n]

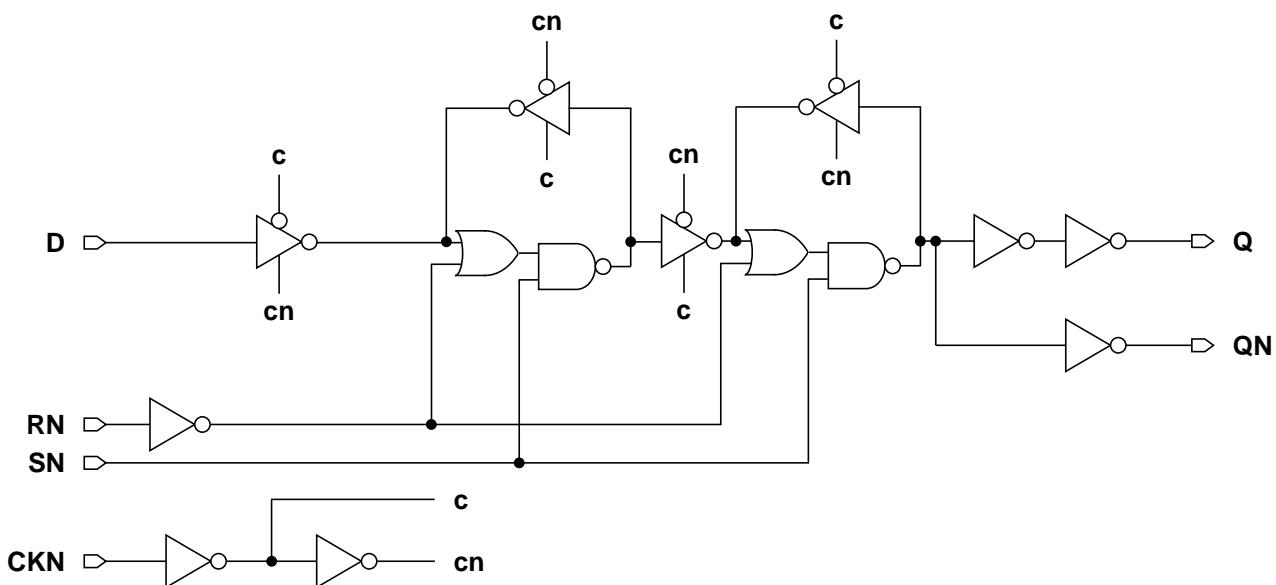
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFNSRHX1	2.52	10.08
DFFNSRHX2	2.52	10.08
DFFNSRHX4	2.52	12.88
DFFNSRHX8	2.52	13.72

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
D	0.0079	0.0089	0.0140	0.0143
CKN	0.0124	0.0136	0.0207	0.0209
SN	0.0041	0.0042	0.0053	0.0056
RN	0.0015	0.0016	0.0026	0.0027
Q	0.0069	0.0079	0.0121	0.0186

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0013	0.0016	0.0021	0.0021
CKN	0.0022	0.0023	0.0027	0.0027
SN	0.0022	0.0023	0.0033	0.0033
RN	0.0019	0.0022	0.0034	0.0034

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CKN → Q↑	0.1625	0.1577	0.1615	0.1723	3.7289	2.6815	1.3582	0.6993
CKN → Q↓	0.1382	0.1258	0.1176	0.1317	3.3530	1.6828	0.8070	0.4145
SN → Q↑	0.1040	0.1151	0.1432	0.1633	3.6380	2.6647	1.3681	0.7041
SN → Q↓	0.1916	0.1844	0.1522	0.1860	3.8567	1.9345	0.9134	0.4773
RN → Q↓	0.1658	0.1596	0.1208	0.1548	3.8679	1.9426	0.9152	0.4783
CKN → QN↑	0.1679	0.1662	0.1583	0.1788	5.4240	10.9479	10.7503	11.0357
CKN → QN↓	0.2106	0.2035	0.2107	0.2263	4.4107	4.3431	4.3291	4.3038
SN → QN↑	0.2252	0.2346	0.2020	0.2476	5.4512	10.9576	10.7564	11.0381
SN → QN↓	0.1502	0.1607	0.1947	0.2215	4.3951	4.3378	4.3283	4.3036
RN → QN↑	0.1996	0.2102	0.1709	0.2168	5.4516	10.9565	10.7550	11.0369

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CKN	-0.0039	-0.0156	-0.0195	-0.0195
	setup↓ → CKN	0.0156	0.0195	0.0195	0.0195
	hold↑ → CKN	0.0547	0.0547	0.0508	0.0586
	hold↓ → CKN	0.0156	0.0156	0.0117	0.0117
CKN	minpwl	0.1466	0.1417	0.1466	0.1563
	minpwh	0.0444	0.0444	0.0492	0.0492
SN	minpwl	0.0882	0.0979	0.1222	0.1417
	recovery	-0.0078	0.0000	-0.0039	-0.0039
	removal	0.0234	0.0234	0.0234	0.0234
RN	minpwl	0.1612	0.1563	0.1174	0.1466
	recovery	-0.0859	-0.0859	-0.0898	-0.0898
	removal	0.1250	0.1250	0.1641	0.1602

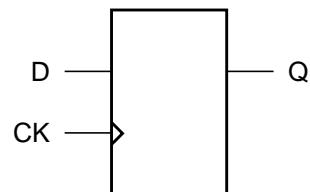
Cell Description

The DFFQ cell is a positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) .

Functions

D	CK	Q[n+1]
0	/	0
1	/	1
x	\	Q[n]

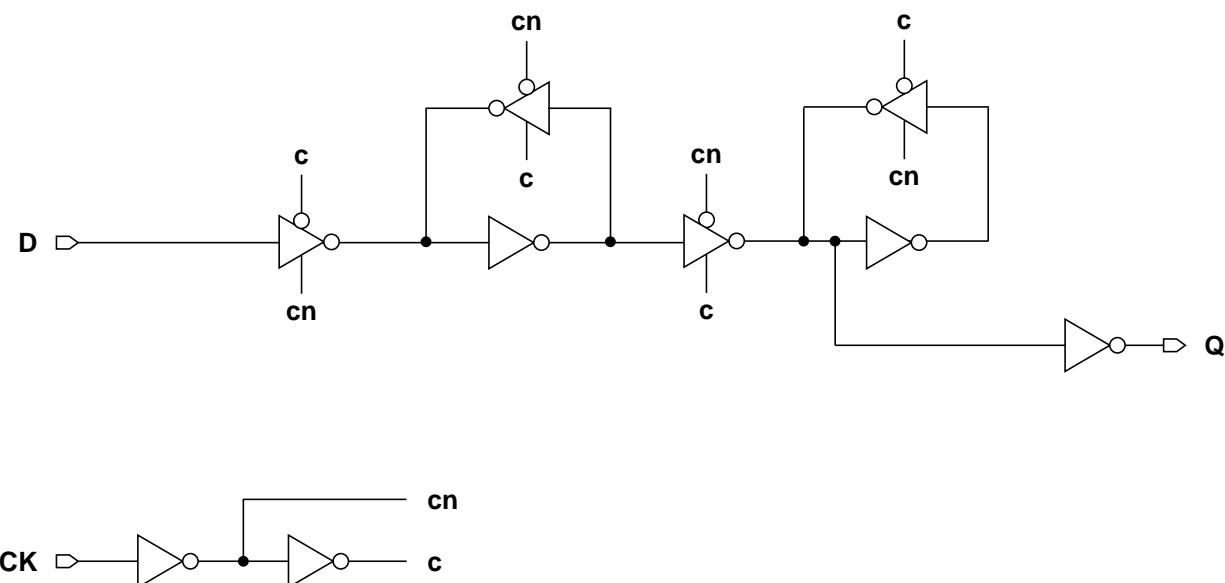
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFQXL	2.52	5.32
DFFQX1	2.52	5.60
DFFQX2	2.52	5.60
DFFQX4	2.52	7.00

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0044	0.0045	0.0044	0.0054
CK	0.0097	0.0098	0.0099	0.0117
Q	0.0037	0.0041	0.0054	0.0084

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0011	0.0011	0.0010	0.0010
CK	0.0016	0.0016	0.0016	0.0016

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.0998	0.0973	0.0971	0.1010	5.6335	3.5863	2.5965	1.3362
CK → Q↓	0.1164	0.1131	0.1138	0.1009	5.2381	3.3883	1.7117	0.8247

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0273	0.0312	0.0273	0.0352
	setup↓ → CK	0.0430	0.0469	0.0547	0.0664
	hold↑ → CK	-0.0156	-0.0156	-0.0117	-0.0195
	hold↓ → CK	-0.0117	-0.0078	-0.0195	-0.0195
CK	minpwh	0.0930	0.0882	0.0882	0.0784
	minpwl	0.0590	0.0590	0.0590	0.0638

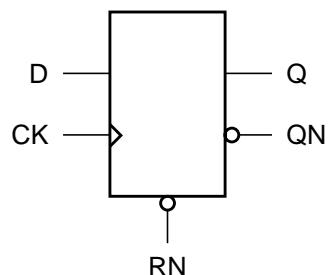
Cell Description

The DFFR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Functions

RN	D	CK	Q[n+1]	QN[n+1]
0	x	x	0	1
1	0	—	0	1
1	1	—	1	0
1	x	—	Q[n]	QN[n]

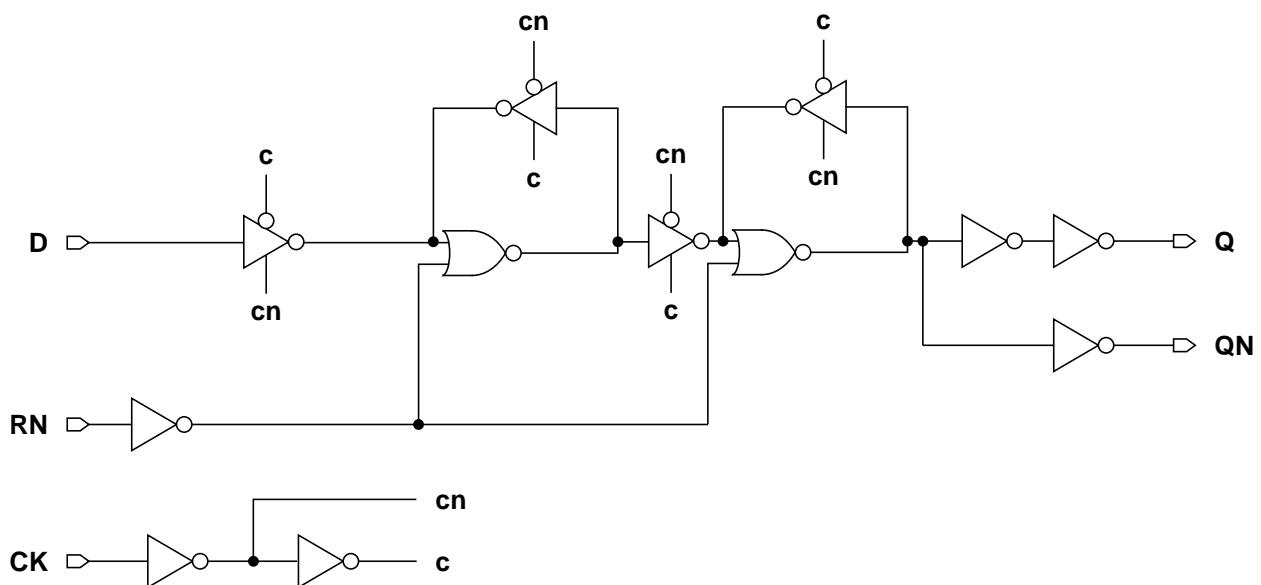
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFRLXL	2.52	6.72
DFFRX1	2.52	6.72
DFFRX2	2.52	7.00
DFFRX4	2.52	7.56

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
D	0.0055	0.0055	0.0053	0.0060
CK	0.0104	0.0104	0.0103	0.0111
RN	0.0012	0.0013	0.0014	0.0019
Q	0.0049	0.0058	0.0080	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0010	0.0010	0.0008	0.0008
CK	0.0016	0.0016	0.0016	0.0016
RN	0.0030	0.0030	0.0032	0.0037

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1317	0.1400	0.1509	0.1583	5.7226	3.7932	2.6771	1.3769
CK → Q↓	0.1503	0.1614	0.1567	0.1584	4.3812	3.1989	1.5744	0.7749
RN → Q↓	0.0730	0.0810	0.0644	0.0577	4.4370	3.2036	1.5788	0.7776
CK → QN↑	0.0934	0.0946	0.1016	0.1050	5.7381	3.8060	2.7323	1.4437
CK → QN↓	0.0862	0.0929	0.1011	0.1117	4.6286	3.3456	1.7363	0.8980
RN → QN↑	0.1231	0.1314	0.1272	0.1470	5.6672	3.7612	2.6987	1.4462

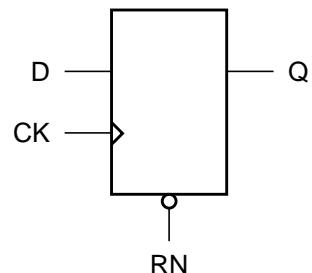
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0742	0.0742	0.0625	0.0664
	setup↓ → CK	0.0312	0.0312	0.0898	0.0898
	hold↑ → CK	-0.0430	-0.0430	-0.0312	-0.0312
	hold↓ → CK	0.0078	0.0078	-0.0234	-0.0195
CK	minpwh	0.0784	0.0882	0.0979	0.1028
	minpw1	0.0736	0.0736	0.0687	0.0736
RN	minpw1	0.0833	0.0882	0.0784	0.0882
	recovery	0.0742	0.0742	0.0625	0.0664
	removal	-0.0547	-0.0586	-0.0469	-0.0508

Cell Description

The DFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



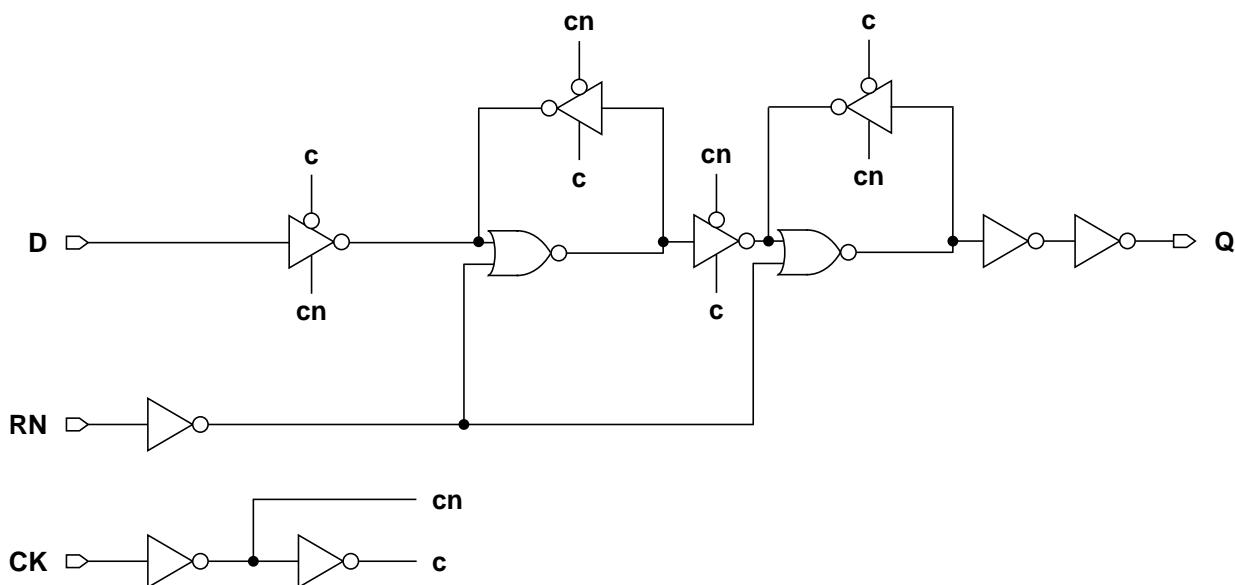
Functions

RN	D	CK	$Q[n+1]$
0	x	x	0
1	0	—	0
1	1	—	1
1	x	—	$Q[n]$

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRHQX1	2.52	7.56
DFFRHQX2	2.52	7.56
DFFRHQX4	2.52	9.52
DFFRHQX8	2.52	10.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
D	0.0074	0.0084	0.0127	0.0130
CK	0.0135	0.0158	0.0240	0.0239
RN	0.0013	0.0016	0.0024	0.0025
Q	0.0040	0.0052	0.0079	0.0134

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0015	0.0012	0.0015	0.0016
CK	0.0020	0.0021	0.0029	0.0029
RN	0.0018	0.0021	0.0033	0.0032

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0807	0.0796	0.0747	0.0846	3.6543	2.6408	1.3461	0.6980
CK → Q↓	0.0811	0.0774	0.0745	0.0846	3.2435	1.5958	0.7872	0.4006
RN → Q↓	0.0847	0.0900	0.0720	0.0936	3.2947	1.6591	0.8079	0.4147

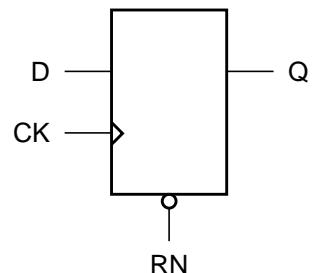
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CK	0.0625	0.0508	0.0508	0.0508
	setup↓ → CK	0.0430	0.0508	0.0508	0.0508
	hold↑ → CK	-0.0156	-0.0117	-0.0078	-0.0078
	hold↓ → CK	-0.0117	-0.0234	-0.0234	-0.0234
CK	minpwh	0.0444	0.0492	0.0444	0.0492
	minpwl	0.1125	0.1028	0.0930	0.0930
RN	minpwl	0.0784	0.0882	0.0687	0.0882
	recovery	-0.0117	-0.0156	-0.0195	-0.0195
	removal	0.0391	0.0430	0.0586	0.0547

Cell Description

The DFFRQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q).

Logic Symbol



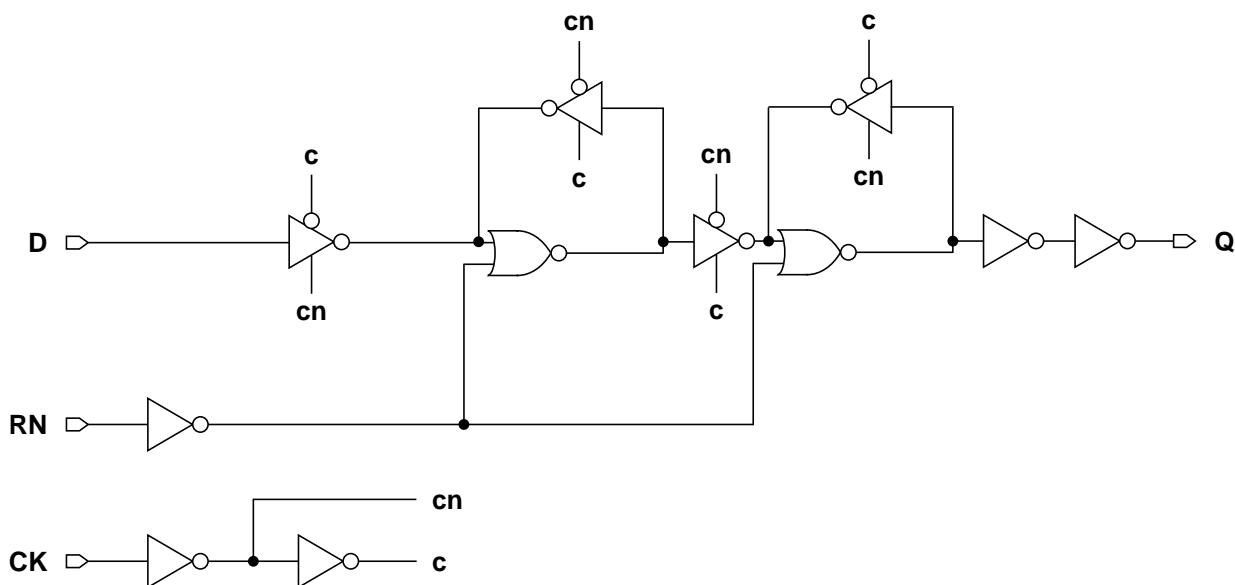
Functions

RN	D	CK	$Q[n+1]$
0	x	x	0
1	0	—	0
1	1	—	1
1	x	—	$Q[n]$

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRQXL	2.52	6.16
DFFRQX1	2.52	6.16
DFFRQX2	2.52	6.16
DFFRQX4	2.52	6.44

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0045	0.0045	0.0046	0.0048
CK	0.0086	0.0086	0.0088	0.0089
RN	0.0009	0.0009	0.0010	0.0012
Q	0.0037	0.0042	0.0052	0.0084

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0010	0.0010	0.0010	0.0010
CK	0.0012	0.0012	0.0012	0.0012
RN	0.0027	0.0027	0.0028	0.0031

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1215	0.1252	0.1266	0.1250	5.7289	3.6574	2.6690	1.3563
CK → Q↓	0.1513	0.1587	0.1593	0.1647	4.7434	3.2226	1.6580	0.8237
RN → Q↓	0.0665	0.0744	0.0808	0.0833	4.7637	3.2052	1.6336	0.8096

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0742	0.0703	0.0742	0.0742
	setup↓ → CK	0.0117	0.0117	0.0156	0.0156
	hold↑ → CK	-0.0391	-0.0391	-0.0391	-0.0391
	hold↓ → CK	0.0156	0.0156	0.0117	0.0117
CK	minpwh	0.0638	0.0687	0.0687	0.0736
	minpwl	0.0882	0.0882	0.0882	0.0882
RN	minpwl	0.0687	0.0736	0.0833	0.0882
	recovery	0.0742	0.0742	0.0742	0.0781
	removal	-0.0508	-0.0508	-0.0547	-0.0547

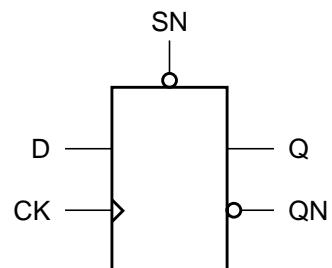
Cell Description

The DFFS cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Functions

SN	D	CK	Q[n+1]	QN[n+1]
0	x	x	1	0
1	0	✓	0	1
1	1	✓	1	0
1	x	✗	Q[n]	QN[n]

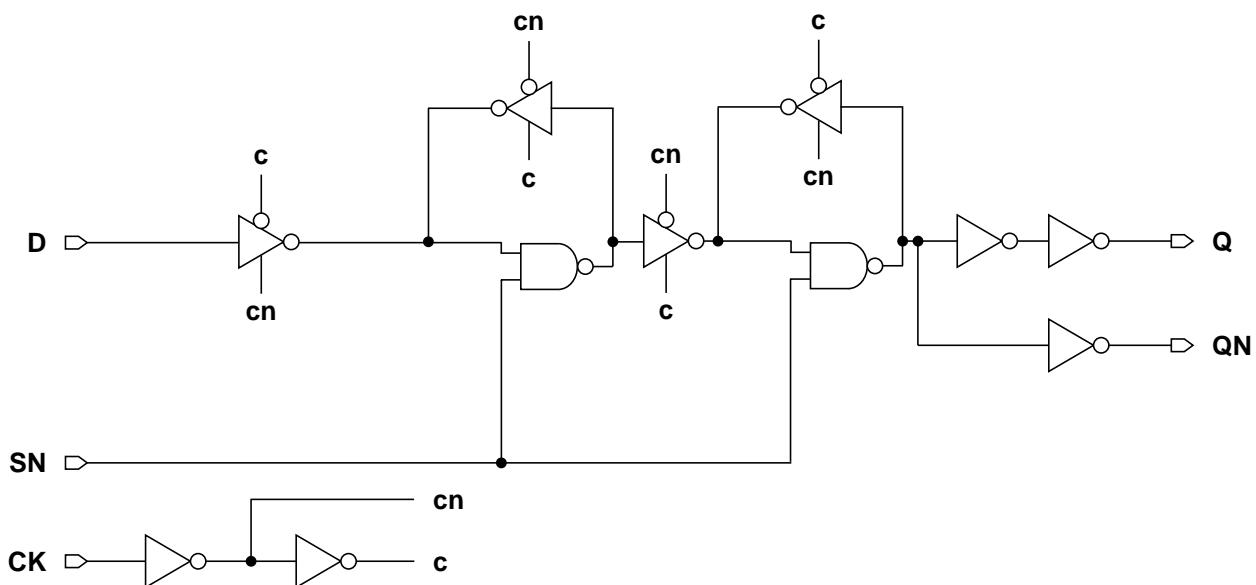
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFSXL	2.52	6.16
DFFSX1	2.52	6.16
DFFSX2	2.52	6.16
DFFSX4	2.52	7.28

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
D	0.0053	0.0053	0.0051	0.0068
CK	0.0104	0.0104	0.0103	0.0121
SN	0.0010	0.0011	0.0011	0.0015
Q	0.0054	0.0064	0.0081	0.0135

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0015	0.0014	0.0011	0.0011
CK	0.0018	0.0018	0.0017	0.0018
SN	0.0020	0.0020	0.0021	0.0026

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1394	0.1484	0.1511	0.1537	5.6371	3.7464	2.6561	1.3708
CK → Q↓	0.1408	0.1493	0.1474	0.1595	4.5075	3.0887	1.5812	0.8068
SN → Q↑	0.1107	0.1175	0.1352	0.1893	5.6071	3.7307	2.6527	1.3709
CK → QN↑	0.0984	0.1002	0.0930	0.0882	5.8931	3.8787	2.6906	1.3988
CK → QN↓	0.1034	0.1112	0.1016	0.0941	5.5898	3.7029	1.8381	0.8686
SN → QN↓	0.0778	0.0833	0.0873	0.1186	4.8877	3.2882	1.7126	0.9195

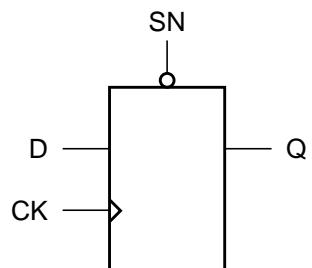
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0586	0.0547	0.0430	0.0469
	setup↓ → CK	0.0156	0.0156	0.0547	0.0742
	hold↑ → CK	-0.0234	-0.0234	-0.0195	-0.0234
	hold↓ → CK	0.0117	0.0117	-0.0156	-0.0273
CK	minpwh	0.0930	0.1028	0.0979	0.0979
	minpw1	0.0590	0.0590	0.0590	0.0638
SN	minpw1	0.0784	0.0833	0.0979	0.1417
	recovery	-0.0312	-0.0312	-0.0273	-0.0273
	removal	0.0469	0.0469	0.0430	0.0469

Cell Description

The DFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



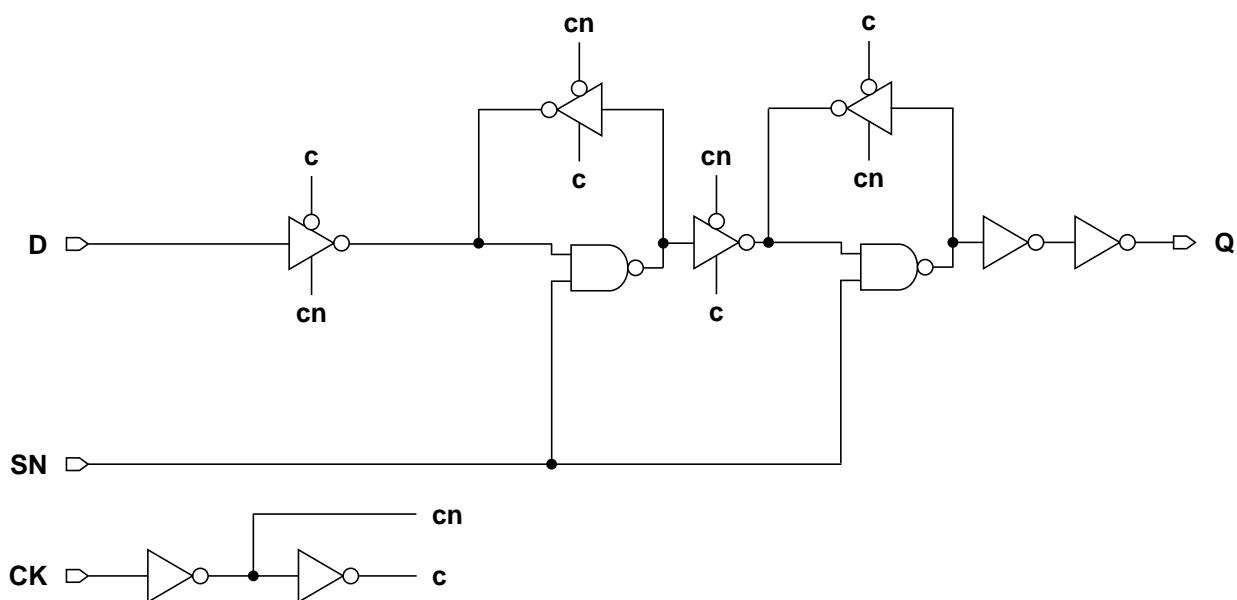
Functions

SN	D	CK	Q[n+1]
0	x	x	1
1	0	—	0
1	1	—	1
1	x	—	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSHQX1	2.52	7.84
DFFSHQX2	2.52	7.84
DFFSHQX4	2.52	9.24
DFFSHQX8	2.52	10.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
D	0.0072	0.0073	0.0104	0.0108
CK	0.0137	0.0146	0.0193	0.0196
SN	0.0033	0.0036	0.0042	0.0045
Q	0.0048	0.0057	0.0085	0.0141

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0011	0.0011	0.0014	0.0014
CK	0.0021	0.0022	0.0029	0.0029
SN	0.0021	0.0024	0.0024	0.0024

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0759	0.0796	0.0753	0.0845	3.6065	2.6646	1.3567	0.6991
CK → Q↓	0.0839	0.0856	0.0737	0.0854	3.2019	1.6374	0.7920	0.4040
SN → Q↑	0.0828	0.0922	0.1036	0.1208	3.5953	2.6541	1.3566	0.6979

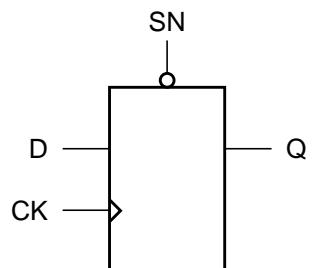
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CK	0.0664	0.0508	0.0586	0.0586
	setup↓ → CK	0.0547	0.0547	0.0625	0.0586
	hold↑ → CK	-0.0273	-0.0156	-0.0078	-0.0078
	hold↓ → CK	-0.0234	-0.0195	-0.0234	-0.0195
CK	minpwh	0.0492	0.0492	0.0444	0.0444
	minpwl	0.1125	0.1028	0.0930	0.0930
SN	minpwl	0.0687	0.0784	0.0882	0.1028
	recovery	0.0273	0.0234	0.0391	0.0391
	removal	-0.0156	-0.0117	-0.0195	-0.0195

Cell Description

The DFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol



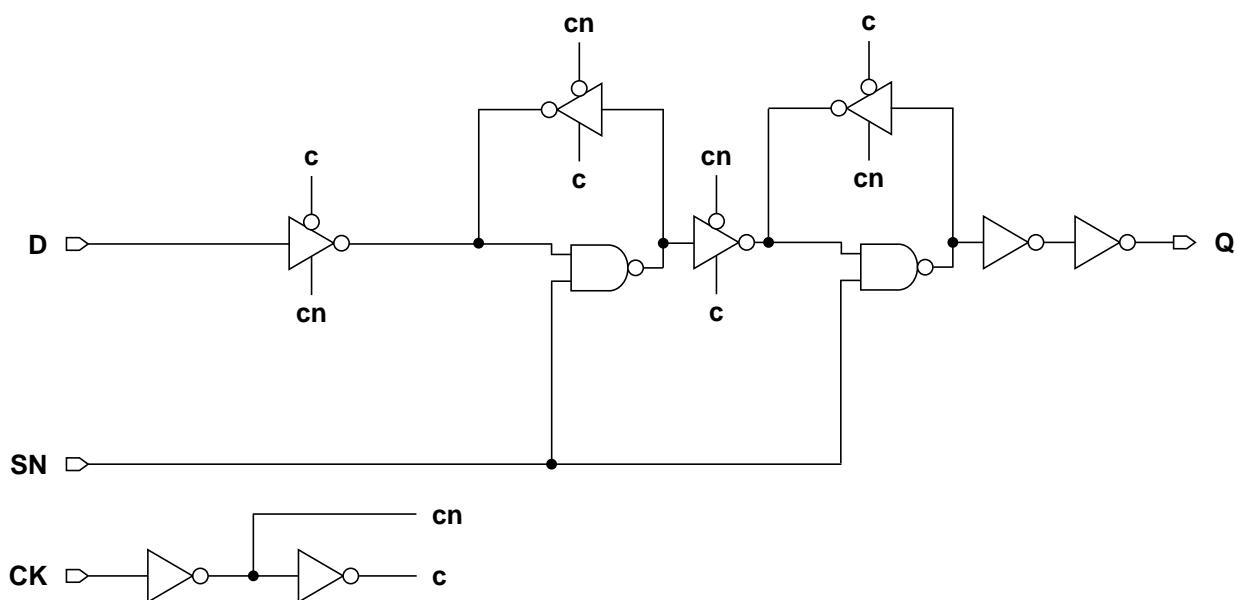
Functions

SN	D	CK	Q[n+1]
0	x	x	1
1	0	—	0
1	1	—	1
1	x	—	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSQXL	2.52	5.60
DFFSQX1	2.52	5.88
DFFSQX2	2.52	5.88
DFFSQX4	2.52	6.16

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
D	0.0047	0.0048	0.0048	0.0049
CK	0.0098	0.0099	0.0099	0.0101
SN	0.0010	0.0010	0.0010	0.0012
Q	0.0041	0.0046	0.0055	0.0085

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0011	0.0011	0.0011	0.0011
CK	0.0018	0.0018	0.0018	0.0018
SN	0.0019	0.0019	0.0019	0.0019

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1161	0.1187	0.1238	0.1350	5.4359	3.6030	2.6370	1.3480
CK → Q↓	0.1257	0.1330	0.1364	0.1505	4.5311	3.1400	1.5969	0.8144
SN → Q↑	0.0962	0.1008	0.1052	0.1150	5.4191	3.5945	2.6341	1.3465

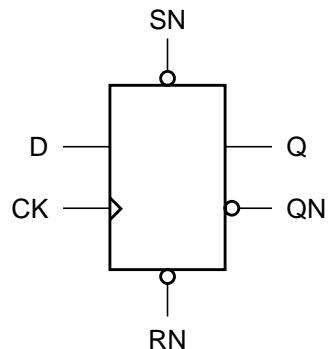
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0547	0.0586	0.0547	0.0547
	setup↓ → CK	0.0586	0.0586	0.0586	0.0586
	hold↑ → CK	-0.0195	-0.0195	-0.0195	-0.0195
	hold↓ → CK	-0.0117	-0.0117	-0.0117	-0.0156
CK	minpwh	0.0736	0.0784	0.0784	0.0882
	minpwl	0.0541	0.0590	0.0590	0.0590
SN	minpwl	0.0687	0.0687	0.0736	0.0784
	recovery	-0.0234	-0.0195	-0.0195	-0.0234
	removal	0.0391	0.0391	0.0391	0.0391

Cell Description

The DFFSR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Logic Symbol



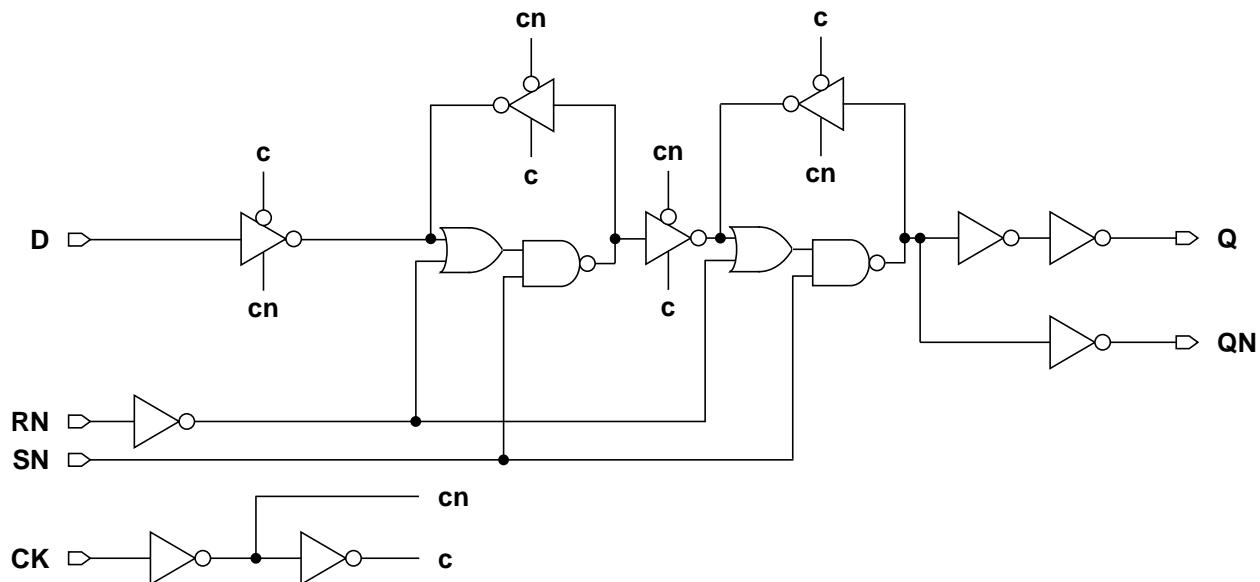
Functions

RN	SN	D	CK	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	✓	0	1
1	1	1	✓	1	0
1	1	x	✗	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSRXL	2.52	7.84
DFFSRX1	2.52	8.12
DFFSRX2	2.52	8.40
DFFSRX4	2.52	10.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0055	0.0055	0.0059	0.0092
CK	0.0108	0.0108	0.0113	0.0155
SN	0.0012	0.0012	0.0013	0.0017
RN	0.0026	0.0027	0.0029	0.0033
Q	0.0061	0.0073	0.0088	0.0140

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0010	0.0010	0.0010	0.0012
CK	0.0016	0.0016	0.0017	0.0020
SN	0.0020	0.0020	0.0022	0.0029
RN	0.0011	0.0011	0.0011	0.0011

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q \uparrow	0.1495	0.1568	0.1553	0.1581	5.6743	3.6605	2.6560	1.3725
CK → Q \downarrow	0.1524	0.1607	0.1603	0.1682	4.2120	3.0995	1.5886	0.8081
SN → Q \uparrow	0.1245	0.1299	0.1485	0.2057	5.6240	3.6324	2.6514	1.3721
SN → Q \downarrow	0.1196	0.1270	0.1376	0.1607	4.1852	3.0880	1.5847	0.8083
RN → Q \downarrow	0.1385	0.1460	0.1656	0.2044	4.1747	3.0841	1.5832	0.8082
CK → QN \uparrow	0.1073	0.1083	0.1016	0.0950	6.1146	3.8969	2.7137	1.4023
CK → QN \downarrow	0.1115	0.1205	0.1087	0.0965	5.7511	3.9663	1.8912	0.8920
SN → QN \uparrow	0.0750	0.0756	0.0773	0.0818	5.9478	3.7983	2.6992	1.4182
SN → QN \downarrow	0.0904	0.0967	0.1026	0.1325	4.7719	3.3731	1.7592	0.9332
RN → QN \uparrow	0.0946	0.0953	0.1056	0.1251	5.8897	3.7723	2.6922	1.4172

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0781	0.0742	0.0547	0.0625
	setup↓ → CK	0.0703	0.0664	0.0742	0.0703
	hold↑ → CK	-0.0195	-0.0195	-0.0195	-0.0234
	hold↓ → CK	-0.0156	-0.0156	-0.0234	-0.0156
CK	minpwh	0.1028	0.1076	0.1028	0.1028
	minpwl	0.0687	0.0687	0.0638	0.0638
SN	minpwl	0.0930	0.0930	0.1076	0.1563
	recovery	-0.0195	-0.0195	-0.0234	-0.0312
	removal	0.0391	0.0391	0.0430	0.0547
RN	minpwl	0.0833	0.0882	0.0979	0.1271
	recovery	0.0664	0.0664	0.0469	0.0469
	removal	-0.0234	-0.0234	-0.0156	-0.0156

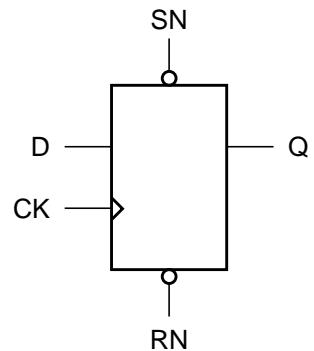
Cell Description

The DFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Functions

RN	SN	D	CK	Q[n+1]
0	1	x	x	0
1	0	x	x	1
0	0	x	x	1
1	1	0	/	0
1	1	1	/	1
1	1	x	/	Q[n]

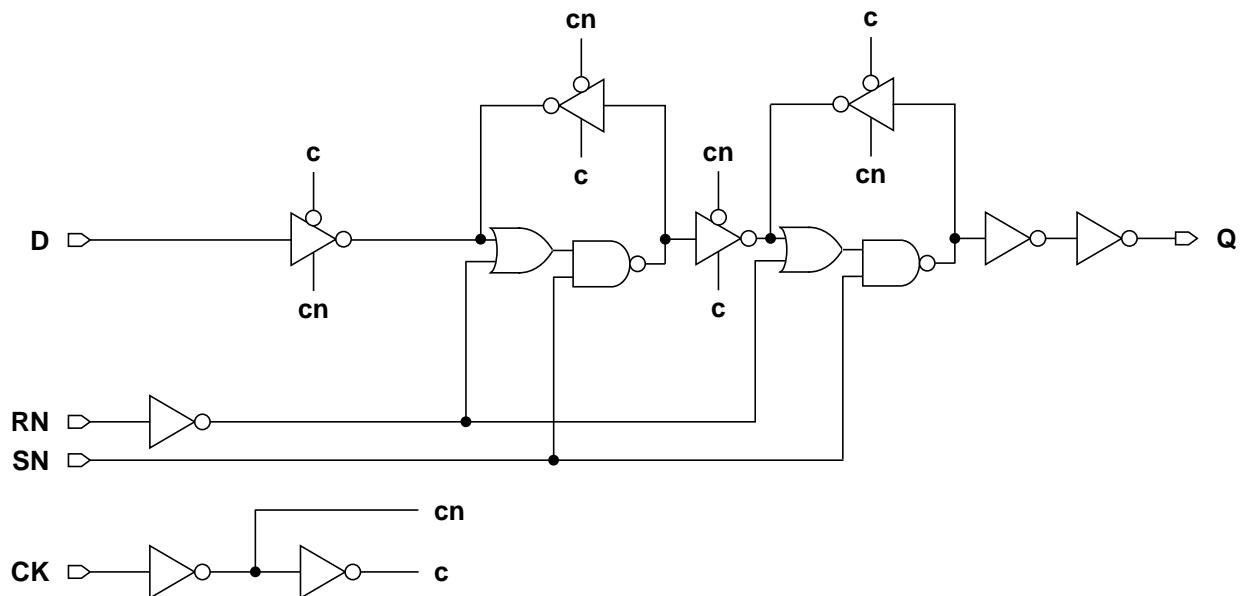
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFSRHQX1	2.52	9.24
DFFSRHQX2	2.52	9.24
DFFSRHQX4	2.52	11.76
DFFSRHQX8	2.52	12.60

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
D	0.0074	0.0085	0.0123	0.0126
CK	0.0142	0.0158	0.0220	0.0224
SN	0.0041	0.0043	0.0054	0.0057
RN	0.0014	0.0016	0.0024	0.0025
Q	0.0054	0.0064	0.0096	0.0156

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0012	0.0012	0.0014	0.0014
CK	0.0022	0.0022	0.0027	0.0027
SN	0.0022	0.0025	0.0032	0.0032
RN	0.0019	0.0021	0.0031	0.0031

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0902	0.0865	0.0841	0.0953	3.7482	2.6709	1.3586	0.7050
CK → Q↓	0.0949	0.0863	0.0857	0.0963	3.4021	1.6719	0.8209	0.4208
SN → Q↑	0.1040	0.1120	0.1424	0.1633	3.6381	2.6450	1.3578	0.7025
SN → Q↓	0.2037	0.1758	0.1527	0.1879	3.6708	1.8697	0.8986	0.4687
RN → Q↓	0.1811	0.1533	0.1204	0.1552	3.6781	1.8752	0.9000	0.4693

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CK	0.0742	0.0625	0.0742	0.0742
	setup↓ → CK	0.0586	0.0547	0.0469	0.0469
	hold↑ → CK	-0.0195	-0.0156	-0.0234	-0.0195
	hold↓ → CK	-0.0195	-0.0195	-0.0117	-0.0117
CK	minpwh	0.0492	0.0492	0.0541	0.0541
	minpw1	0.1222	0.1125	0.1125	0.1174
SN	minpw1	0.0882	0.0979	0.1222	0.1417
	recovery	0.0312	0.0234	0.0195	0.0195
	removal	-0.0156	-0.0117	-0.0078	-0.0078
RN	minpw1	0.1661	0.1417	0.1125	0.1466
	recovery	-0.0117	-0.0156	-0.0156	-0.0156
	removal	0.0352	0.0391	0.0469	0.0469

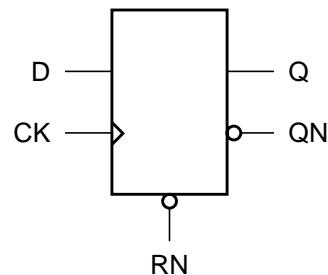
Cell Description

The DFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-low reset (RN).

Functions

RN	D	CK	Q[n+1]	QN[n+1]
0	x	—	0	1
x	x	—	Q[n]	QN[n]
1	0	—	0	1
1	1	—	1	0

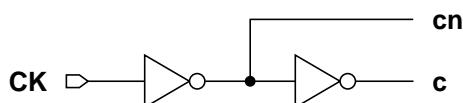
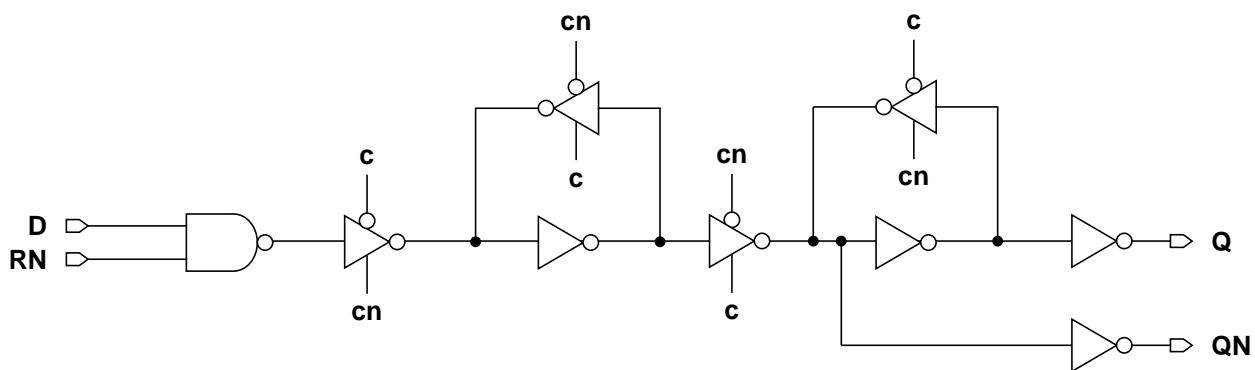
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
DFFTRXL	2.52	5.88
DFFTRX1	2.52	6.16
DFFTRX2	2.52	6.16
DFFTRX4	2.52	8.12

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
D	0.0053	0.0058	0.0066	0.0103
CK	0.0106	0.0112	0.0121	0.0177
RN	0.0056	0.0062	0.0071	0.0117
Q	0.0053	0.0061	0.0078	0.0127

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0011	0.0011	0.0012	0.0017
CK	0.0015	0.0015	0.0015	0.0020
RN	0.0010	0.0010	0.0011	0.0014

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1201	0.1157	0.1209	0.1191	5.6273	3.6174	2.6492	1.3635
CK → Q↓	0.1316	0.1354	0.1382	0.1346	4.1514	3.0777	1.5673	0.7710
CK → QN↑	0.0924	0.0874	0.0877	0.0856	5.7533	3.6466	2.6431	1.3706
CK → QN↓	0.0876	0.0849	0.0822	0.0782	4.6107	3.2373	1.6185	0.7911

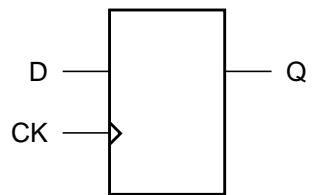
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0664	0.0664	0.0625	0.0508
	setup↓ → CK	0.0938	0.0977	0.0820	0.0586
	hold↑ → CK	-0.0273	-0.0312	-0.0273	-0.0234
	hold↓ → CK	-0.0312	-0.0312	-0.0234	-0.0117
CK	minpwh	0.0784	0.0736	0.0736	0.0687
	minpwl	0.0687	0.0687	0.0687	0.0541
RN	setup↑ → CK	0.0664	0.0703	0.0625	0.0508
	setup↓ → CK	0.1016	0.1016	0.1016	0.1172
	hold↑ → CK	-0.0273	-0.0312	-0.0312	-0.0234
	hold↓ → CK	-0.0312	-0.0312	-0.0352	-0.0391

Cell Description

The DFFYQ cell is a positive-edge triggered, static D-type flip-flop to be used in synchronizing circuitry between asynchronous systems. The cell has a single output (Q) and overdriven feedback loops to increase MTBF due to metastability.

Logic Symbol



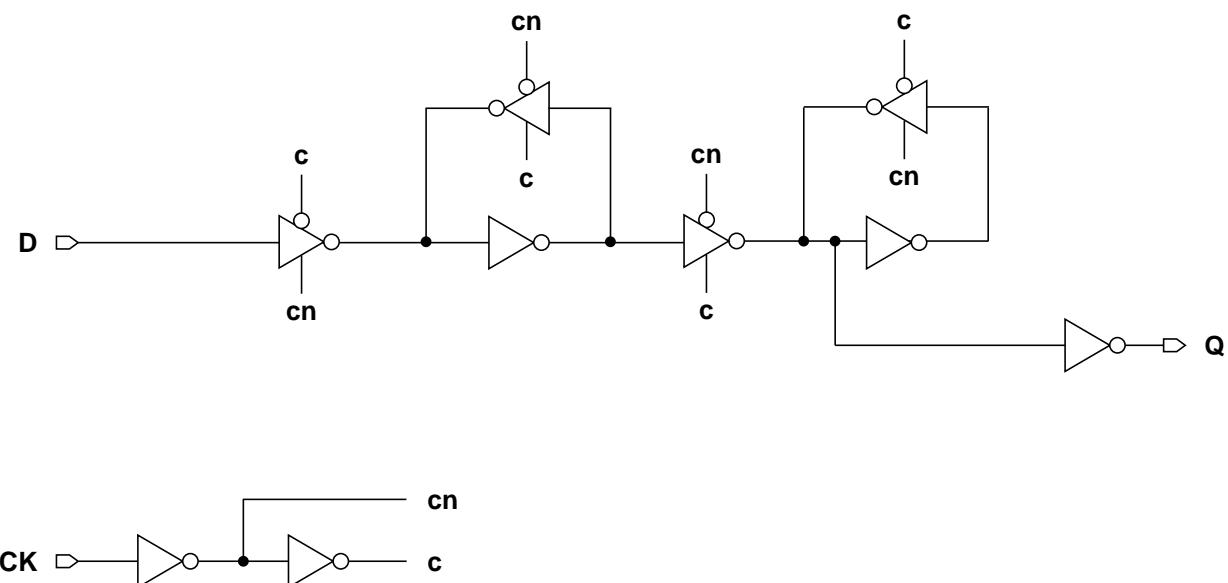
Functions

D	CK	Q[n+1]
0	—/—	0
1	—/—	1
x	—\—	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFYQX2	2.52	6.16

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)
	X2
D	0.0081
CK	0.0147
Q	0.0054

Pin Capacitance

Pin	Capacitance (pF)
	X2
D	0.0020
CK	0.0022

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	X2
CK → Q↑	0.0902	2.6103
CK → Q↓	0.0994	1.6836

Timing Constraints at 25°C, 1.0V, Typical Process

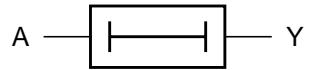
Pin	Requirement	Interval (ns)
		X2
D	setup↑ → CK	0.0195
	setup↓ → CK	0.0391
	hold↑ → CK	-0.0117
	hold↓ → CK	-0.0078
CK	minpwh	0.0784
	minpwl	0.0541

Cell Description

The DLY1 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



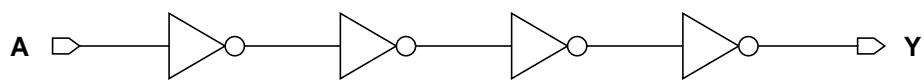
Functions

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (um)	Width (um)
DLY1X1	2.52	2.52
DLY1X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X1	X4
A	0.0059	0.0087

Pin Capacitance

Pin	Capacitance (pF)	
	X1	X4
A	0.0013	0.0017

Delays at 25°C, 1.0V, Typical Process

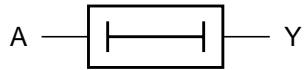
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	X4	X1	X4
A → Y↑	0.0652	0.0622	3.7841	1.3458
A → Y↓	0.0832	0.0787	2.9670	1.4817

Cell Description

The DLY2 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



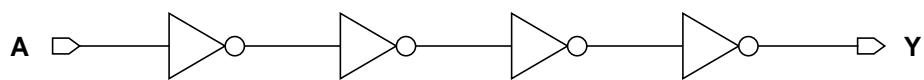
Functions

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (um)	Width (um)
DLY2X1	2.52	2.52
DLY2X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X1	X4
A	0.0069	0.0105

Pin Capacitance

Pin	Capacitance (pF)	
	X1	X4
A	0.0013	0.0017

Delays at 25°C, 1.0V, Typical Process

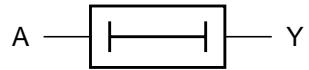
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	X4	X1	X4
A → Y↑	0.1124	0.1085	3.8233	1.3565
A → Y↓	0.1284	0.1282	3.1239	1.5234

Cell Description

The DLY3 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



Functions

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (um)	Width (um)
DLY3X1	2.52	2.52
DLY3X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X1	X4
A	0.0081	0.0125

Pin Capacitance

Pin	Capacitance (pF)	
	X1	X4
A	0.0014	0.0018

Delays at 25°C, 1.0V, Typical Process

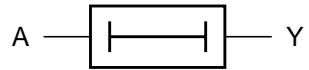
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	X4	X1	X4
A → Y↑	0.1699	0.1635	3.8843	1.3762
A → Y↓	0.1776	0.1798	3.3245	1.5720

Cell Description

The DLY4 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



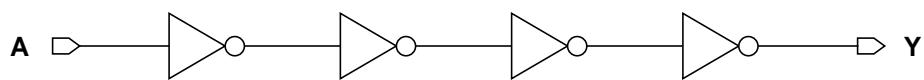
Functions

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (um)	Width (um)
DLY4X1	2.52	2.52
DLY4X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X1	X4
A	0.0093	0.0146

Pin Capacitance

Pin	Capacitance (pF)	
	X1	X4
A	0.0014	0.0018

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	X4	X1	X4
A → Y↑	0.2404	0.2312	3.9677	1.4025
A → Y↓	0.2341	0.2397	3.5502	1.6306

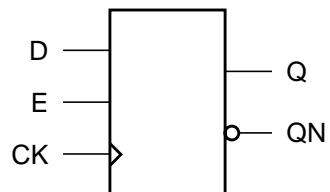
Cell Description

The EDFF cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E).

Functions

E	D	CK	Q[n+1]	QN[n+1]
0	x	x	Q[n]	QN[n]
1	0	—	0	1
1	1	—	1	0
1	x	—	Q[n]	QN[n]

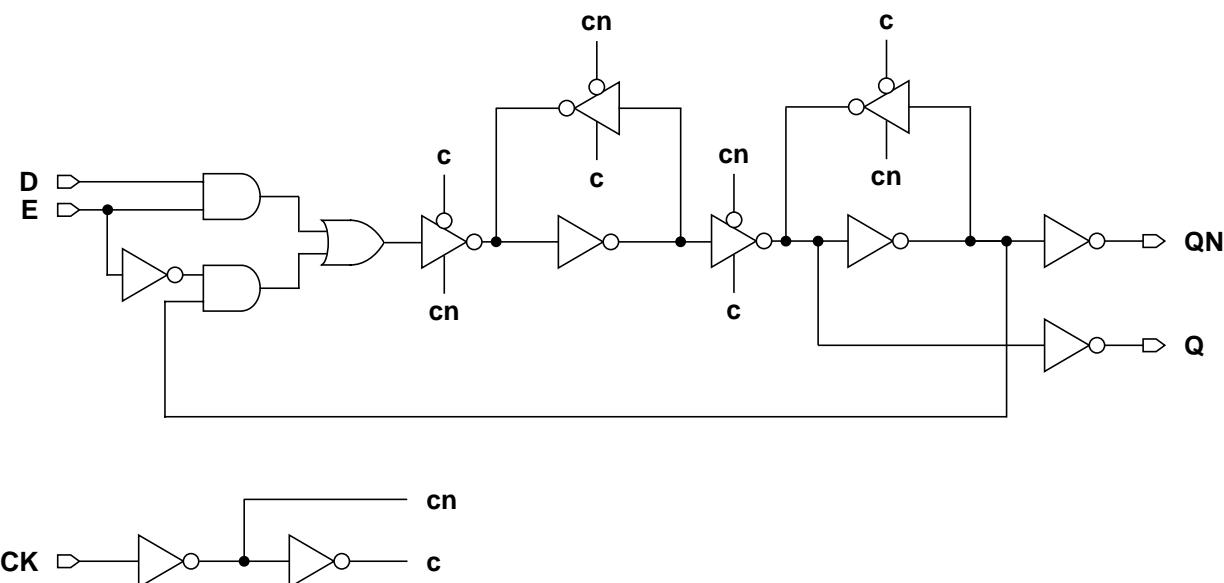
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
EDFFXL	2.52	7.56
EDFFX1	2.52	7.56
EDFFX2	2.52	7.56
EDFFX4	2.52	9.24

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
D	0.0059	0.0061	0.0056	0.0067
CK	0.0097	0.0099	0.0103	0.0119
E	0.0085	0.0087	0.0082	0.0089
Q	0.0061	0.0070	0.0089	0.0140

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0014	0.0014	0.0010	0.0011
CK	0.0015	0.0015	0.0015	0.0017
E	0.0026	0.0026	0.0021	0.0022

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.0974	0.0946	0.0954	0.0996	5.6458	3.5982	2.6136	1.3713
CK → Q↓	0.1129	0.1092	0.0992	0.0945	5.3027	3.4193	1.6488	0.8114
CK → QN↑	0.1574	0.1529	0.1518	0.1429	5.6775	3.6100	2.6403	1.3663
CK → QN↓	0.1514	0.1550	0.1590	0.1529	4.7974	3.2443	1.6346	0.7802

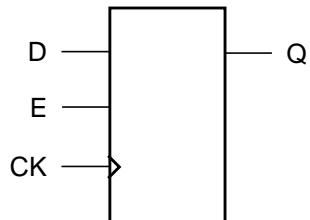
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0859	0.0859	0.0625	0.0625
	setup↓ → CK	0.0820	0.0820	0.1914	0.1992
	hold↑ → CK	-0.0625	-0.0625	-0.0430	-0.0430
	hold↓ → CK	-0.0469	-0.0469	-0.1406	-0.1406
CK	minpwh	0.1028	0.0979	0.0930	0.0833
	minpwl	0.0882	0.0930	0.0784	0.0736
E	setup↑ → CK	0.1016	0.1016	0.2070	0.2188
	setup↓ → CK	0.1055	0.1094	0.1680	0.1641
	hold↑ → CK	-0.0703	-0.0703	-0.0469	-0.0469
	hold↓ → CK	-0.0430	-0.0430	-0.0742	-0.0703

Cell Description

The EDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a synchronous, active-high enable (E). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



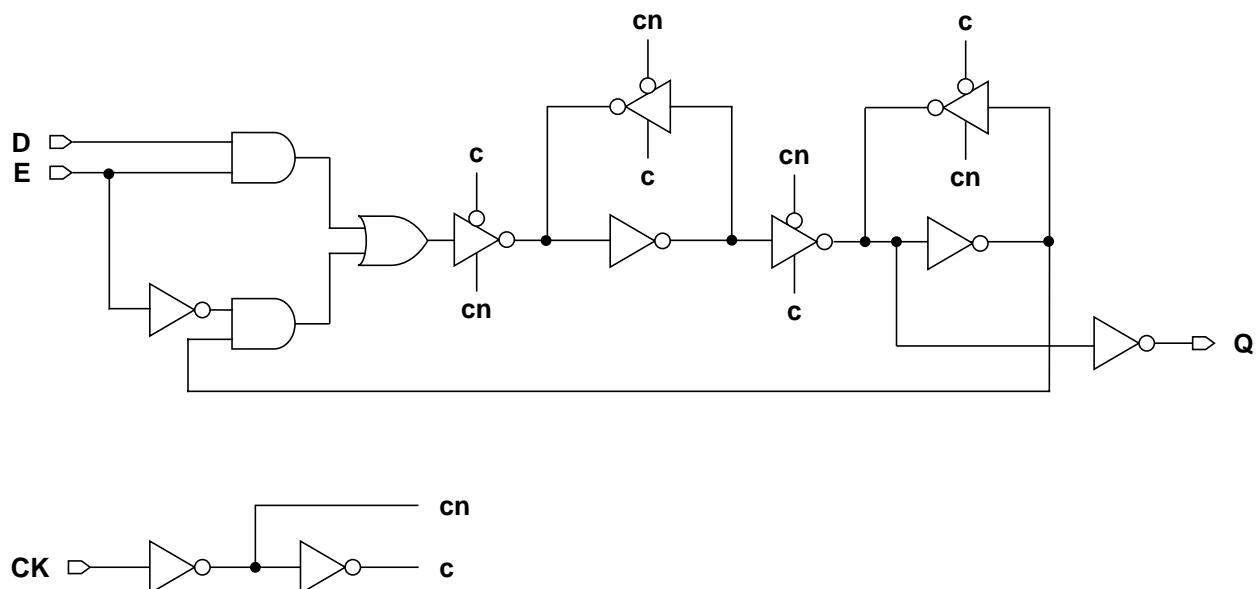
Functions

E	D	CK	Q[n+1]
0	x	x	Q[n]
1	0	—/—	0
1	1	—/—	1
x	x	—\—	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFHQX1	2.52	8.68
EDFFHQX2	2.52	8.96
EDFFHQX4	2.52	11.20
EDFFHQX8	2.52	12.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
D	0.0092	0.0107	0.0155	0.0158
CK	0.0153	0.0173	0.0242	0.0245
E	0.0101	0.0112	0.0152	0.0155
Q	0.0048	0.0060	0.0084	0.0136

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D	0.0018	0.0015	0.0024	0.0023
CK	0.0022	0.0023	0.0033	0.0033
E	0.0031	0.0032	0.0032	0.0032

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0778	0.0727	0.0680	0.0767	3.6170	2.6389	1.3482	0.6950
CK → Q↓	0.0850	0.0773	0.0722	0.0821	3.1927	1.6066	0.7818	0.3977

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D	setup↑ → CK	0.0664	0.0508	0.0508	0.0508
	setup↓ → CK	0.0586	0.0664	0.0625	0.0625
	hold↑ → CK	-0.0273	-0.0195	-0.0195	-0.0156
	hold↓ → CK	-0.0273	-0.0391	-0.0312	-0.0312
CK	minpwh	0.0492	0.0444	0.0444	0.0492
	minpwl	0.1125	0.0979	0.0833	0.0833
E	setup↑ → CK	0.0586	0.0586	0.0586	0.0586
	setup↓ → CK	0.0781	0.0820	0.0898	0.0898
	hold↑ → CK	-0.0391	-0.0312	-0.0273	-0.0312
	hold↓ → CK	-0.0586	-0.0586	-0.0664	-0.0664

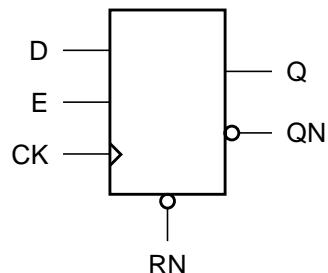
Cell Description

The EDFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E) and synchronous active-low reset (RN).

Functions

RN	E	D	CK	Q[n+1]	QN[n+1]
0	x	x	/\	0	1
x	x	x	\/\	Q[n]	QN[n]
1	0	x	/\	Q[n]	QN[n]
1	1	0	/\	0	1
1	1	1	/\	1	0

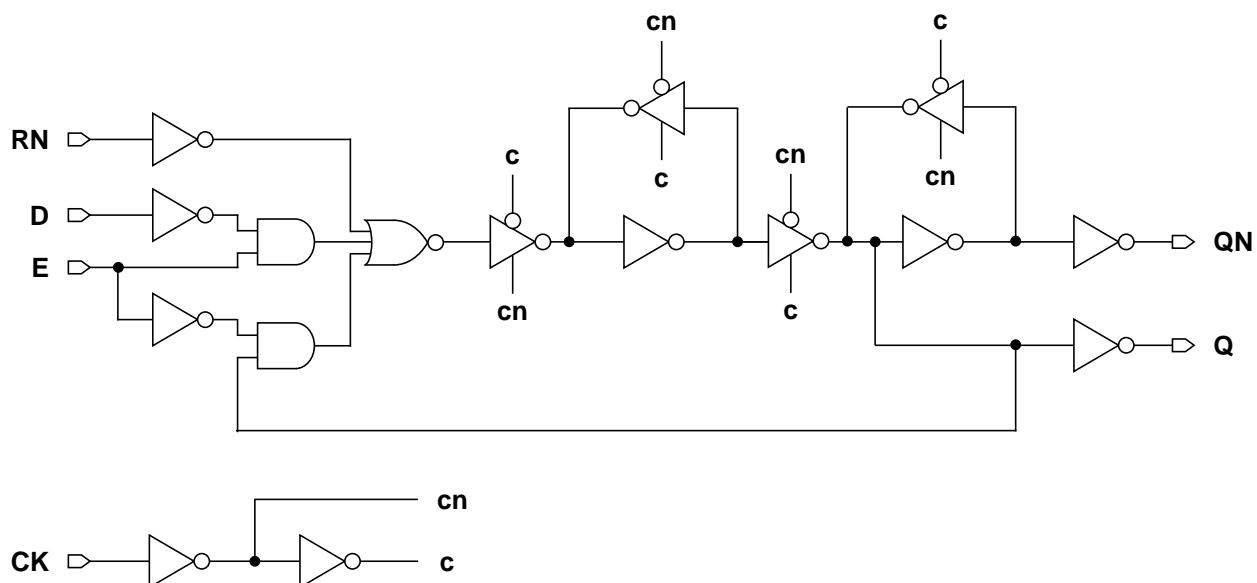
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
EDFFTRXL	2.52	8.40
EDFFTRX1	2.52	8.68
EDFFTRX2	2.52	8.68
EDFFTRX4	2.52	10.08

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
D	0.0055	0.0056	0.0057	0.0068
CK	0.0109	0.0110	0.0113	0.0131
E	0.0082	0.0083	0.0085	0.0096
RN	0.0060	0.0061	0.0063	0.0073
Q	0.0061	0.0069	0.0087	0.0140

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0011	0.0011	0.0011	0.0011
CK	0.0015	0.0015	0.0015	0.0017
E	0.0027	0.0027	0.0027	0.0027
RN	0.0010	0.0010	0.0010	0.0010

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1062	0.1006	0.0996	0.0979	5.7409	3.6315	2.6778	1.3770
CK → Q↓	0.1149	0.1106	0.1046	0.0944	4.8448	3.3437	1.6574	0.8105
CK → QN↑	0.1622	0.1535	0.1556	0.1427	5.6961	3.6539	2.6687	1.3677
CK → QN↓	0.1597	0.1629	0.1616	0.1511	4.3685	3.1896	1.6201	0.7810

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0781	0.0781	0.0781	0.0898
	setup↓ → CK	0.2031	0.2031	0.2031	0.2266
	hold↑ → CK	-0.0625	-0.0586	-0.0586	-0.0664
	hold↓ → CK	-0.1641	-0.1562	-0.1523	-0.1641
CK	minpwh	0.1076	0.0979	0.0930	0.0833
	minpw1	0.0882	0.0930	0.0882	0.0979
E	setup↑ → CK	0.2227	0.2266	0.2227	0.2461
	setup↓ → CK	0.1719	0.1719	0.1680	0.1836
	hold↑ → CK	-0.0625	-0.0625	-0.0625	-0.0703
	hold↓ → CK	-0.0977	-0.0938	-0.0938	-0.0977
RN	setup↑ → CK	0.0859	0.0859	0.0859	0.0977
	setup↓ → CK	0.1484	0.1523	0.1523	0.1719
	hold↑ → CK	-0.0703	-0.0703	-0.0664	-0.0742
	hold↓ → CK	-0.1055	-0.0977	-0.0977	-0.1055

Cell Description

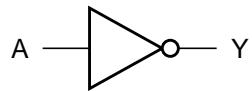
The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$$Y = \bar{A}$$

Functions

A	Y
0	1
1	0

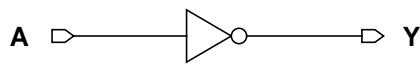
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
INVXL	2.52	0.84
INVX1	2.52	0.84
INVX2	2.52	0.84
INVX3	2.52	1.12
INVX4	2.52	1.12
INVX5	2.52	1.40
INVX6	2.52	1.68
INVX8	2.52	1.96
INVX10	2.52	2.24
INVX12	2.52	2.52
INVX14	2.52	3.08
INVX16	2.52	3.36
INVX18	2.52	3.64
INVX20	2.52	3.92

Functional Schematic



AC Power

Pin	Power (μ W/MHz)						
	XL	X1	X2	X3	X4	X5	X6
A	0.0012	0.0017	0.0024	0.0033	0.0043	0.0050	0.0066
Pin	Power (μ W/MHz)						
	X8	X10	X12	X14	X16	X18	X20
A	0.0081	0.0100	0.0123	0.0147	0.0165	0.0190	0.0203

Pin Capacitance

Pin	Capacitance (pF)						
	XL	X1	X2	X3	X4	X5	X6
A	0.0012	0.0017	0.0024	0.0034	0.0046	0.0051	0.0068
Pin	Capacitance (pF)						
	X8	X10	X12	X14	X16	X18	X20
A	0.0084	0.0103	0.0128	0.0151	0.0171	0.0195	0.0210

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	XL	X1	X2	X3	X4	X5	X6
A → Y↑	0.0118	0.0111	0.0114	0.0109	0.0105	0.0111	0.0109
A → Y↓	0.0103	0.0103	0.0086	0.0080	0.0079	0.0082	0.0079
Description	Intrinsic Delay (ns)						
	X8	X10	X12	X14	X16	X18	X20
A → Y↑	0.0109	0.0111	0.0107	0.0111	0.0109	0.0110	0.0110
A → Y↓	0.0081	0.0079	0.0078	0.0080	0.0079	0.0079	0.0080

Delays at 25°C, 1.0V, Typical Process

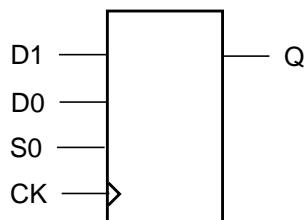
Description	K_{load} (ns/pF)						
	XL	X1	X2	X3	X4	X5	X6
A → Y↑	5.4320	3.5048	2.5850	1.7995	1.3230	1.1952	0.8984
A → Y↓	4.2662	2.9704	1.4888	0.9844	0.7319	0.6727	0.4829

Description	K_{load} (ns/pF)						
	X8	X10	X12	X14	X16	X18	X20
A → Y↑	0.7263	0.6086	0.4704	0.4049	0.3540	0.3148	0.2918
A → Y↓	0.4018	0.3113	0.2484	0.2110	0.1837	0.1625	0.1524

Cell Description

The MDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a 2-to-1 data select control (S0) for the data inputs (D1, D0). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



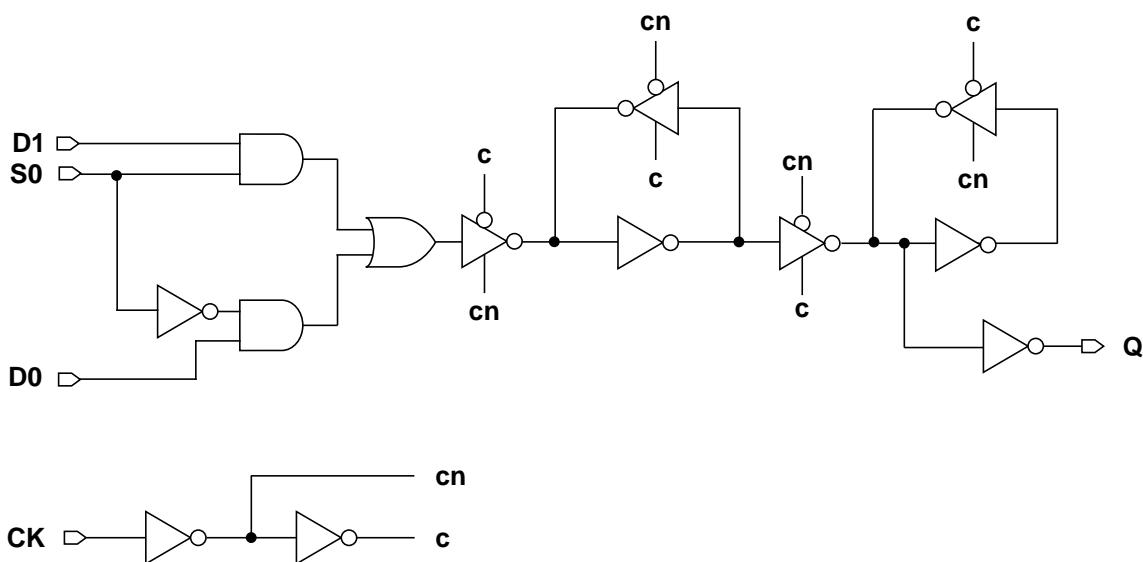
Functions

S0	D1	D0	CK	Q[n+1]
0	x	0	/\	0
0	x	1	/\	1
1	0	x	/\	0
1	1	x	/\	1
x	x	x	\/\	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
MDFFHQX1	2.52	8.12
MDFFHQX2	2.52	8.40
MDFFHQX4	2.52	10.92
MDFFHQX8	2.52	11.76

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
D0	0.0078	0.0097	0.0157	0.0159
D1	0.0084	0.0103	0.0172	0.0174
S0	0.0087	0.0104	0.0167	0.0168
CK	0.0134	0.0150	0.0235	0.0236
Q	0.0041	0.0050	0.0076	0.0131

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
D0	0.0011	0.0014	0.0023	0.0023
D1	0.0011	0.0014	0.0023	0.0023
S0	0.0021	0.0023	0.0028	0.0028
CK	0.0023	0.0022	0.0029	0.0030

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0749	0.0758	0.0673	0.0757	3.6029	2.6188	1.3246	0.6853
CK → Q↓	0.0838	0.0812	0.0745	0.0850	3.2019	1.6016	0.7783	0.3972

Timing Constraints at 25°C, 1.0V, Typical Process

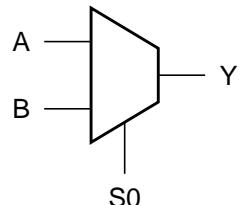
Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
D0	setup↑ → CK	0.0781	0.0742	0.0586	0.0586
	setup↓ → CK	0.0898	0.0742	0.0625	0.0625
	hold↑ → CK	-0.0430	-0.0352	-0.0234	-0.0234
	hold↓ → CK	-0.0586	-0.0430	-0.0352	-0.0312
D1	setup↑ → CK	0.0781	0.0703	0.0586	0.0586
	setup↓ → CK	0.0898	0.0742	0.0664	0.0664
	hold↑ → CK	-0.0391	-0.0352	-0.0234	-0.0234
	hold↓ → CK	-0.0625	-0.0430	-0.0391	-0.0391
S0	setup↑ → CK	0.0859	0.0703	0.0625	0.0625
	setup↓ → CK	0.0938	0.0898	0.0859	0.0859
	hold↑ → CK	-0.0312	-0.0273	-0.0156	-0.0156
	hold↓ → CK	-0.0508	-0.0391	-0.0352	-0.0312
CK	minpwh	0.0492	0.0492	0.0444	0.0492
	minpw1	0.1076	0.1028	0.0882	0.0882

Cell Description

The MX2 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$$

Logic Symbol



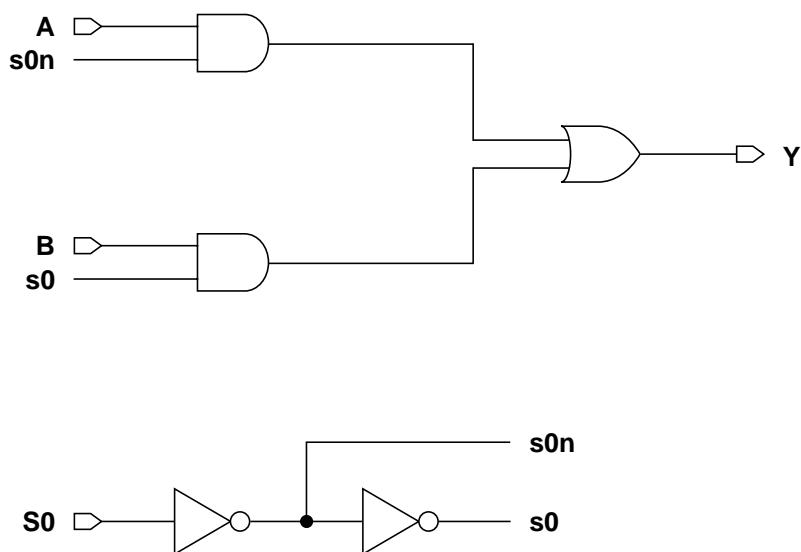
Functions

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX2XL	2.52	2.52
MX2X1	2.52	2.52
MX2X2	2.52	2.80
MX2X3	2.52	3.36
MX2X4	2.52	3.36
MX2X6	2.52	3.92
MX2X8	2.52	4.20

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)						
	XL	X1	X2	X3	X4	X6	X8
S0	0.0044	0.0056	0.0072	0.0100	0.0110	0.0139	0.0177
A	0.0038	0.0048	0.0065	0.0084	0.0098	0.0133	0.0171
B	0.0040	0.0052	0.0071	0.0090	0.0105	0.0144	0.0182

Pin Capacitance

Pin	Capacitance (pF)						
	XL	X1	X2	X3	X4	X6	X8
S0	0.0026	0.0029	0.0034	0.0041	0.0041	0.0042	0.0041
A	0.0014	0.0017	0.0021	0.0024	0.0026	0.0025	0.0025
B	0.0012	0.0015	0.0019	0.0021	0.0021	0.0023	0.0021

Delay Tables at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	XL	X1	X2	X3	X4	X6	X8
S0 → Y↑	0.0598	0.0589	0.0599	0.0647	0.0665	0.0742	0.0780
S0 → Y↓	0.0612	0.0584	0.0501	0.0548	0.0588	0.0725	0.0811
A → Y↑	0.0480	0.0429	0.0440	0.0423	0.0448	0.0521	0.0569
A → Y↓	0.0692	0.0621	0.0552	0.0585	0.0591	0.0696	0.0766
B → Y↑	0.0461	0.0412	0.0422	0.0408	0.0433	0.0496	0.0564
B → Y↓	0.0688	0.0629	0.0562	0.0583	0.0627	0.0704	0.0816

Description	K_{load} (ns/pF)						
	XL	X1	X2	X3	X4	X6	X8
S0 → Y↑	5.6852	3.6262	2.6810	1.8269	1.3708	0.9289	0.7032
S0 → Y↓	4.8397	3.0655	1.5800	1.0436	0.8039	0.5500	0.4223
A → Y↑	5.6900	3.6273	2.6832	1.8283	1.3720	0.9304	0.7042
A → Y↓	4.8409	3.0665	1.5823	1.0512	0.8010	0.5525	0.4235
B → Y↑	5.6896	3.6260	2.6813	1.8287	1.3727	0.9304	0.7050
B → Y↓	4.8438	3.0664	1.5806	1.0462	0.8045	0.5454	0.4262

Cell Description

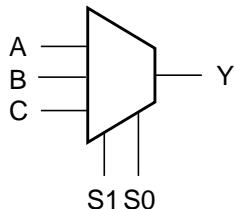
The MX3 cell is a 3-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \cdot \overline{S1} \cdot A) + (S0 \cdot \overline{S1} \cdot B) + (S1 \cdot C)$$

Functions

S1	S0	A	B	C	Y
0	0	0	x	x	0
0	0	1	x	x	1
0	1	x	0	x	0
0	1	x	1	x	1
1	x	x	x	0	0
1	x	x	x	1	1

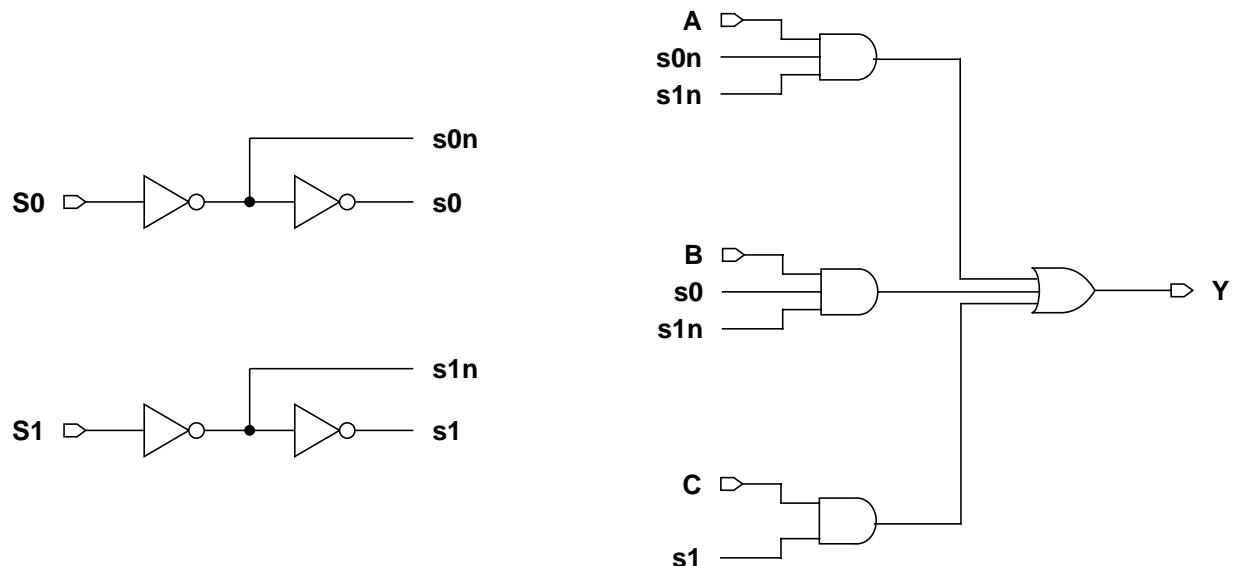
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
MX3XL	2.52	5.04
MX3X1	2.52	5.04
MX3X2	2.52	5.88
MX3X4	2.52	6.16

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
S1	0.0054	0.0067	0.0084	0.0108
S0	0.0068	0.0087	0.0115	0.0143
C	0.0051	0.0062	0.0091	0.0122
B	0.0063	0.0082	0.0111	0.0148
A	0.0059	0.0076	0.0100	0.0136

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S1	0.0028	0.0031	0.0039	0.0040
S0	0.0028	0.0033	0.0050	0.0049
C	0.0011	0.0014	0.0020	0.0024
B	0.0014	0.0018	0.0023	0.0024
A	0.0015	0.0020	0.0023	0.0024

Delays at 25°C, 1.0V, Typical Process

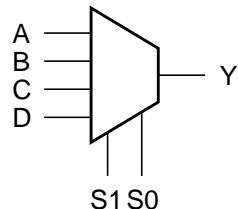
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S1 → Y↑	0.0621	0.0615	0.0617	0.0669	5.6682	3.5985	2.6234	1.3513
S1 → Y↓	0.0623	0.0621	0.0479	0.0604	4.6608	3.2734	1.6686	0.8744
S0 → Y↑	0.0824	0.0807	0.0824	0.0883	5.6829	3.6011	2.6257	1.3518
S0 → Y↓	0.0918	0.0878	0.0822	0.0920	5.1539	3.4950	1.7375	0.8918
C → Y↑	0.0535	0.0491	0.0458	0.0459	5.5616	3.5552	2.6074	1.3363
C → Y↓	0.0793	0.0721	0.0634	0.0641	4.6806	3.2769	1.6075	0.8038
B → Y↑	0.0685	0.0645	0.0634	0.0691	5.6811	3.6065	2.6275	1.3526
B → Y↓	0.0960	0.0902	0.0844	0.0932	5.1689	3.5057	1.7445	0.8938
A → Y↑	0.0705	0.0644	0.0645	0.0707	5.6873	3.6013	2.6268	1.3524
A → Y↓	0.0941	0.0871	0.0807	0.0899	5.1569	3.4974	1.7404	0.8924

Cell Description

The MX4 cell is a 4-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \cdot \overline{S1} \cdot A) + (S0 \cdot \overline{S1} \cdot B) + (\overline{S0} \cdot S1 \cdot C) + (S0 \cdot S1 \cdot D)$$

Logic Symbol



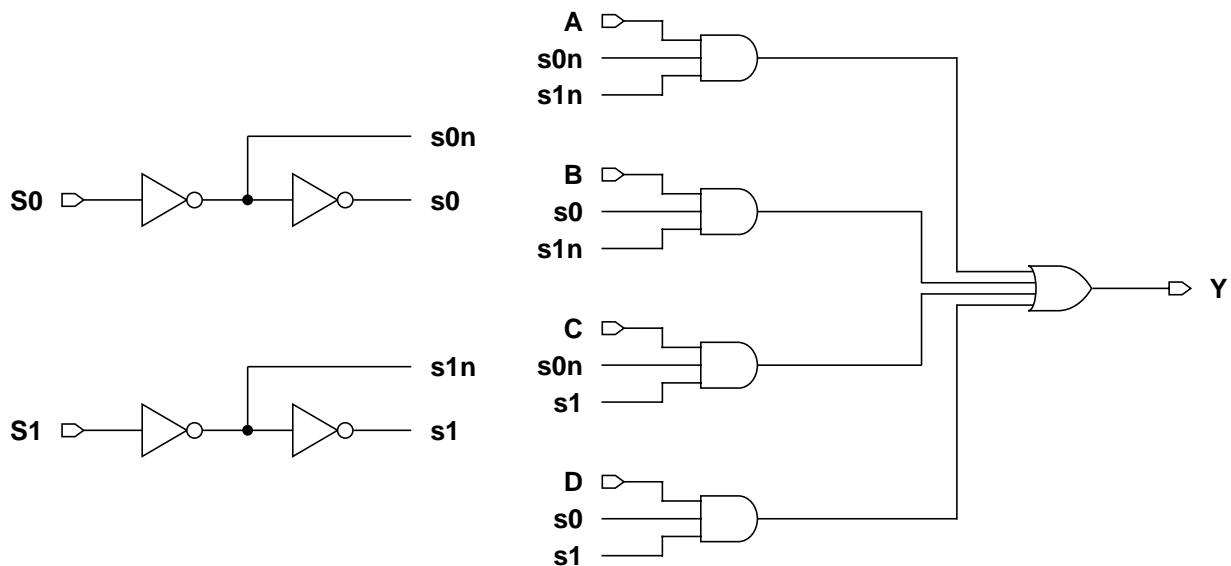
Functions

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX4XL	2.52	6.72
MX4X1	2.52	7.00
MX4X2	2.52	7.28
MX4X4	2.52	7.84

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
S0	0.0098	0.0115	0.0151	0.0188
S1	0.0054	0.0065	0.0087	0.0113
A	0.0061	0.0075	0.0099	0.0138
B	0.0065	0.0081	0.0110	0.0149
C	0.0076	0.0091	0.0119	0.0159
D	0.0080	0.0096	0.0128	0.0167

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0061	0.0071	0.0089	0.0089
S1	0.0032	0.0034	0.0040	0.0041
A	0.0015	0.0019	0.0023	0.0023
B	0.0014	0.0017	0.0022	0.0022
C	0.0014	0.0019	0.0023	0.0023
D	0.0014	0.0018	0.0022	0.0023

Delays at 25°C, 1.0V, Typical Process

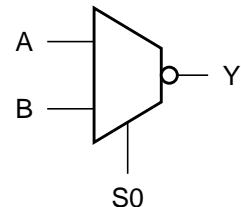
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S0 → Y↑	0.0929	0.0798	0.0802	0.0857	5.7180	4.0042	2.6322	1.3567
S0 → Y↓	0.1085	0.0937	0.0906	0.1007	5.5922	3.5185	1.7717	0.9028
S1 → Y↑	0.0592	0.0611	0.0623	0.0700	5.6561	4.0307	2.6265	1.3548
S1 → Y↓	0.0551	0.0565	0.0526	0.0640	5.4243	3.5130	1.7557	0.8982
A → Y↑	0.0673	0.0614	0.0648	0.0706	5.6650	3.9934	2.6274	1.3543
A → Y↓	0.0923	0.0879	0.0819	0.0930	5.4537	3.5286	1.7611	0.9012
B → Y↑	0.0671	0.0708	0.0656	0.0722	5.6672	4.0387	2.6284	1.3561
B → Y↓	0.0946	0.0856	0.0845	0.0963	5.4622	3.4686	1.7626	0.9049
C → Y↑	0.0730	0.0633	0.0675	0.0730	5.7199	4.0043	2.6331	1.3570
C → Y↓	0.1025	0.0896	0.0888	0.0988	5.5983	3.5147	1.7733	0.9033
D → Y↑	0.0701	0.0641	0.0658	0.0713	5.7066	4.0184	2.6327	1.3570
D → Y↓	0.1038	0.0976	0.0905	0.1008	5.6084	3.5635	1.7786	0.9066

Cell Description

The MXI2 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(S0 \bullet A)} + (S0 \bullet B)$$

Logic Symbol



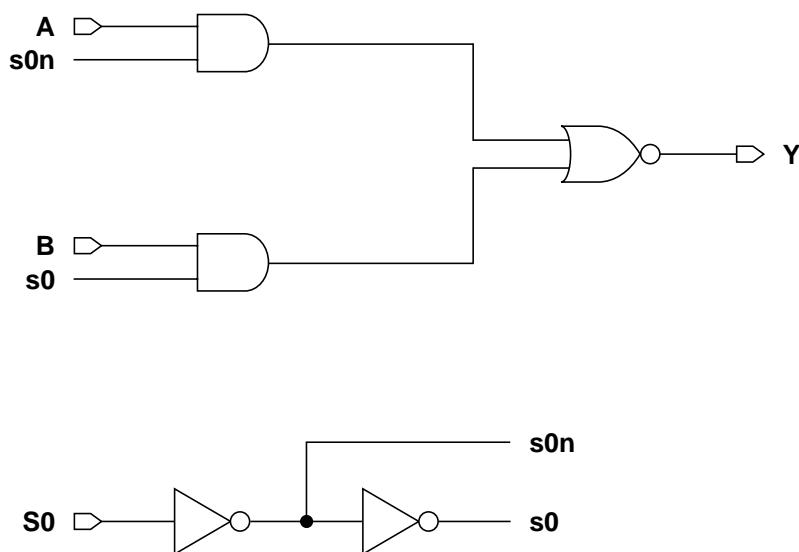
Functions

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI2XL	2.52	2.24
MXI2X1	2.52	2.24
MXI2X2	2.52	3.08
MXI2X3	2.52	4.48
MXI2X4	2.52	4.48
MXI2X6	2.52	6.16
MXI2X8	2.52	8.68

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)						
	XL	X1	X2	X3	X4	X6	X8
S0	0.0035	0.0044	0.0063	0.0093	0.0110	0.0151	0.0219
A	0.0024	0.0031	0.0050	0.0079	0.0092	0.0136	0.0185
B	0.0030	0.0038	0.0059	0.0087	0.0104	0.0158	0.0227

Pin Capacitance

Pin	Capacitance (pF)						
	XL	X1	X2	X3	X4	X6	X8
S0	0.0026	0.0031	0.0042	0.0060	0.0068	0.0097	0.0137
A	0.0012	0.0016	0.0024	0.0036	0.0044	0.0067	0.0089
B	0.0013	0.0017	0.0024	0.0036	0.0045	0.0067	0.0089

Delay Tables at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	XL	X1	X2	X3	X4	X6	X8
S0 → Y↑	0.0274	0.0256	0.0275	0.0278	0.0271	0.0232	0.0247
S0 → Y↓	0.0344	0.0354	0.0368	0.0368	0.0357	0.0311	0.0324
A → Y↑	0.0284	0.0244	0.0266	0.0275	0.0263	0.0252	0.0260
A → Y↓	0.0252	0.0237	0.0204	0.0215	0.0201	0.0196	0.0200
B → Y↑	0.0315	0.0267	0.0294	0.0288	0.0273	0.0273	0.0290
B → Y↓	0.0252	0.0226	0.0187	0.0183	0.0172	0.0166	0.0177

Description	K _{load} (ns/pF)						
	XL	X1	X2	X3	X4	X6	X8
S0 → Y↑	7.6513	5.0443	3.3742	2.2399	1.8071	1.2069	0.8837
S0 → Y↓	5.4477	3.7766	1.9889	1.3447	1.0491	0.7148	0.5167
A → Y↑	7.5938	5.0113	3.3665	2.2448	1.8109	1.2110	0.8910
A → Y↓	5.8360	4.0333	2.0826	1.4074	1.0893	0.7373	0.5363
B → Y↑	7.7466	5.0568	3.4008	2.2779	1.8589	1.2215	0.8832
B → Y↓	5.8717	4.0322	2.0742	1.4007	1.1428	0.7172	0.5250

Cell Description

The MXI2D cell is a 2-to-1 multiplexer with inverted output. The state of the select input S0 determines which data input A, B is presented to the output Y. The output Y is represented by the logic equation:

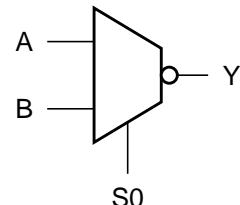
$$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$$

NOTE: The MXI2D cell architecture uses transmission gate inputs for the data input pins and a double-buffered select signal to minimize the risk associated with transmission gate inputs. Do not drive MXI2D inputs from MXI2, ACCSHCIN, ACCSHCON, ACHCIN, ACHCON, ADDH, AFHCIN, AFHCON, AHHCIN, AND AHHCON cells. Furthermore, special care should be taken in designs that use multiple voltage domains for standard cell regions. Do not allow high voltage signals to be coupled into the input pins, A and B, when the cell is used in a low voltage domain; otherwise, it may be possible for the cell to latch. If your design methodology does not permit cells with transmission gate inputs, the MXI2 cell may be used as an alternative.

Functions

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
MXI2DXL	2.52	2.80
MXI2DX1	2.52	2.80
MXI2DX2	2.52	2.80
MXI2DX4	2.52	4.20

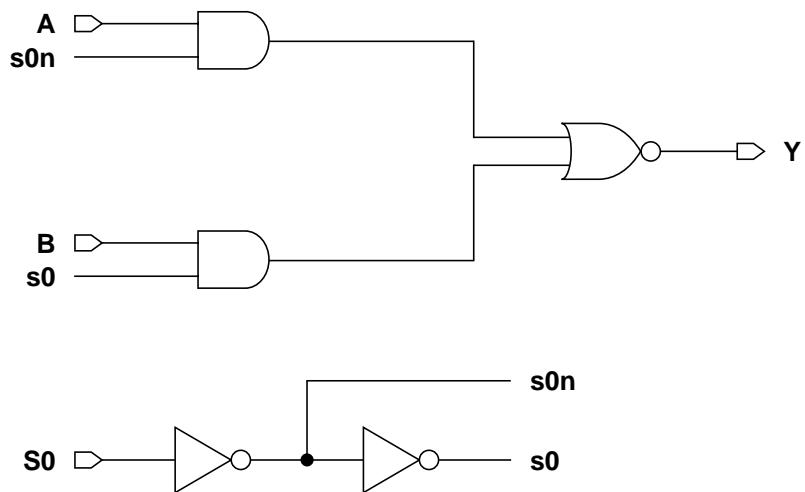
AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
S0	0.0050	0.0058	0.0076	0.0130
A	0.0023	0.0029	0.0042	0.0076
B	0.0024	0.0030	0.0043	0.0078

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0011	0.0011	0.0014	0.0020
A	0.0036	0.0045	0.0063	0.0116
B	0.0041	0.0050	0.0068	0.0123

Functional Schematic



Delay Tables at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
S0 → Y↑	0.0850	0.0840	0.0799	0.0686
S0 → Y↓	0.0951	0.0848	0.0771	0.0728
A → Y↑	0.0267	0.0232	0.0226	0.0220
A → Y↓	0.0277	0.0252	0.0219	0.0208
B → Y↑	0.0282	0.0246	0.0240	0.0223
B → Y↓	0.0278	0.0250	0.0214	0.0198

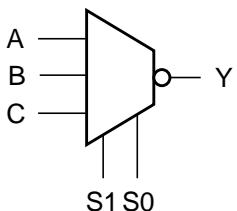
Description	K _{load} (ns/pF)			
	XL	X1	X2	X4
S0 → Y↑	5.4476	3.4900	2.5627	1.3138
S0 → Y↓	4.4921	3.0518	1.5243	0.7510
A → Y↑	5.4455	3.4890	2.5645	1.3144
A → Y↓	4.4918	3.0520	1.5232	0.7507
B → Y↑	5.4492	3.4901	2.5645	1.3140
B → Y↓	4.4951	3.0541	1.5260	0.7517

Cell Description

The MXI3 cell is a 3-to-1 multiplexer with inverted output. The state of the select inputs (S1, S0) determines which data input (A, B, C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (S0 \bullet S1 \bullet \bar{A}) + (\bar{S0} \bullet S1 \bullet \bar{B}) + (\bar{S1} \bullet \bar{C})$$

Logic Symbol



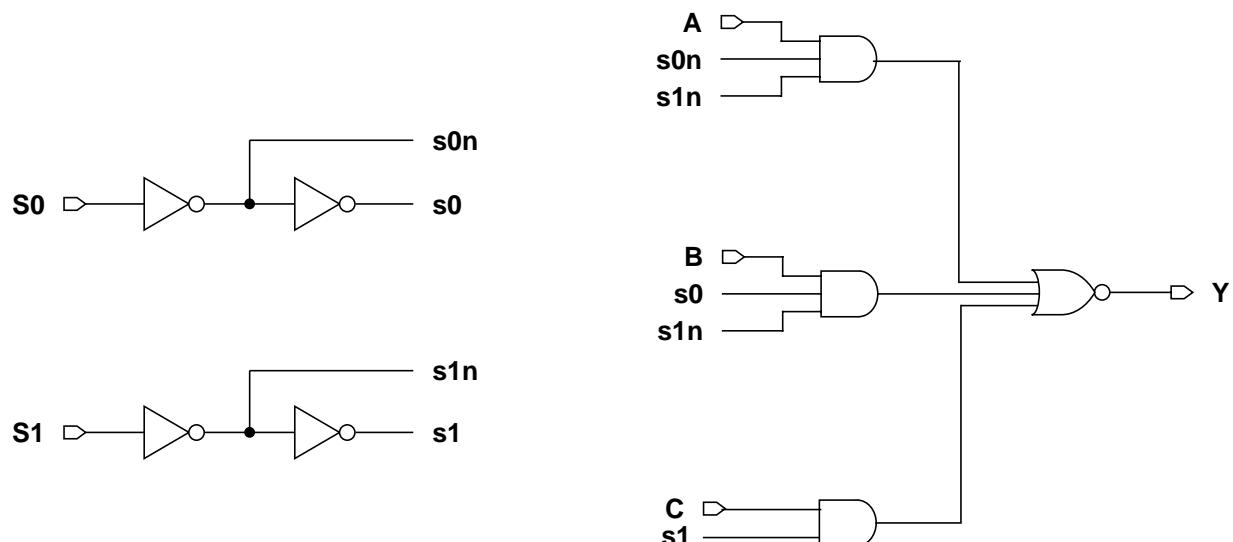
Functions

S1	S0	A	B	C	Y
0	0	0	x	x	1
0	0	1	x	x	0
0	1	x	0	x	1
0	1	x	1	x	0
1	0	x	x	0	1
1	0	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI3XL	2.52	5.32
MXI3X1	2.52	5.32
MXI3X2	2.52	5.60
MXI3X4	2.52	6.44

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
S1	0.0047	0.0058	0.0080	0.0106
S0	0.0070	0.0083	0.0114	0.0159
C	0.0046	0.0058	0.0079	0.0111
B	0.0063	0.0077	0.0106	0.0151
A	0.0063	0.0075	0.0103	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S1	0.0018	0.0019	0.0024	0.0024
S0	0.0024	0.0026	0.0032	0.0035
C	0.0013	0.0012	0.0014	0.0014
B	0.0012	0.0013	0.0017	0.0019
A	0.0013	0.0013	0.0016	0.0020

Delays at 25°C, 1.0V, Typical Process

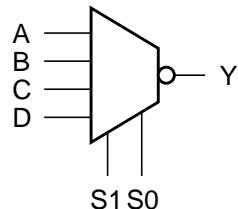
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S1 → Y↑	0.0598	0.0584	0.0621	0.0635	5.7011	3.5885	2.6359	1.3338
S1 → Y↓	0.0634	0.0584	0.0512	0.0576	4.9464	3.1913	1.6050	0.8234
S0 → Y↑	0.1090	0.1028	0.0949	0.1027	5.7213	3.5979	2.6389	1.3358
S0 → Y↓	0.1217	0.1143	0.1059	0.1171	4.9762	3.2008	1.6067	0.8127
C → Y↑	0.0768	0.0736	0.0772	0.0771	5.6985	3.5839	2.6357	1.3313
C → Y↓	0.0877	0.0813	0.0702	0.0798	4.9659	3.1884	1.6044	0.8237
B → Y↑	0.1167	0.1097	0.1011	0.1073	5.7210	3.5981	2.6389	1.3358
B → Y↓	0.1096	0.1012	0.0873	0.0965	4.9745	3.1996	1.6059	0.8127
A → Y↑	0.1205	0.1110	0.1024	0.1030	5.7117	3.5933	2.6362	1.3357
A → Y↓	0.1139	0.1040	0.0935	0.0959	4.9658	3.1951	1.6047	0.8126

Cell Description

The MXI4 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S_1 , S_0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S_0} \cdot \overline{S_1} \cdot A)} + (S_0 \cdot \overline{S_1} \cdot B) + (\overline{S_0} \cdot S_1 \cdot C) + (S_0 \cdot S_1 \cdot D)$$

Logic Symbol



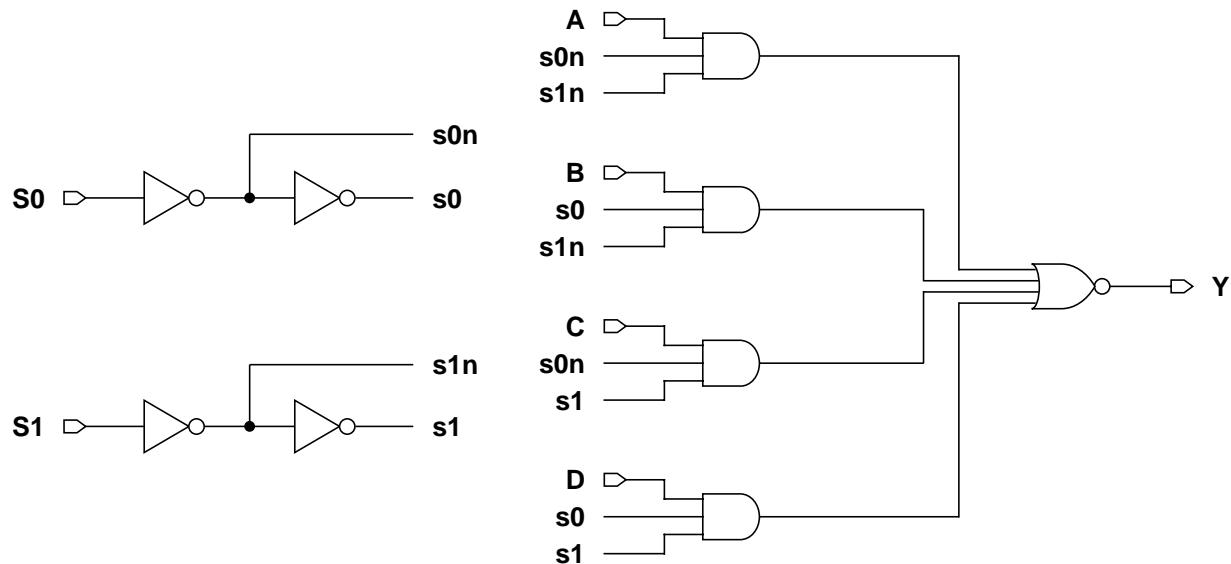
Functions

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	1
0	0	1	x	x	x	0
0	1	x	0	x	x	1
0	1	x	1	x	x	0
1	0	x	x	0	x	1
1	0	x	x	1	x	0
1	1	x	x	x	0	1
1	1	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI4XL	2.52	7.00
MXI4X1	2.52	7.00
MXI4X2	2.52	7.00
MXI4X4	2.52	7.56

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
S0	0.0084	0.0101	0.0135	0.0180
S1	0.0050	0.0063	0.0086	0.0111
A	0.0064	0.0077	0.0105	0.0149
B	0.0068	0.0082	0.0112	0.0154
C	0.0056	0.0069	0.0095	0.0133
D	0.0056	0.0068	0.0095	0.0129

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0040	0.0042	0.0052	0.0059
S1	0.0021	0.0021	0.0023	0.0024
A	0.0012	0.0013	0.0017	0.0020
B	0.0011	0.0012	0.0016	0.0019
C	0.0014	0.0016	0.0019	0.0021
D	0.0011	0.0012	0.0016	0.0018

Delays at 25°C, 1.0V, Typical Process

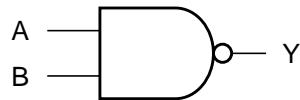
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S0 → Y↑	0.1170	0.1097	0.0981	0.1068	5.5893	3.5609	2.6007	1.3638
S0 → Y↓	0.1385	0.1315	0.1139	0.1145	5.0834	3.2948	1.6458	0.8218
S1 → Y↑	0.0624	0.0618	0.0643	0.0649	5.5552	3.5478	2.5969	1.3617
S1 → Y↓	0.0646	0.0617	0.0534	0.0595	5.0751	3.2856	1.6345	0.8214
A → Y↑	0.1180	0.1096	0.0995	0.1061	5.5871	3.5601	2.6004	1.3637
A → Y↓	0.1164	0.1070	0.0933	0.0971	5.0812	3.2948	1.6457	0.8083
B → Y↑	0.1219	0.1139	0.1009	0.1105	5.5894	3.5608	2.6009	1.3638
B → Y↓	0.1153	0.1061	0.0921	0.0960	5.0818	3.2948	1.6456	0.8083
C → Y↑	0.1133	0.1059	0.0949	0.0924	5.5738	3.5546	2.5977	1.3596
C → Y↓	0.1111	0.1030	0.0900	0.0966	5.0811	3.2890	1.6362	0.8220
D → Y↑	0.1094	0.1023	0.0945	0.0942	5.5722	3.5538	2.5972	1.3597
D → Y↓	0.1092	0.1014	0.0901	0.0990	5.0812	3.2890	1.6362	0.8222

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B)}$$

Logic Symbol



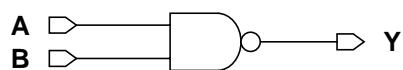
Functions

A	B	Y
0	x	1
x	0	1
1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND2XL	2.52	1.12
NAND2X1	2.52	1.12
NAND2X2	2.52	1.12
NAND2X3	2.52	1.96
NAND2X4	2.52	1.96
NAND2X5	2.52	2.52
NAND2X6	2.52	2.80
NAND2X8	2.52	3.64

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)							
	XL	X1	X2	X3	X4	X5	X6	X8
A	0.0015	0.0020	0.0028	0.0041	0.0052	0.0069	0.0079	0.0104
B	0.0018	0.0024	0.0036	0.0058	0.0071	0.0090	0.0103	0.0138

Pin Capacitance

Pin	Capacitance (pF)							
	XL	X1	X2	X3	X4	X5	X6	X8
A	0.0013	0.0017	0.0024	0.0036	0.0045	0.0061	0.0071	0.0091
B	0.0012	0.0016	0.0024	0.0039	0.0048	0.0059	0.0068	0.0094

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	XL	X1	X2	X3	X4	X5	X6	X8
A → Y↑	0.0147	0.0132	0.0133	0.0136	0.0129	0.0137	0.0132	0.0131
A → Y↓	0.0174	0.0167	0.0125	0.0120	0.0115	0.0122	0.0121	0.0116
B → Y↑	0.0157	0.0145	0.0156	0.0168	0.0158	0.0162	0.0157	0.0158
B → Y↓	0.0178	0.0177	0.0140	0.0146	0.0139	0.0137	0.0136	0.0133

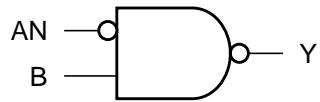
Description	K _{load} (ns/pF)							
	XL	X1	X2	X3	X4	X5	X6	X8
A → Y↑	5.5867	3.5790	2.6455	1.8521	1.3765	1.1045	0.9161	0.7001
A → Y↓	7.1282	5.0022	2.5008	1.6250	1.2225	0.9687	0.8294	0.6020
B → Y↑	5.5513	3.5807	2.6434	1.8023	1.3378	1.1045	0.9155	0.6907
B → Y↓	7.1148	4.9995	2.5010	1.6266	1.2226	0.9690	0.8291	0.6022

Cell Description

The NAND2B cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A}N \bullet B)}$$

Logic Symbol



Functions

AN	B	Y
1	x	1
x	0	1
0	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND2BXL	2.52	1.40
NAND2BX1	2.52	1.40
NAND2BX2	2.52	1.40
NAND2BX4	2.52	2.24
NAND2BX8	2.52	3.92

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)				
	XL	X1	X2	X4	X8
AN	0.0026	0.0030	0.0041	0.0071	0.0135
B	0.0015	0.0020	0.0030	0.0056	0.0111

Pin Capacitance

Pin	Capacitance (pF)				
	XL	X1	X2	X4	X8
AN	0.0011	0.0011	0.0013	0.0019	0.0036
B	0.0013	0.0016	0.0024	0.0048	0.0094

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	XL	X1	X2	X4	X8
AN → Y↑	0.0297	0.0295	0.0287	0.0304	0.0287
AN → Y↓	0.0554	0.0571	0.0479	0.0450	0.0424
B → Y↑	0.0153	0.0139	0.0155	0.0153	0.0155
B → Y↓	0.0178	0.0178	0.0152	0.0150	0.0149

Description	K _{load} (ns/pF)				
	XL	X1	X2	X4	X8
AN → Y↑	5.5762	3.6022	2.6539	1.3862	0.7030
AN → Y↓	7.1999	5.0076	2.4915	1.2253	0.6045
B → Y↑	5.5772	3.6005	2.6639	1.3566	0.6948
B → Y↓	7.1181	4.9752	2.4800	1.2204	0.6028

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C)}$$

Logic Symbol



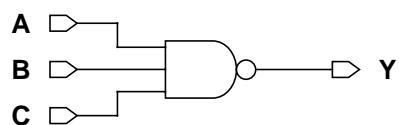
Functions

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3XL	2.52	1.40
NAND3X1	2.52	1.68
NAND3X2	2.52	1.68
NAND3X3	2.52	2.80
NAND3X4	2.52	2.80
NAND3X6	2.52	4.20
NAND3X8	2.52	5.32

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)						
	XL	X1	X2	X3	X4	X6	X8
A	0.0017	0.0023	0.0033	0.0048	0.0058	0.0091	0.0116
B	0.0020	0.0028	0.0041	0.0064	0.0076	0.0116	0.0156
C	0.0023	0.0031	0.0049	0.0080	0.0095	0.0143	0.0193

Pin Capacitance

Pin	Capacitance (pF)						
	XL	X1	X2	X3	X4	X6	X8
A	0.0013	0.0017	0.0025	0.0036	0.0045	0.0073	0.0089
B	0.0013	0.0017	0.0024	0.0040	0.0048	0.0071	0.0095
C	0.0012	0.0016	0.0023	0.0045	0.0051	0.0071	0.0100

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	XL	X1	X2	X3	X4	X6	X8
A → Y↑	0.0167	0.0154	0.0160	0.0159	0.0148	0.0154	0.0161
A → Y↓	0.0257	0.0252	0.0188	0.0169	0.0162	0.0169	0.0159
B → Y↑	0.0186	0.0175	0.0188	0.0195	0.0179	0.0181	0.0180
B → Y↓	0.0284	0.0288	0.0218	0.0217	0.0202	0.0200	0.0197
C → Y↑	0.0200	0.0183	0.0206	0.0221	0.0200	0.0210	0.0207
C → Y↓	0.0304	0.0298	0.0235	0.0244	0.0224	0.0220	0.0219

Description	K _{load} (ns/pF)						
	XL	X1	X2	X3	X4	X6	X8
A → Y↑	5.5856	3.6068	2.6739	1.8838	1.4024	0.9264	0.7893
A → Y↓	9.9373	6.9725	3.4999	2.2762	1.7308	1.1314	0.8421
B → Y↑	5.7103	3.6921	2.7247	1.8675	1.3884	0.9337	0.6987
B → Y↓	9.9307	6.9706	3.4985	2.2766	1.7314	1.1314	0.8426
C → Y↑	5.5953	3.6145	2.6651	1.8186	1.3453	0.9465	0.6938
C → Y↓	9.9366	6.9682	3.4981	2.2773	1.7312	1.1308	0.8428

Cell Description

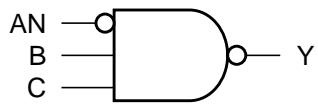
The NAND3B cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C)}$$

Functions

AN	B	C	Y
1	x	x	1
x	0	x	1
x	x	0	1
0	1	1	0

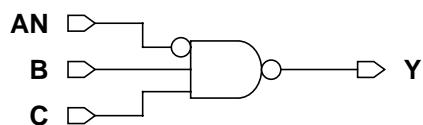
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
NAND3BXL	2.52	1.96
NAND3BX1	2.52	1.96
NAND3BX2	2.52	1.96
NAND3BX4	2.52	3.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
AN	0.0028	0.0034	0.0047	0.0080
B	0.0018	0.0025	0.0034	0.0063
C	0.0021	0.0029	0.0042	0.0080

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0010	0.0011	0.0013	0.0020
B	0.0013	0.0017	0.0024	0.0047
C	0.0012	0.0017	0.0024	0.0052

Delays at 25°C, 1.0V, Typical Process

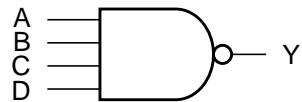
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0319	0.0324	0.0312	0.0323	5.6119	3.6175	2.6700	1.4107
AN → Y↓	0.0639	0.0669	0.0539	0.0464	9.8370	6.8581	3.4599	1.7022
B → Y↑	0.0192	0.0176	0.0186	0.0177	5.7731	3.7143	2.7494	1.3986
B → Y↓	0.0300	0.0298	0.0232	0.0213	9.8106	6.8495	3.4561	1.7018
C → Y↑	0.0205	0.0190	0.0209	0.0202	5.7207	3.6755	2.7407	1.3672
C → Y↓	0.0315	0.0318	0.0248	0.0237	9.8098	6.8492	3.4557	1.7014

Cell Description

The NAND4 cell provides a logical NAND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C \bullet D)}$$

Logic Symbol



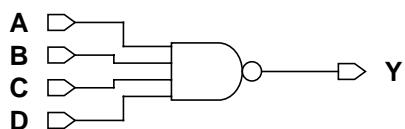
Functions

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4XL	2.52	1.96
NAND4X1	2.52	1.96
NAND4X2	2.52	1.96
NAND4X4	2.52	3.92
NAND4X6	2.52	5.60
NAND4X8	2.52	7.28

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X4	X6	X8
A	0.0022	0.0028	0.0036	0.0069	0.0100	0.0137
B	0.0024	0.0032	0.0045	0.0088	0.0126	0.0168
C	0.0028	0.0037	0.0054	0.0106	0.0154	0.0203
D	0.0031	0.0041	0.0062	0.0125	0.0184	0.0240

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0014	0.0018	0.0024	0.0045	0.0072	0.0100
B	0.0013	0.0017	0.0023	0.0049	0.0072	0.0097
C	0.0013	0.0017	0.0023	0.0049	0.0075	0.0097
D	0.0012	0.0017	0.0023	0.0053	0.0081	0.0100

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0201	0.0177	0.0171	0.0171	0.0183	0.0186
A → Y↓	0.0387	0.0365	0.0237	0.0220	0.0214	0.0232
B → Y↑	0.0222	0.0198	0.0203	0.0206	0.0214	0.0214
B → Y↓	0.0428	0.0411	0.0290	0.0281	0.0264	0.0277
C → Y↑	0.0238	0.0214	0.0229	0.0230	0.0243	0.0242
C → Y↓	0.0459	0.0444	0.0325	0.0316	0.0301	0.0313
D → Y↑	0.0245	0.0219	0.0242	0.0249	0.0277	0.0270
D → Y↓	0.0478	0.0461	0.0344	0.0343	0.0332	0.0340

Delays at 25°C, 1.0V, Typical Process

Description	K_{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	5.6188	3.6184	2.6694	1.4119	1.0529	0.7814
A → Y↓	12.7199	8.9530	4.4752	2.1910	1.4539	1.1478
B → Y↑	5.7767	3.7265	2.7487	1.4077	1.0469	0.7845
B → Y↓	12.7075	8.9478	4.4743	2.1913	1.4542	1.1478
C → Y↑	5.7903	3.7355	2.7545	1.3973	1.0358	0.7819
C → Y↓	12.7063	8.9454	4.4741	2.1921	1.4544	1.1475
D → Y↑	5.6539	3.6429	2.6855	1.3634	1.0429	0.7813
D → Y↓	12.7129	8.9438	4.4752	2.1931	1.4546	1.1480

Cell Description

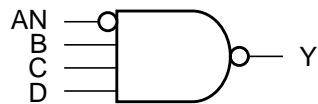
The NAND4B cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C \bullet D)}$$

Functions

AN	B	C	D	Y
1	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
0	1	1	1	0

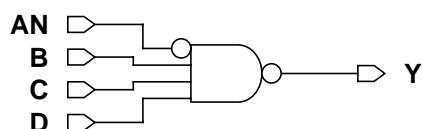
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
NAND4BXL	2.52	2.24
NAND4BX1	2.52	2.24
NAND4BX2	2.52	2.24
NAND4BX4	2.52	3.92

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
AN	0.0031	0.0037	0.0050	0.0087
B	0.0021	0.0026	0.0037	0.0073
C	0.0023	0.0030	0.0045	0.0090
D	0.0027	0.0035	0.0054	0.0110

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0011	0.0011	0.0014	0.0020
B	0.0013	0.0017	0.0023	0.0047
C	0.0013	0.0016	0.0023	0.0049
D	0.0013	0.0017	0.0023	0.0054

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0348	0.0349	0.0329	0.0347	5.6731	3.6556	2.6769	1.4165
AN → Y↓	0.0755	0.0782	0.0599	0.0527	12.6041	8.8678	4.4522	2.2060
B → Y↑	0.0214	0.0187	0.0199	0.0200	5.8138	3.7467	2.7604	1.4135
B → Y↓	0.0418	0.0396	0.0299	0.0292	12.5835	8.8613	4.4491	2.2072
C → Y↑	0.0232	0.0204	0.0226	0.0227	5.8408	3.7562	2.7687	1.4051
C → Y↓	0.0453	0.0434	0.0337	0.0330	12.5768	8.8539	4.4515	2.2061
D → Y↑	0.0242	0.0210	0.0243	0.0251	5.7775	3.6733	2.7236	1.3824
D → Y↓	0.0471	0.0447	0.0354	0.0360	12.5794	8.8596	4.4511	2.2080

Cell Description

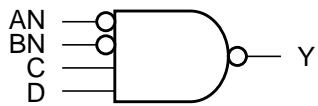
The NAND4BB cell provides a logical NAND of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet \overline{BN} \bullet C \bullet D)}$$

Functions

AN	BN	C	D	Y
1	x	x	x	1
x	1	x	x	1
x	x	0	x	1
x	x	x	0	1
0	0	1	1	0

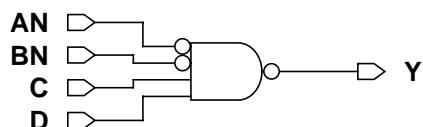
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
NAND4BBXL	2.52	2.80
NAND4BBX1	2.52	2.80
NAND4BBX2	2.52	2.80
NAND4BBX4	2.52	4.48

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
AN	0.0032	0.0039	0.0053	0.0092
BN	0.0033	0.0040	0.0056	0.0102
C	0.0020	0.0026	0.0039	0.0076
D	0.0023	0.0030	0.0047	0.0094

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0010	0.0010	0.0013	0.0019
BN	0.0010	0.0010	0.0014	0.0019
C	0.0012	0.0016	0.0023	0.0049
D	0.0012	0.0016	0.0024	0.0054

Delays at 25°C, 1.0V, Typical Process

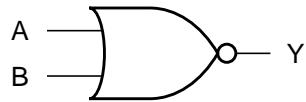
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0357	0.0356	0.0343	0.0349	5.6387	3.6409	2.6748	1.4137
AN → Y↓	0.0758	0.0783	0.0618	0.0562	12.7480	8.9399	4.4758	2.2181
BN → Y↑	0.0357	0.0353	0.0353	0.0378	5.7820	3.7350	2.7551	1.4096
BN → Y↓	0.0753	0.0776	0.0635	0.0617	12.7564	8.9527	4.4810	2.2219
C → Y↑	0.0223	0.0199	0.0225	0.0221	5.7976	3.7392	2.7643	1.3978
C → Y↓	0.0450	0.0440	0.0351	0.0342	12.7318	8.9356	4.4739	2.2189
D → Y↑	0.0227	0.0205	0.0240	0.0243	5.6306	3.6175	2.6842	1.3572
D → Y↓	0.0465	0.0462	0.0372	0.0376	12.7308	8.9319	4.4768	2.2194

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B)}$$

Logic Symbol



Functions

A	B	Y
0	0	1
x	1	0
1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2XL	2.52	1.12
NOR2X1	2.52	1.12
NOR2X2	2.52	1.12
NOR2X3	2.52	1.96
NOR2X4	2.52	1.96
NOR2X5	2.52	2.52
NOR2X6	2.52	2.52
NOR2X8	2.52	3.36

Functional Schematic



AC Power

Pin	Power (μ W/MHz)							
	XL	X1	X2	X3	X4	X5	X6	X8
A	0.0015	0.0020	0.0029	0.0045	0.0057	0.0071	0.0083	0.0110
B	0.0018	0.0025	0.0036	0.0056	0.0072	0.0088	0.0103	0.0139

Pin Capacitance

Pin	Capacitance (pF)							
	XL	X1	X2	X3	X4	X5	X6	X8
A	0.0013	0.0017	0.0024	0.0036	0.0046	0.0059	0.0069	0.0090
B	0.0012	0.0016	0.0023	0.0038	0.0048	0.0055	0.0065	0.0090

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	XL	X1	X2	X3	X4	X5	X6	X8
A → Y↑	0.0212	0.0192	0.0198	0.0201	0.0192	0.0208	0.0201	0.0196
A → Y↓	0.0117	0.0115	0.0093	0.0091	0.0088	0.0091	0.0088	0.0086
B → Y↑	0.0250	0.0230	0.0239	0.0254	0.0241	0.0257	0.0246	0.0247
B → Y↓	0.0132	0.0133	0.0106	0.0107	0.0104	0.0109	0.0100	0.0104

Description	K_{load} (ns/pF)							
	XL	X1	X2	X3	X4	X5	X6	X8
A → Y↑	10.8654	7.0192	5.1382	3.5992	2.6596	2.2904	1.8984	1.4180
A → Y↓	4.1897	2.9214	1.4593	0.9625	0.7151	0.5899	0.4780	0.3565
B → Y↑	10.8355	7.0051	5.1326	3.5979	2.6583	2.2876	1.8969	1.4171
B → Y↓	4.2138	2.9367	1.4675	0.9817	0.7288	0.5924	0.4798	0.3808

Cell Description

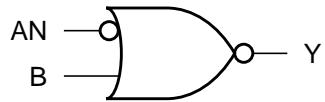
The NOR2B cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A}N + B)}$$

Functions

AN	B	Y
1	0	1
x	1	0
0	x	0

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
NOR2BXL	2.52	1.40
NOR2BX1	2.52	1.40
NOR2BX2	2.52	1.68
NOR2BX4	2.52	2.24
NOR2BX8	2.52	4.20

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)				
	XL	X1	X2	X4	X8
AN	0.0024	0.0029	0.0039	0.0065	0.0065
B	0.0019	0.0025	0.0037	0.0071	0.0071

Pin Capacitance

Pin	Capacitance (pF)				
	XL	X1	X2	X4	X8
AN	0.0010	0.0011	0.0013	0.0020	0.0020
B	0.0013	0.0017	0.0023	0.0047	0.0047

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	XL	X1	X2	X4	X8
AN → Y↑	0.0350	0.0342	0.0350	0.0347	0.0343
AN → Y↓	0.0477	0.0510	0.0445	0.0385	0.0383
B → Y↑	0.0263	0.0238	0.0255	0.0251	0.0256
B → Y↓	0.0131	0.0129	0.0105	0.0101	0.0099

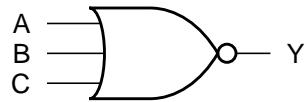
Description	K_{load} (ns/pF)				
	XL	X1	X2	X4	X8
AN → Y↑	10.9867	7.0812	5.2220	2.6795	1.3790
AN → Y↓	4.4150	3.0315	1.4983	0.7335	0.3643
B → Y↑	10.9700	7.0735	5.2183	2.6789	1.3784
B → Y↓	4.1484	2.9093	1.4520	0.7249	0.3575

Cell Description

The NOR3 cell provides a logical NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C)}$$

Logic Symbol



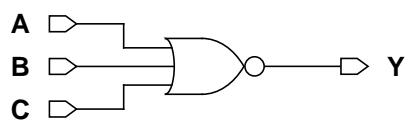
Functions

A	B	C	Y
0	0	0	1
x	x	1	0
x	1	x	0
1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR3XL	2.52	1.40
NOR3X1	2.52	1.40
NOR3X2	2.52	1.68
NOR3X4	2.52	2.52
NOR3X6	2.52	3.92
NOR3X8	2.52	5.32

Functional Schematic



AC Power

Pin	Power (μ W/MHz)					
	XL	X1	X2	X4	X6	X8
A	0.0019	0.0024	0.0037	0.0069	0.0104	0.0143
B	0.0023	0.0030	0.0045	0.0085	0.0126	0.0173
C	0.0027	0.0036	0.0052	0.0100	0.0147	0.0203

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0013	0.0017	0.0024	0.0044	0.0072	0.0094
B	0.0013	0.0017	0.0024	0.0047	0.0069	0.0094
C	0.0012	0.0016	0.0023	0.0047	0.0068	0.0099

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0342	0.0281	0.0316	0.0280	0.0315	0.0308
A → Y↓	0.0134	0.0125	0.0104	0.0094	0.0097	0.0096
B → Y↑	0.0450	0.0388	0.0419	0.0405	0.0421	0.0424
B → Y↓	0.0152	0.0145	0.0117	0.0111	0.0109	0.0110
C → Y↑	0.0493	0.0435	0.0456	0.0453	0.0468	0.0481
C → Y↓	0.0160	0.0158	0.0122	0.0128	0.0120	0.0117

Description	K _{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	16.6175	10.7370	7.8406	4.0635	2.8755	2.1319
A → Y↓	4.1941	2.9169	1.4550	0.7115	0.4756	0.3532
B → Y↑	16.5816	10.7235	7.8321	4.0616	2.8713	2.1300
B → Y↓	4.1382	2.8819	1.4424	0.7184	0.4759	0.3553
C → Y↑	16.5880	10.7217	7.8303	4.0604	2.8713	2.1309
C → Y↓	4.2533	2.9588	1.4774	0.8283	0.5199	0.3616

Cell Description

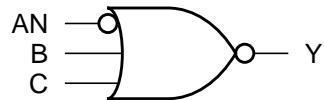
The NOR3B cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C)}$$

Functions

AN	B	C	Y
1	0	0	1
x	x	1	0
x	1	x	0
0	x	x	0

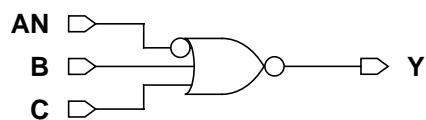
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
NOR3BXL	2.52	1.68
NOR3BX1	2.52	1.68
NOR3BX2	2.52	1.96
NOR3BX4	2.52	3.08

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
AN	0.0028	0.0032	0.0041	0.0071
B	0.0024	0.0029	0.0045	0.0086
C	0.0028	0.0035	0.0052	0.0101

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0011	0.0011	0.0013	0.0020
B	0.0012	0.0016	0.0023	0.0045
C	0.0012	0.0016	0.0023	0.0048

Delays at 25°C, 1.0V, Typical Process

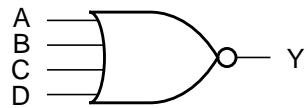
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0523	0.0450	0.0465	0.0468	16.7679	10.7573	7.9631	4.2226
AN → Y↓	0.0527	0.0565	0.0462	0.0405	4.3527	3.0272	1.5007	0.7288
B → Y↑	0.0468	0.0384	0.0434	0.0424	16.7240	10.7377	7.9573	4.2189
B → Y↓	0.0152	0.0140	0.0116	0.0108	4.1250	2.8817	1.4412	0.7143
C → Y↑	0.0514	0.0429	0.0480	0.0480	16.7356	10.7368	7.9583	4.2201
C → Y↓	0.0160	0.0151	0.0123	0.0117	4.1957	2.9407	1.4714	0.7308

Cell Description

The NOR4 cell provides a logical NOR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C + D)}$$

Logic Symbol



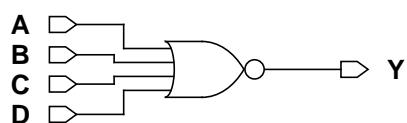
Functions

A	B	C	D	Y
0	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR4XL	2.52	1.68
NOR4X1	2.52	1.68
NOR4X2	2.52	1.68
NOR4X4	2.52	3.08
NOR4X6	2.52	4.48
NOR4X8	2.52	8.12

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X4	X6	X8
A	0.0023	0.0028	0.0031	0.0061	0.0086	0.0143
B	0.0027	0.0034	0.0039	0.0077	0.0107	0.0174
C	0.0031	0.0039	0.0046	0.0091	0.0128	0.0206
D	0.0035	0.0045	0.0053	0.0106	0.0150	0.0235

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0014	0.0018	0.0020	0.0037	0.0057	0.0092
B	0.0013	0.0016	0.0019	0.0039	0.0054	0.0092
C	0.0013	0.0016	0.0019	0.0039	0.0056	0.0094
D	0.0013	0.0016	0.0019	0.0042	0.0057	0.0091

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0430	0.0378	0.0303	0.0288	0.0301	0.0348
A → Y↓	0.0148	0.0135	0.0151	0.0143	0.0142	0.0135
B → Y↑	0.0611	0.0552	0.0477	0.0470	0.0479	0.0534
B → Y↓	0.0169	0.0156	0.0186	0.0184	0.0175	0.0166
C → Y↑	0.0713	0.0655	0.0576	0.0569	0.0594	0.0652
C → Y↓	0.0179	0.0166	0.0207	0.0206	0.0201	0.0185
D → Y↑	0.0752	0.0695	0.0618	0.0623	0.0654	0.0699
D → Y↓	0.0180	0.0169	0.0221	0.0225	0.0217	0.0190

Delays at 25°C, 1.0V, Typical Process

Description	K _{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	20.5306	14.5386	10.6573	5.4577	4.0072	2.7724
A → Y↓	4.1956	2.9249	3.0274	1.5121	1.0304	0.5997
B → Y↑	20.4783	14.5190	10.6500	5.4550	4.0036	2.7704
B → Y↓	4.1194	2.8686	2.9632	1.5179	1.0306	0.6018
C → Y↑	20.4706	14.5118	10.6482	5.4541	4.0040	2.7705
C → Y↓	4.1971	2.9108	2.9857	1.5377	1.0447	0.6085
D → Y↑	20.4568	14.5094	10.6473	5.4546	4.0053	2.7702
D → Y↓	4.3980	3.0291	3.0883	1.5919	1.0766	0.6230

Cell Description

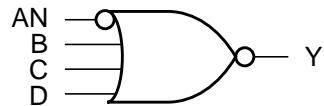
The NOR4B cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C + D)}$$

Functions

AN	B	C	D	Y
1	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
0	x	x	x	0

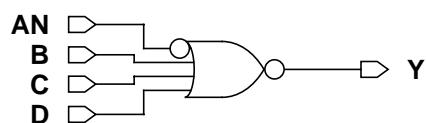
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
NOR4BXL	2.52	2.24
NOR4BX1	2.52	2.24
NOR4BX2	2.52	2.24
NOR4BX4	2.52	3.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
AN	0.0027	0.0031	0.0036	0.0060
B	0.0027	0.0034	0.0039	0.0075
C	0.0030	0.0039	0.0046	0.0088
D	0.0034	0.0045	0.0054	0.0103

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0011	0.0011	0.0013	0.0015
B	0.0013	0.0017	0.0019	0.0038
C	0.0013	0.0016	0.0019	0.0038
D	0.0013	0.0016	0.0018	0.0041

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0567	0.0539	0.0445	0.0498	20.6646	14.6232	10.7089	5.7342
AN → Y↓	0.0552	0.0486	0.0528	0.0489	4.3690	2.9759	3.0348	1.5234
B → Y↑	0.0597	0.0555	0.0480	0.0488	20.6279	14.6078	10.7019	5.7302
B → Y↓	0.0163	0.0153	0.0182	0.0175	4.1096	2.8635	2.9516	1.5180
C → Y↑	0.0706	0.0657	0.0580	0.0585	20.6103	14.6028	10.6995	5.7293
C → Y↓	0.0173	0.0163	0.0205	0.0197	4.1707	2.8938	2.9635	1.5331
D → Y↑	0.0748	0.0706	0.0623	0.0642	20.6114	14.6015	10.7002	5.7308
D → Y↓	0.0172	0.0166	0.0214	0.0214	4.2738	2.9651	3.0014	1.5753

Cell Description

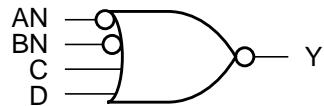
The NOR4BB cell provides a logical NOR of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + \overline{BN}) + C + D}$$

Functions

AN	BN	C	D	Y
1	1	0	0	1
x	x	x	1	0
x	x	1	x	0
x	0	x	x	0
0	x	x	x	0

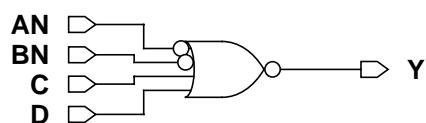
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
NOR4BBXL	2.52	2.80
NOR4BBX1	2.52	2.80
NOR4BBX2	2.52	2.80
NOR4BBX4	2.52	3.92

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
AN	0.0030	0.0035	0.0040	0.0062
BN	0.0029	0.0034	0.0040	0.0078
C	0.0030	0.0040	0.0046	0.0090
D	0.0034	0.0045	0.0053	0.0105

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0011	0.0011	0.0013	0.0016
BN	0.0011	0.0011	0.0013	0.0016
C	0.0013	0.0016	0.0019	0.0038
D	0.0013	0.0016	0.0019	0.0041

Delays at 25°C, 1.0V, Typical Process

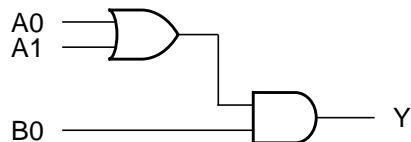
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0566	0.0568	0.0457	0.0489	20.3361	14.5851	10.6461	5.7841
AN → Y↓	0.0583	0.0530	0.0561	0.0493	4.3923	2.9822	3.0238	1.5198
BN → Y↑	0.0716	0.0718	0.0612	0.0706	20.2702	14.5551	10.6380	5.7818
BN → Y↓	0.0562	0.0513	0.0558	0.0551	4.2653	2.9210	2.9755	1.5233
C → Y↑	0.0683	0.0665	0.0581	0.0606	20.2720	14.5528	10.6374	5.7806
C → Y↓	0.0170	0.0164	0.0205	0.0196	4.1981	2.9089	2.9841	1.5281
D → Y↑	0.0722	0.0711	0.0626	0.0668	20.2610	14.5517	10.6378	5.7813
D → Y↓	0.0172	0.0170	0.0221	0.0211	4.3819	3.0264	3.0851	1.5507

Cell Description

The OA21 cell provides the logical AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (A_0 + A_1) \bullet B_0$$

Logic Symbol



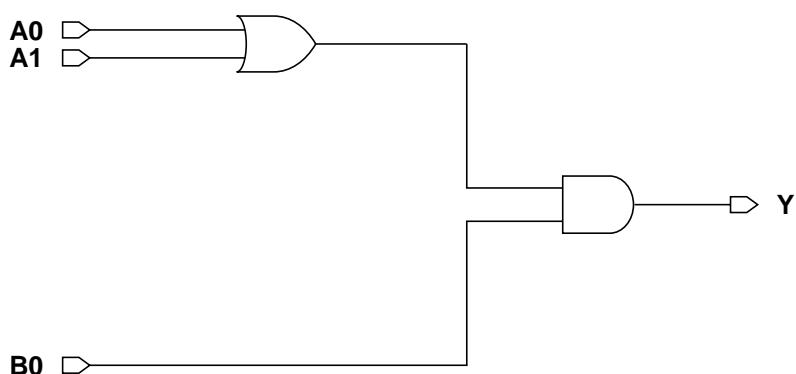
Functions

A0	A1	B0	Y
x	x	0	0
0	0	x	0
x	1	1	1
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA21XL	2.52	1.96
OA21X1	2.52	1.96
OA21X2	2.52	2.24
OA21X4	2.52	2.52

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0035	0.0043	0.0056	0.0099
A1	0.0037	0.0045	0.0059	0.0105
B0	0.0026	0.0032	0.0043	0.0077

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0010	0.0011	0.0014	0.0022
A1	0.0009	0.0010	0.0012	0.0020
B0	0.0011	0.0011	0.0013	0.0022

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0417	0.0454	0.0399	0.0387	5.6506	3.5964	2.6266	1.3616
A0 → Y↓	0.1030	0.1142	0.0933	0.0825	5.1094	3.4474	1.6894	0.8215
A1 → Y↑	0.0445	0.0482	0.0427	0.0419	5.6715	3.6081	2.6315	1.3642
A1 → Y↓	0.1074	0.1178	0.0974	0.0870	5.1102	3.4471	1.6894	0.8217
B0 → Y↑	0.0398	0.0438	0.0390	0.0385	5.6717	3.6073	2.6313	1.3642
B0 → Y↓	0.0525	0.0591	0.0490	0.0447	4.6504	3.1919	1.5820	0.7746

Cell Description

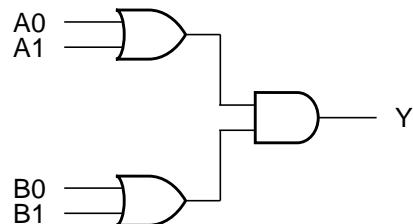
The OA22 cell provides the logical AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = (A_0 + A_1) \bullet (B_0 + B_1)$$

Functions

A0	A1	B0	B1	Y
x	x	0	0	0
0	0	x	x	0
x	1	x	1	1
x	1	1	x	1
1	x	x	1	1
1	x	1	x	1

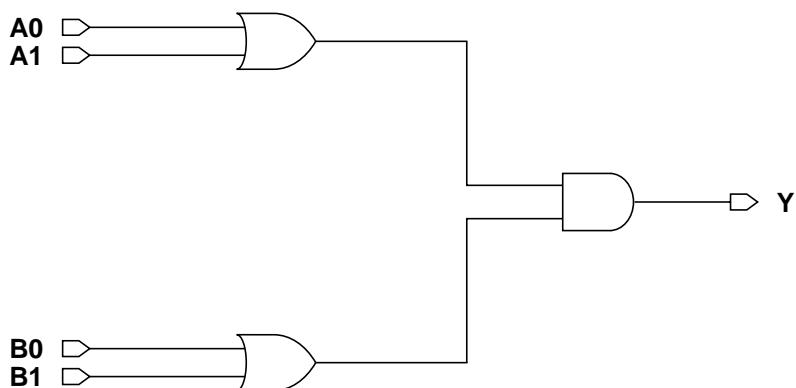
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OA22XL	2.52	2.52
OA22X1	2.52	2.52
OA22X2	2.52	2.52
OA22X4	2.52	3.08

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0034	0.0041	0.0056	0.0097
A1	0.0035	0.0043	0.0060	0.0104
B0	0.0046	0.0053	0.0073	0.0125
B1	0.0048	0.0056	0.0077	0.0132

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0010	0.0011	0.0014	0.0024
A1	0.0010	0.0011	0.0015	0.0023
B0	0.0010	0.0011	0.0015	0.0023
B1	0.0011	0.0012	0.0015	0.0023

Delays at 25°C, 1.0V, Typical Process

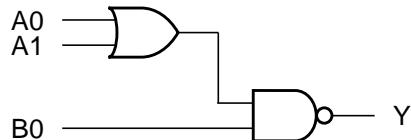
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0441	0.0488	0.0447	0.0439	5.7166	3.6840	2.6598	1.3787
A0 → Y↓	0.0957	0.0928	0.0791	0.0709	5.3098	3.4480	1.7104	0.8316
A1 → Y↑	0.0463	0.0517	0.0480	0.0471	5.7320	3.6942	2.6638	1.3811
A1 → Y↓	0.0999	0.0971	0.0842	0.0753	5.3099	3.4478	1.7102	0.8317
B0 → Y↑	0.0515	0.0562	0.0517	0.0495	5.7176	3.6850	2.6600	1.3791
B0 → Y↓	0.1282	0.1187	0.1027	0.0897	5.5076	3.5419	1.7552	0.8523
B1 → Y↑	0.0544	0.0599	0.0546	0.0528	5.7326	3.6946	2.6640	1.3812
B1 → Y↓	0.1354	0.1255	0.1079	0.0949	5.5100	3.5417	1.7553	0.8523

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet B_0}$$

Logic Symbol



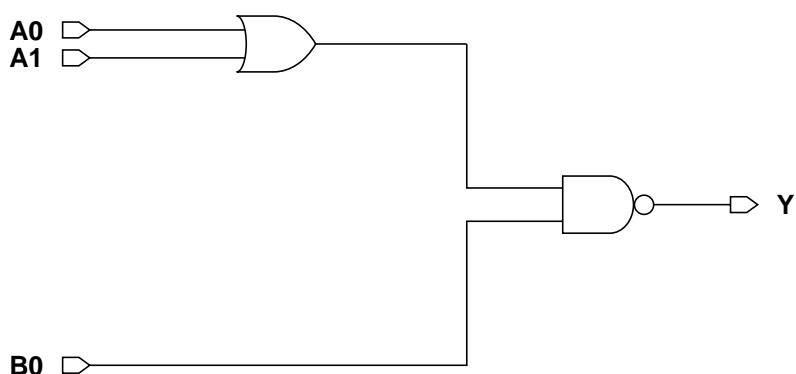
Functions

A0	A1	B0	Y
0	0	x	1
x	x	0	1
x	1	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21XL	2.52	1.40
OAI21X1	2.52	1.40
OAI21X2	2.52	1.68
OAI21X3	2.52	2.52
OAI21X4	2.52	2.52
OAI21X6	2.52	3.64
OAI21X8	2.52	4.76

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)						
	XL	X1	X2	X3	X4	X6	X8
A0	0.0022	0.0028	0.0044	0.0068	0.0081	0.0124	0.0162
A1	0.0025	0.0034	0.0052	0.0080	0.0096	0.0146	0.0193
B0	0.0019	0.0025	0.0035	0.0052	0.0064	0.0098	0.0127

Pin Capacitance

Pin	Capacitance (pF)						
	XL	X1	X2	X3	X4	X6	X8
A0	0.0013	0.0017	0.0024	0.0036	0.0043	0.0070	0.0091
A1	0.0012	0.0016	0.0022	0.0038	0.0045	0.0068	0.0091
B0	0.0013	0.0017	0.0024	0.0036	0.0045	0.0063	0.0084

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	XL	X1	X2	X3	X4	X6	X8
A0 → Y↑	0.0311	0.0268	0.0312	0.0322	0.0320	0.0305	0.0298
A0 → Y↓	0.0210	0.0199	0.0163	0.0162	0.0152	0.0158	0.0152
A1 → Y↑	0.0353	0.0311	0.0354	0.0375	0.0372	0.0353	0.0346
A1 → Y↓	0.0248	0.0242	0.0191	0.0191	0.0178	0.0184	0.0178
B0 → Y↑	0.0148	0.0133	0.0139	0.0140	0.0132	0.0141	0.0135
B0 → Y↓	0.0212	0.0208	0.0157	0.0153	0.0144	0.0153	0.0147

Description	K _{load} (ns/pF)						
	XL	X1	X2	X3	X4	X6	X8
A0 → Y↑	11.1279	7.1550	5.2647	3.6269	2.9502	1.8372	1.3865
A0 → Y↓	7.0183	4.9040	2.4525	1.6261	1.2340	0.8544	0.6315
A1 → Y↑	11.1097	7.1496	5.2630	3.6253	2.9490	1.8366	1.3856
A1 → Y↓	7.1188	4.9812	2.5055	1.6259	1.2287	0.8508	0.6299
B0 → Y↑	5.6386	3.6286	2.6764	1.8313	1.3723	0.9767	0.7278
B0 → Y↓	7.1417	4.9917	2.5074	1.6278	1.2295	0.8517	0.6304

Cell Description

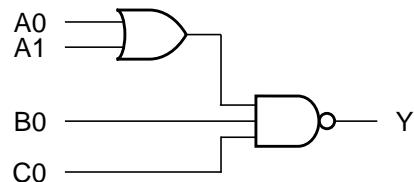
The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1)} \bullet B_0 \bullet C_0$$

Functions

A0	A1	B0	C0	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
x	1	1	1	0
1	x	1	1	0

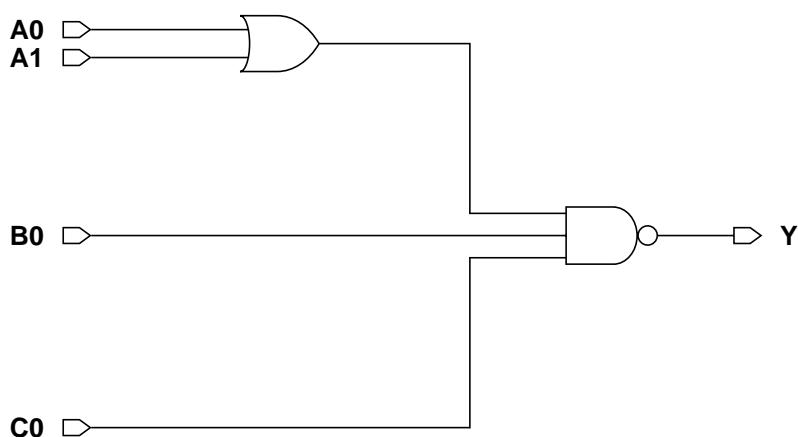
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI211XL	2.52	1.68
OAI211X1	2.52	1.96
OAI211X2	2.52	1.96
OAI211X4	2.52	3.36

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0030	0.0040	0.0059	0.0109
A1	0.0033	0.0045	0.0066	0.0124
B0	0.0022	0.0031	0.0040	0.0076
C0	0.0025	0.0035	0.0049	0.0093

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0025	0.0046
A1	0.0012	0.0016	0.0023	0.0043
B0	0.0013	0.0017	0.0025	0.0045
C0	0.0014	0.0017	0.0024	0.0046

Delays at 25°C, 1.0V, Typical Process

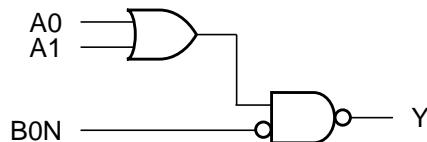
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0424	0.0380	0.0415	0.0418	11.1205	7.2532	5.3118	2.8531
A0 → Y↓	0.0369	0.0350	0.0261	0.0253	10.0215	6.8754	3.4495	1.7959
A1 → Y↑	0.0462	0.0419	0.0455	0.0461	11.1109	7.2492	5.3083	2.8514
A1 → Y↓	0.0426	0.0411	0.0301	0.0294	10.1284	6.9616	3.4959	1.8115
B0 → Y↑	0.0177	0.0166	0.0165	0.0161	5.6444	3.6425	2.6863	1.4029
B0 → Y↓	0.0340	0.0341	0.0235	0.0227	10.1509	6.9733	3.4989	1.8134
C0 → Y↑	0.0206	0.0189	0.0194	0.0189	5.7999	3.7720	2.7621	1.3790
C0 → Y↓	0.0383	0.0375	0.0266	0.0268	10.1517	6.9701	3.4994	1.8137

Cell Description

The OAI21B cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet \overline{B_{0N}}}$$

Logic Symbol



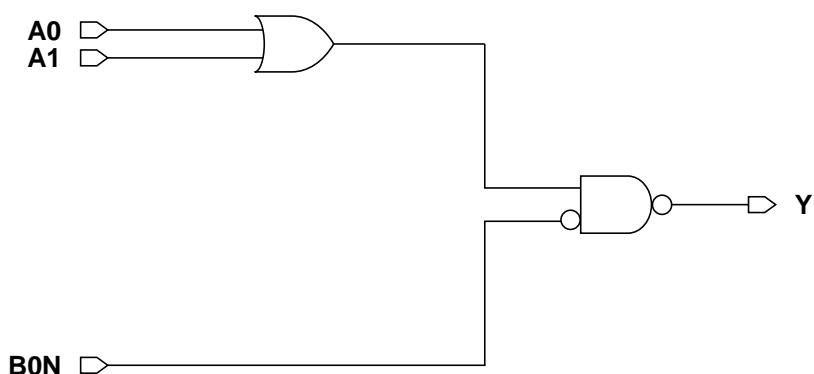
Functions

A0	A1	B0N	Y
0	0	x	1
x	x	1	1
x	1	0	0
1	x	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21BXL	2.52	1.96
OAI21BX1	2.52	1.96
OAI21BX2	2.52	2.24
OAI21BX4	2.52	3.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0021	0.0026	0.0036	0.0066
A1	0.0024	0.0031	0.0043	0.0082
B0N	0.0027	0.0033	0.0044	0.0079

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0044
A1	0.0011	0.0015	0.0023	0.0046
B0N	0.0010	0.0011	0.0013	0.0020

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0356	0.0295	0.0313	0.0298	11.2458	7.2209	5.3131	2.7243
A0 → Y↓	0.0254	0.0240	0.0184	0.0176	7.1510	4.9925	2.4657	1.2386
A1 → Y↑	0.0392	0.0333	0.0354	0.0348	11.2186	7.2082	5.3077	2.7232
A1 → Y↓	0.0296	0.0286	0.0214	0.0204	7.2748	5.0881	2.5093	1.2308
B0N → Y↑	0.0313	0.0317	0.0294	0.0305	5.8221	3.7425	2.7672	1.4110
B0N → Y↓	0.0602	0.0644	0.0504	0.0444	7.3159	5.1068	2.5155	1.2329

Cell Description

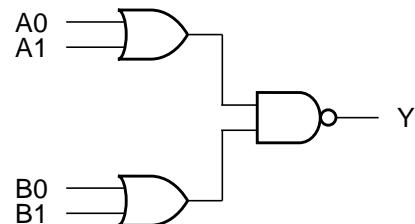
The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet (B_0 + B_1)}$$

Functions

A0	A1	B0	B1	Y
0	0	x	x	1
x	x	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	x	1	0
1	x	1	x	0

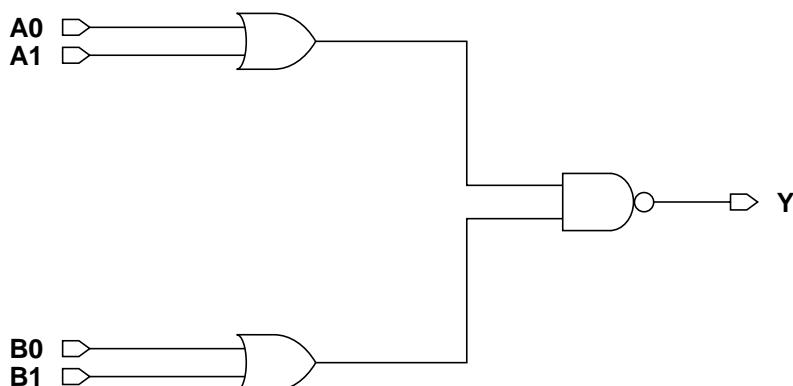
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI22XL	2.52	1.68
OAI22X1	2.52	1.68
OAI22X2	2.52	1.96
OAI22X4	2.52	3.36

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0023	0.0030	0.0041	0.0080
A1	0.0027	0.0036	0.0048	0.0094
B0	0.0034	0.0043	0.0062	0.0119
B1	0.0037	0.0049	0.0069	0.0134

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0014	0.0018	0.0024	0.0045
A1	0.0013	0.0016	0.0022	0.0045
B0	0.0013	0.0017	0.0024	0.0045
B1	0.0013	0.0016	0.0024	0.0046

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0292	0.0248	0.0255	0.0260	11.3005	7.2608	5.3486	2.8825
A0 → Y↓	0.0238	0.0228	0.0166	0.0162	7.0384	4.9285	2.4683	1.2292
A1 → Y↑	0.0335	0.0293	0.0296	0.0317	11.2814	7.2536	5.3442	2.8809
A1 → Y↓	0.0282	0.0277	0.0194	0.0203	7.1992	5.0406	2.4948	1.2978
B0 → Y↑	0.0436	0.0363	0.0402	0.0387	11.3524	7.2975	5.4093	2.7346
B0 → Y↓	0.0317	0.0297	0.0220	0.0218	7.1010	4.9664	2.4715	1.3005
B1 → Y↑	0.0484	0.0411	0.0448	0.0438	11.3401	7.2925	5.4058	2.7336
B1 → Y↓	0.0363	0.0347	0.0250	0.0249	7.2022	5.0393	2.4942	1.2985

Cell Description

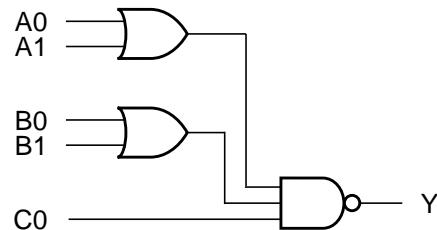
The OAI221 cell provides the logical inverted AND of two OR groups and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet (B_0 + B_1) \bullet C_0}$$

Functions

A0	A1	B0	B1	C0	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
x	1	x	1	1	0
x	1	1	x	1	0
1	x	x	1	1	0
1	x	1	x	1	0

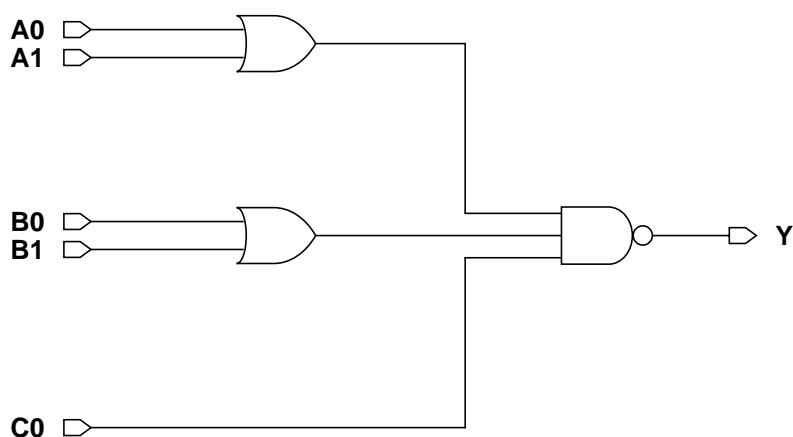
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI221XL	2.52	2.52
OAI221X1	2.52	2.52
OAI221X2	2.52	2.52
OAI221X4	2.52	4.48

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0032	0.0042	0.0058	0.0110
A1	0.0036	0.0048	0.0066	0.0124
B0	0.0041	0.0053	0.0075	0.0147
B1	0.0044	0.0058	0.0083	0.0161
C0	0.0026	0.0036	0.0047	0.0092

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0012	0.0017	0.0024	0.0050
A1	0.0013	0.0016	0.0023	0.0043
B0	0.0012	0.0017	0.0024	0.0046
B1	0.0012	0.0016	0.0022	0.0043
C0	0.0013	0.0017	0.0022	0.0044

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0460	0.0398	0.0410	0.0395	11.7319	7.5327	5.4910	2.8117
A0 → Y↓	0.0465	0.0450	0.0319	0.0307	10.0907	7.0776	3.5801	1.8252
A1 → Y↑	0.0513	0.0447	0.0456	0.0433	11.7271	7.5301	5.4891	2.8098
A1 → Y↓	0.0525	0.0512	0.0356	0.0345	10.0077	7.0070	3.5281	1.8325
B0 → Y↑	0.0546	0.0470	0.0501	0.0519	11.4823	7.3515	5.3741	2.8880
B0 → Y↓	0.0523	0.0501	0.0355	0.0352	9.9978	7.0011	3.5235	1.8310
B1 → Y↑	0.0583	0.0510	0.0542	0.0561	11.4760	7.3486	5.3724	2.8872
B1 → Y↓	0.0577	0.0561	0.0396	0.0393	10.0080	7.0102	3.5293	1.8329
C0 → Y↑	0.0195	0.0180	0.0202	0.0170	5.7096	3.6797	3.2381	1.3838
C0 → Y↓	0.0414	0.0425	0.0287	0.0287	10.0250	7.0180	3.5318	1.8345

Cell Description

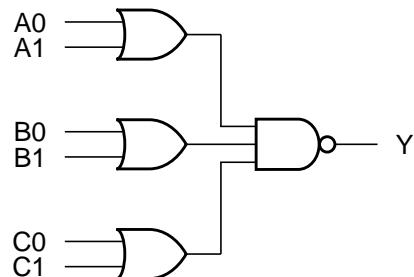
The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet (B_0 + B_1) \bullet (C_0 + C_1)}$$

Functions

A0	A1	B0	B1	C0	C1	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
x	1	x	1	1	x	0
x	1	x	1	x	1	0
x	1	1	x	1	x	0
x	1	1	x	x	1	0
1	x	x	1	1	x	0
1	x	x	1	x	1	0
1	x	1	x	x	1	0

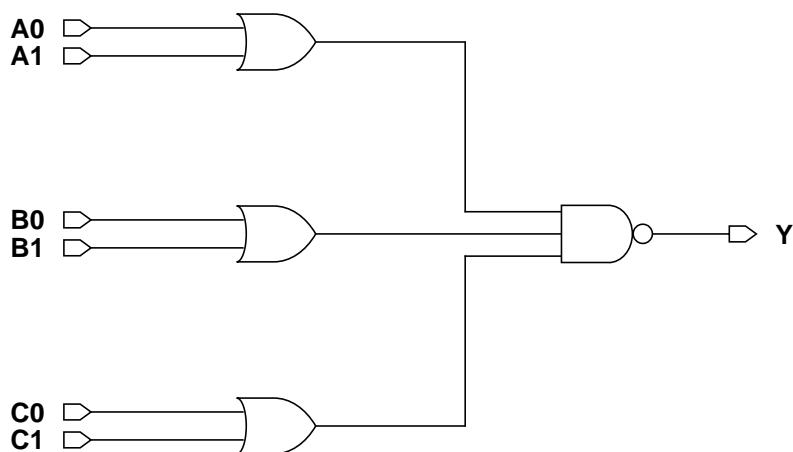
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI222XL	2.52	2.80
OAI222X1	2.52	2.80
OAI222X2	2.52	3.08
OAI222X4	2.52	5.04

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0042	0.0055	0.0075	0.0144
A1	0.0046	0.0060	0.0083	0.0159
B0	0.0051	0.0065	0.0093	0.0182
B1	0.0054	0.0070	0.0099	0.0197
C0	0.0030	0.0041	0.0055	0.0107
C1	0.0033	0.0046	0.0062	0.0121

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0018	0.0024	0.0048
A1	0.0013	0.0016	0.0024	0.0044
B0	0.0013	0.0017	0.0024	0.0047
B1	0.0011	0.0015	0.0020	0.0043
C0	0.0013	0.0017	0.0024	0.0048
C1	0.0013	0.0017	0.0023	0.0043

Delays at 25°C, 1.0V, Typical Process

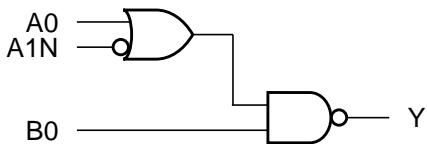
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0565	0.0475	0.0500	0.0477	11.9092	7.6291	5.5955	2.8398
A0 → Y↓	0.0602	0.0576	0.0413	0.0381	10.0254	7.0313	3.6263	1.7543
A1 → Y↑	0.0614	0.0516	0.0550	0.0524	11.9036	7.6250	5.5942	2.8388
A1 → Y↓	0.0655	0.0626	0.0453	0.0422	9.8977	6.9381	3.5845	1.7553
B0 → Y↑	0.0657	0.0543	0.0664	0.0624	11.5458	7.3993	5.9522	2.8974
B0 → Y↓	0.0658	0.0617	0.0447	0.0429	9.9196	6.9456	3.4975	1.7535
B1 → Y↑	0.0688	0.0581	0.0708	0.0665	11.5395	7.3966	5.9500	2.8967
B1 → Y↓	0.0707	0.0675	0.0495	0.0468	9.9061	6.9363	3.5835	1.7557
C0 → Y↑	0.0382	0.0335	0.0344	0.0334	11.5503	7.4072	5.4256	2.7715
C0 → Y↓	0.0440	0.0444	0.0314	0.0311	9.9938	7.0072	3.6333	1.8232
C1 → Y↑	0.0427	0.0379	0.0388	0.0378	11.5374	7.4013	5.4229	2.7704
C1 → Y↓	0.0491	0.0499	0.0351	0.0336	9.9064	6.9380	3.5849	1.7559

Cell Description

The OAI2B1 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + \overline{A_{1N}})} \bullet B_0$$

Logic Symbol



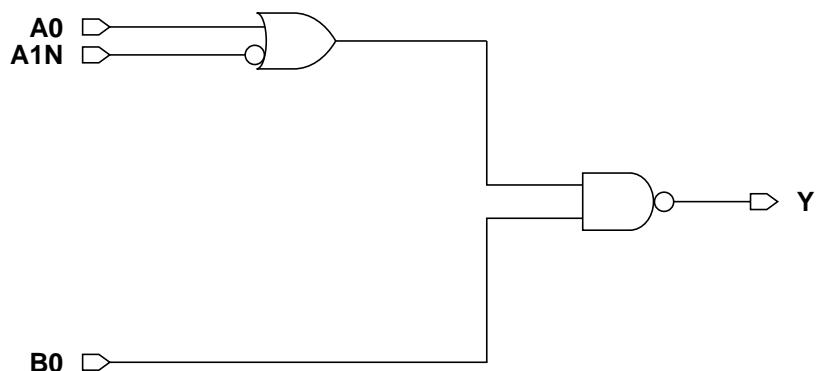
Functions

A0	A1N	B0	Y
0	1	x	1
x	x	0	1
x	0	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B1XL	2.52	1.96
OAI2B1X1	2.52	1.96
OAI2B1X2	2.52	2.24
OAI2B1X4	2.52	3.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0023	0.0030	0.0045	0.0084
A1N	0.0027	0.0035	0.0053	0.0100
B0	0.0019	0.0025	0.0034	0.0065

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0045
A1N	0.0010	0.0011	0.0013	0.0019
B0	0.0013	0.0017	0.0024	0.0045

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0335	0.0281	0.0319	0.0307	11.3923	7.2444	5.4017	2.7755
A0 → Y↓	0.0221	0.0207	0.0163	0.0155	7.0135	4.9397	2.4558	1.2320
A1N → Y↑	0.0511	0.0480	0.0515	0.0535	11.3594	7.2366	5.3978	2.7744
A1N → Y↓	0.0602	0.0638	0.0535	0.0493	7.1523	5.0530	2.5106	1.2343
B0 → Y↑	0.0152	0.0135	0.0138	0.0134	5.6805	3.6505	2.6872	1.3740
B0 → Y↓	0.0216	0.0212	0.0155	0.0147	7.1403	5.0423	2.5031	1.2307

Cell Description

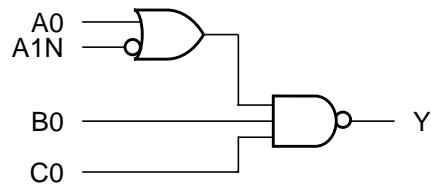
The OAI2B11 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N})} \bullet B0 \bullet C0$$

Functions

A0	A1N	B0	C0	Y
0	1	x	x	1
x	x	0	x	1
x	x	x	0	1
x	0	1	1	0
1	x	1	1	0

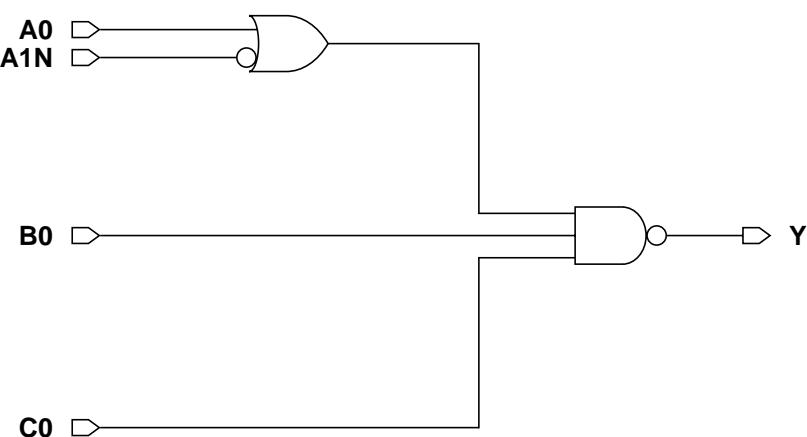
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B11XL	2.52	2.24
OAI2B11X1	2.52	2.24
OAI2B11X2	2.52	2.24
OAI2B11X4	2.52	3.92

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0028	0.0038	0.0058	0.0113
A1N	0.0032	0.0043	0.0066	0.0129
B0	0.0020	0.0028	0.0039	0.0073
C0	0.0023	0.0032	0.0048	0.0091

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0048
A1N	0.0011	0.0011	0.0014	0.0019
B0	0.0013	0.0017	0.0024	0.0045
C0	0.0013	0.0017	0.0024	0.0048

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0415	0.0367	0.0415	0.0413	11.5595	7.3897	5.3613	2.7354
A0 → Y↓	0.0345	0.0336	0.0260	0.0253	9.8326	6.8956	3.4519	1.7147
A1N → Y↑	0.0597	0.0571	0.0602	0.0633	11.5478	7.3825	5.3605	2.7339
A1N → Y↓	0.0744	0.0780	0.0624	0.0573	9.9977	7.0150	3.5257	1.7295
B0 → Y↑	0.0170	0.0157	0.0165	0.0164	5.6506	3.6412	2.6886	1.4042
B0 → Y↓	0.0322	0.0323	0.0237	0.0223	10.0082	7.0188	3.5265	1.7288
C0 → Y↑	0.0194	0.0179	0.0196	0.0193	5.8227	3.7559	2.7647	1.3816
C0 → Y↓	0.0355	0.0359	0.0270	0.0262	10.0065	7.0183	3.5268	1.7296

Cell Description

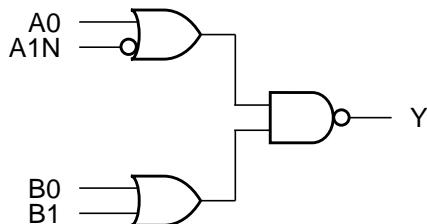
The OAI2B2 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + \overline{A_1N})} \bullet (B_0 + B_1)$$

Functions

A0	A1N	B0	B1	Y
0	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
1	x	x	1	0
1	x	1	x	0

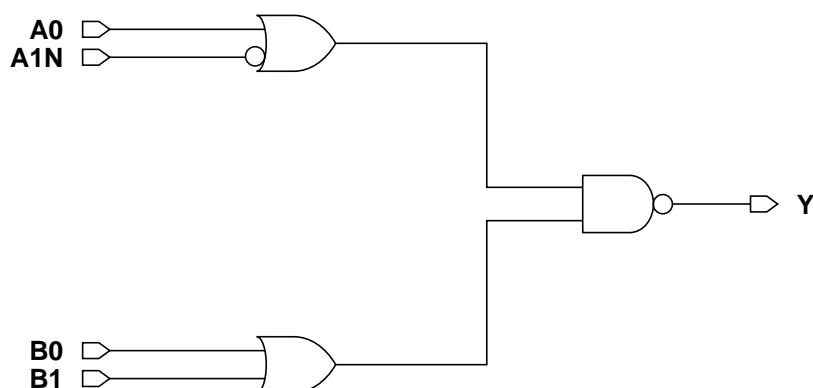
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B2XL	2.52	2.24
OAI2B2X1	2.52	2.24
OAI2B2X2	2.52	2.52
OAI2B2X4	2.52	3.92

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0021	0.0029	0.0040	0.0080
A1N	0.0029	0.0036	0.0048	0.0095
B0	0.0028	0.0037	0.0053	0.0102
B1	0.0032	0.0043	0.0060	0.0118

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0045
A1N	0.0011	0.0011	0.0014	0.0020
B0	0.0013	0.0017	0.0024	0.0045
B1	0.0011	0.0015	0.0022	0.0047

Delays at 25°C, 1.0V, Typical Process

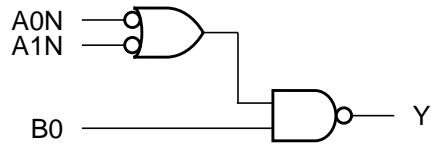
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0269	0.0242	0.0251	0.0249	11.6030	7.4288	5.4512	2.7795
A0 → Y↓	0.0223	0.0224	0.0163	0.0160	7.1033	4.9647	2.4695	1.2279
A1N → Y↑	0.0466	0.0455	0.0448	0.0479	11.5878	7.4228	5.4466	2.7785
A1N → Y↓	0.0642	0.0689	0.0546	0.0509	7.3017	5.1034	2.5255	1.2292
B0 → Y↑	0.0412	0.0352	0.0391	0.0384	11.3379	7.2809	5.3337	2.7351
B0 → Y↓	0.0320	0.0314	0.0242	0.0230	7.1507	4.9972	2.4995	1.2322
B1 → Y↑	0.0454	0.0394	0.0434	0.0436	11.3225	7.2742	5.3302	2.7344
B1 → Y↓	0.0366	0.0364	0.0272	0.0261	7.2913	5.0993	2.5248	1.2292

Cell Description

The OAI2BB1 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N})} \bullet B0$$

Logic Symbol



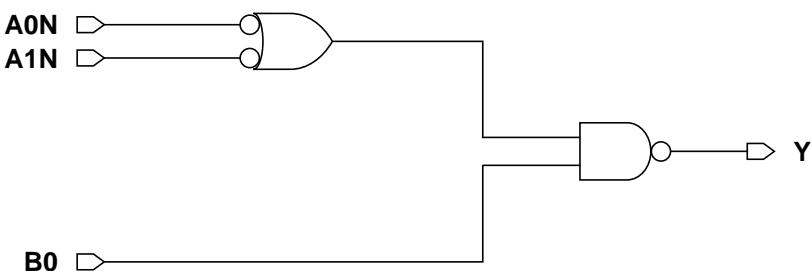
Functions

A0N	A1N	B0	Y
1	1	x	1
x	x	0	1
x	0	1	0
0	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2BB1XL	2.52	1.68
OAI2BB1X1	2.52	1.68
OAI2BB1X2	2.52	1.96
OAI2BB1X4	2.52	2.52

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0N	0.0029	0.0035	0.0048	0.0086
A1N	0.0026	0.0031	0.0043	0.0077
B0	0.0015	0.0020	0.0029	0.0056

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0008	0.0008	0.0011	0.0018
A1N	0.0007	0.0007	0.0008	0.0013
B0	0.0010	0.0013	0.0019	0.0038

Delays at 25°C, 1.0V, Typical Process

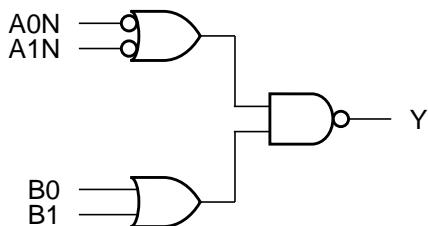
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0412	0.0426	0.0397	0.0396	5.6539	3.6488	2.6687	1.3949
A0N → Y↓	0.0601	0.0647	0.0552	0.0494	7.1121	4.9791	2.4871	1.2187
A1N → Y↑	0.0399	0.0413	0.0381	0.0380	5.6516	3.6486	2.6699	1.3952
A1N → Y↓	0.0542	0.0584	0.0495	0.0442	7.0806	4.9631	2.4809	1.2157
B0 → Y↑	0.0155	0.0144	0.0157	0.0155	5.6065	3.6391	2.6998	1.3615
B0 → Y↓	0.0179	0.0183	0.0150	0.0146	7.0094	4.9325	2.4659	1.2105

Cell Description

The OAI2BB2 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and one OR group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(A0N + A1N)} \bullet (B0 + B1)$$

Logic Symbol



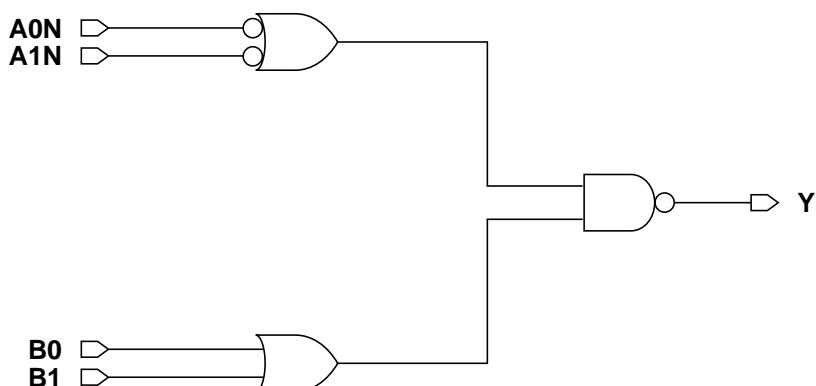
Functions

A0N	A1N	B0	B1	Y
1	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
0	x	x	1	0
0	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2BB2XL	2.52	2.24
OAI2BB2X1	2.52	2.24
OAI2BB2X2	2.52	2.24
OAI2BB2X4	2.52	3.64

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0N	0.0033	0.0038	0.0052	0.0095
A1N	0.0027	0.0031	0.0043	0.0078
B0	0.0020	0.0025	0.0034	0.0064
B1	0.0023	0.0031	0.0041	0.0081

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0011	0.0010	0.0013	0.0021
A1N	0.0011	0.0010	0.0015	0.0022
B0	0.0013	0.0017	0.0023	0.0044
B1	0.0012	0.0016	0.0022	0.0046

Delays at 25°C, 1.0V, Typical Process

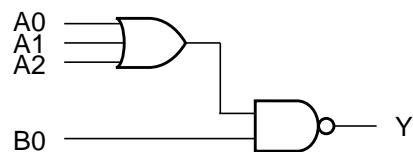
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0439	0.0450	0.0417	0.0405	5.7390	3.6790	2.6990	1.3809
A0N → Y↓	0.0662	0.0705	0.0579	0.0543	7.2838	5.0774	2.5520	1.3149
A1N → Y↑	0.0417	0.0429	0.0395	0.0384	5.7119	3.6627	2.6870	1.3751
A1N → Y↓	0.0573	0.0615	0.0510	0.0477	7.1628	4.9880	2.4908	1.3229
B0 → Y↑	0.0327	0.0283	0.0303	0.0295	11.4278	7.2985	5.4014	2.7814
B0 → Y↓	0.0225	0.0221	0.0176	0.0176	7.0722	4.9481	2.4750	1.3164
B1 → Y↑	0.0370	0.0325	0.0349	0.0346	11.4036	7.2923	5.3972	2.7804
B1 → Y↓	0.0268	0.0269	0.0211	0.0207	7.2154	5.0475	2.5415	1.3100

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1 + A_2) \bullet B_0}$$

Logic Symbol



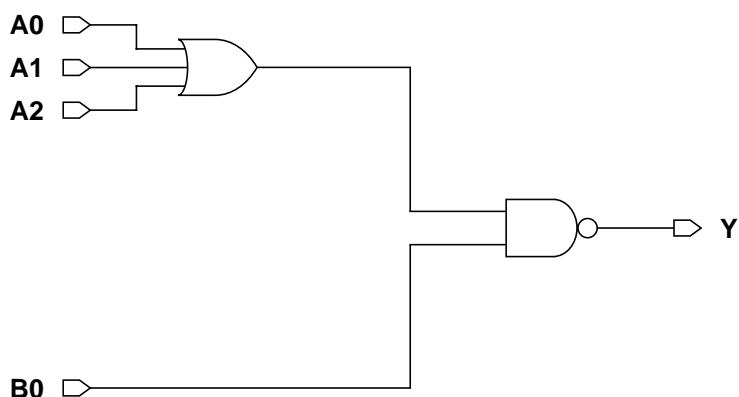
Functions

A0	A1	A2	B0	Y
0	0	0	x	1
x	x	x	0	1
x	x	1	1	0
x	1	x	1	0
1	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI31XL	2.52	1.68
OAI31X1	2.52	1.68
OAI31X2	2.52	1.96
OAI31X4	2.52	3.36

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0024	0.0031	0.0049	0.0091
A1	0.0027	0.0037	0.0056	0.0107
A2	0.0031	0.0042	0.0064	0.0122
B0	0.0022	0.0031	0.0043	0.0078

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0043
A1	0.0012	0.0016	0.0023	0.0046
A2	0.0011	0.0015	0.0022	0.0048
B0	0.0013	0.0017	0.0024	0.0042

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0454	0.0396	0.0466	0.0434	16.9331	10.8738	8.0098	4.1092
A0 → Y↓	0.0218	0.0211	0.0171	0.0164	6.9826	4.8879	2.4458	1.3010
A1 → Y↑	0.0561	0.0499	0.0567	0.0553	16.9080	10.8613	8.0035	4.1071
A1 → Y↓	0.0259	0.0256	0.0199	0.0198	7.0412	4.9277	2.4703	1.3057
A2 → Y↑	0.0604	0.0542	0.0610	0.0603	16.9058	10.8639	8.0044	4.1076
A2 → Y↓	0.0286	0.0287	0.0216	0.0215	7.2544	5.0547	2.5101	1.3149
B0 → Y↑	0.0146	0.0135	0.0138	0.0137	5.6814	3.6364	2.7185	1.4910
B0 → Y↓	0.0238	0.0246	0.0173	0.0171	7.2772	5.0655	2.5123	1.3165

Cell Description

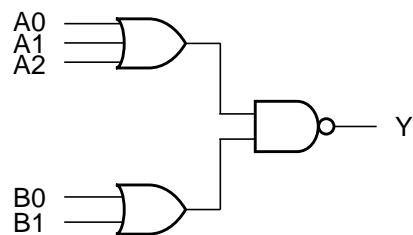
The OAI32 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1 + A_2)} \bullet (B_0 + B_1)$$

Functions

A0	A1	A2	B0	B1	Y
0	0	0	x	x	1
x	x	x	0	0	1
x	x	1	x	1	0
x	x	1	1	x	0
x	1	x	1	x	0
x	1	x	x	1	0
1	x	x	1	x	0
1	x	x	x	1	0

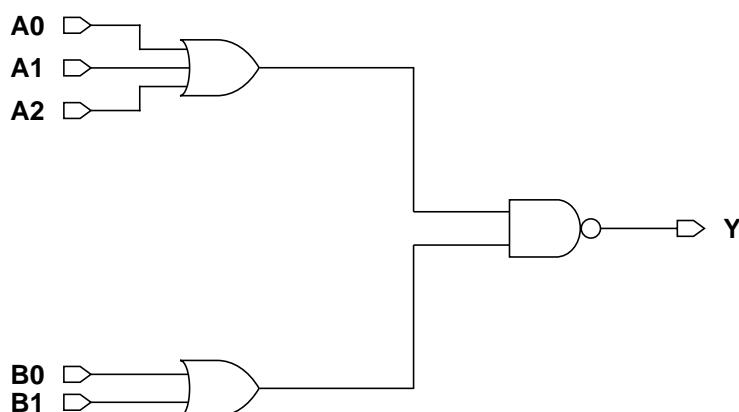
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI32XL	2.52	1.96
OAI32X1	2.52	2.24
OAI32X2	2.52	2.24
OAI32X4	2.52	4.20

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A0	0.0034	0.0043	0.0064	0.0127
A1	0.0038	0.0049	0.0071	0.0144
A2	0.0041	0.0054	0.0079	0.0159
B0	0.0026	0.0034	0.0046	0.0095
B1	0.0029	0.0040	0.0052	0.0109

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0025	0.0044
A1	0.0012	0.0016	0.0023	0.0046
A2	0.0012	0.0016	0.0022	0.0049
B0	0.0013	0.0017	0.0023	0.0045
B1	0.0012	0.0017	0.0022	0.0044

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0613	0.0506	0.0585	0.0580	17.2025	11.0600	8.0085	4.1417
A0 → Y↓	0.0309	0.0289	0.0219	0.0225	7.0826	4.9003	2.4638	1.2917
A1 → Y↑	0.0729	0.0614	0.0683	0.0702	17.1834	11.0490	8.0024	4.1400
A1 → Y↓	0.0357	0.0337	0.0247	0.0260	7.1378	4.9169	2.4724	1.2954
A2 → Y↑	0.0771	0.0662	0.0727	0.0755	17.1797	11.0491	8.0024	4.1399
A2 → Y↓	0.0390	0.0372	0.0268	0.0281	7.3345	5.0103	2.5129	1.3007
B0 → Y↑	0.0275	0.0235	0.0283	0.0261	11.4262	7.3471	6.4265	2.8972
B0 → Y↓	0.0259	0.0253	0.0179	0.0181	7.1796	4.9533	2.4809	1.2377
B1 → Y↑	0.0324	0.0284	0.0331	0.0314	11.4121	7.3419	6.4230	2.8953
B1 → Y↓	0.0312	0.0306	0.0207	0.0223	7.3395	5.0096	2.5131	1.3009

Cell Description

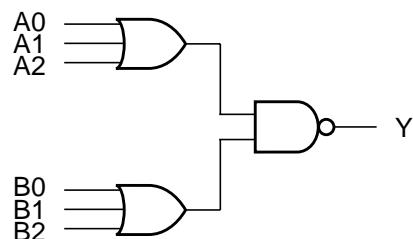
The OAI33 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1 + A_2) \bullet (B_0 + B_1 + B_2)}$$

Functions

A0	A1	A2	B0	B1	B2	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
x	x	1	x	x	1	0
x	x	1	x	1	x	0
x	x	1	1	x	x	0
x	1	x	x	x	1	0
x	1	x	x	1	x	0
1	x	x	x	x	1	0
1	x	x	x	1	x	0
1	x	x	1	x	x	0

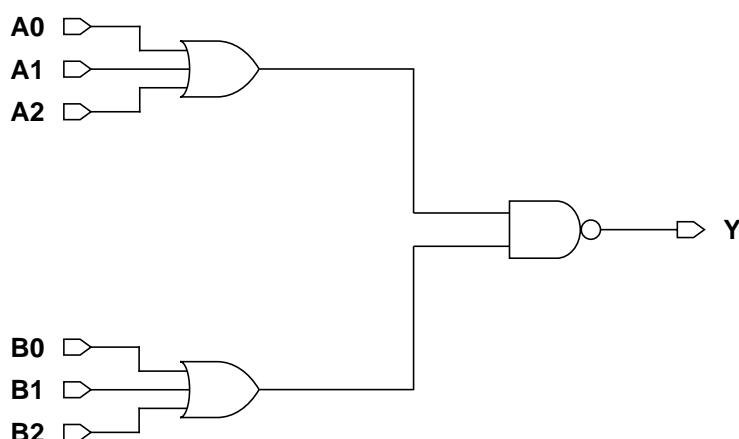
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
OAI33XL	2.52	2.52
OAI33X1	2.52	2.52
OAI33X2	2.52	2.52
OAI33X4	2.52	4.76

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A0	0.0030	0.0040	0.0057	0.0109
A1	0.0034	0.0046	0.0065	0.0125
A2	0.0038	0.0052	0.0072	0.0141
B0	0.0042	0.0055	0.0082	0.0161
B1	0.0046	0.0060	0.0089	0.0177
B2	0.0049	0.0066	0.0096	0.0191

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0024	0.0045
A1	0.0012	0.0016	0.0023	0.0047
A2	0.0013	0.0017	0.0023	0.0048
B0	0.0013	0.0017	0.0024	0.0043
B1	0.0013	0.0016	0.0022	0.0047
B2	0.0012	0.0016	0.0021	0.0047

Delays at 25°C, 1.0V, Typical Process

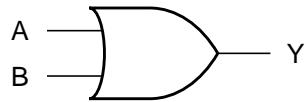
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0442	0.0368	0.0397	0.0382	17.3836	11.1726	8.1743	4.1762
A0 → Y↓	0.0285	0.0277	0.0222	0.0191	7.1171	4.9658	2.8441	1.2251
A1 → Y↑	0.0558	0.0481	0.0514	0.0509	17.3609	11.1632	8.1703	4.1748
A1 → Y↓	0.0334	0.0329	0.0265	0.0228	7.1302	4.9747	2.8675	1.2292
A2 → Y↑	0.0623	0.0537	0.0563	0.0556	17.3781	11.1674	8.1713	4.1743
A2 → Y↓	0.0380	0.0375	0.0297	0.0266	7.2711	5.0644	2.9122	1.3109
B0 → Y↑	0.0726	0.0602	0.0701	0.0721	17.2285	11.0766	8.1114	4.2856
B0 → Y↓	0.0371	0.0355	0.0267	0.0270	7.1122	4.9640	2.4959	1.3023
B1 → Y↑	0.0842	0.0710	0.0809	0.0844	17.2082	11.0680	8.1058	4.2838
B1 → Y↓	0.0421	0.0407	0.0303	0.0307	7.1322	4.9830	2.5141	1.3043
B2 → Y↑	0.0883	0.0757	0.0849	0.0902	17.2078	11.0677	8.1056	4.2836
B2 → Y↓	0.0457	0.0448	0.0378	0.0329	7.2735	5.0614	2.9124	1.3109

Cell Description

The OR2 cell provides the logical OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A + B)$$

Logic Symbol



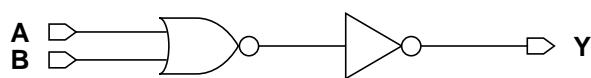
Functions

A	B	Y
0	0	0
x	1	1
1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR2XL	2.52	1.40
OR2X1	2.52	1.40
OR2X2	2.52	1.40
OR2X4	2.52	2.52
OR2X6	2.52	2.80
OR2X8	2.52	3.64

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X4	X6	X8
A	0.0027	0.0032	0.0046	0.0079	0.0114	0.0155
B	0.0029	0.0036	0.0051	0.0093	0.0130	0.0176

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0011	0.0012	0.0017	0.0029	0.0037	0.0056
B	0.0011	0.0013	0.0017	0.0032	0.0040	0.0054

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0273	0.0296	0.0291	0.0304	0.0313	0.0296
A → Y↓	0.0699	0.0608	0.0530	0.0417	0.0454	0.0459
B → Y↑	0.0287	0.0319	0.0315	0.0356	0.0360	0.0330
B → Y↓	0.0757	0.0663	0.0582	0.0473	0.0509	0.0510

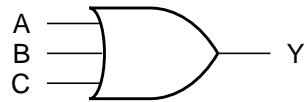
Description	K _{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	5.5430	3.5757	2.6408	1.3592	0.9205	0.6963
A → Y↓	4.7316	3.1367	1.5704	0.7538	0.5070	0.3787
B → Y↑	5.5532	3.5825	2.6438	1.3620	0.9220	0.6974
B → Y↓	4.7318	3.1367	1.5706	0.7537	0.5069	0.3786

Cell Description

The OR3 cell provides the logical OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (A + B + C)$$

Logic Symbol



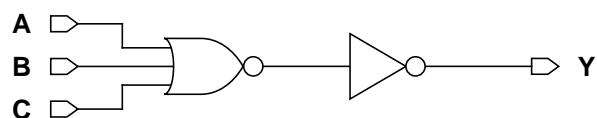
Functions

A	B	C	Y
0	0	0	0
x	x	1	1
x	1	x	1
1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR3XL	2.52	1.68
OR3X1	2.52	1.68
OR3X2	2.52	1.68
OR3X4	2.52	2.80
OR3X6	2.52	4.20
OR3X8	2.52	5.60

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X4	X6	X8
A	0.0035	0.0042	0.0056	0.0094	0.0146	0.0187
B	0.0039	0.0047	0.0063	0.0110	0.0169	0.0217
C	0.0042	0.0051	0.0071	0.0126	0.0190	0.0247

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0012	0.0015	0.0020	0.0034	0.0051	0.0072
B	0.0013	0.0015	0.0020	0.0036	0.0055	0.0073
C	0.0012	0.0014	0.0020	0.0038	0.0053	0.0073

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0333	0.0345	0.0328	0.0345	0.0338	0.0332
A → Y↓	0.0843	0.0713	0.0598	0.0512	0.0549	0.0516
B → Y↑	0.0356	0.0382	0.0369	0.0403	0.0389	0.0383
B → Y↓	0.0966	0.0833	0.0714	0.0629	0.0676	0.0630
C → Y↑	0.0369	0.0405	0.0394	0.0443	0.0423	0.0422
C → Y↓	0.1009	0.0877	0.0757	0.0677	0.0721	0.0687

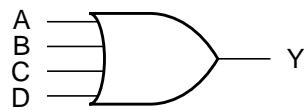
Description	K _{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	5.6063	3.6129	2.6750	1.3724	0.9256	0.7270
A → Y↓	5.0348	3.2876	1.6353	0.7917	0.5298	0.3927
B → Y↑	5.6183	3.6229	2.6791	1.3753	0.9275	0.7283
B → Y↓	5.0339	3.2873	1.6352	0.7916	0.5296	0.3926
C → Y↑	5.6479	3.6419	2.6879	1.3806	0.9309	0.7308
C → Y↓	5.0347	3.2870	1.6349	0.7916	0.5296	0.3926

Cell Description

The OR4 cell provides the logical OR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (A + B + C + D)$$

Logic Symbol



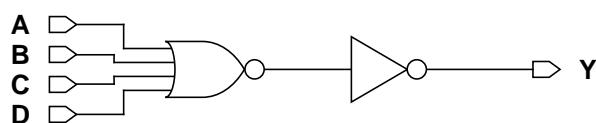
Functions

A	B	C	D	Y
0	0	0	0	0
x	x	x	1	1
x	x	1	x	1
x	1	x	x	1
1	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR4XL	2.52	2.24
OR4X1	2.52	2.24
OR4X2	2.52	2.24
OR4X4	2.52	3.64
OR4X6	2.52	5.32
OR4X8	2.52	7.00

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X4	X6	X8
A	0.0038	0.0045	0.0062	0.0104	0.0168	0.0209
B	0.0041	0.0049	0.0069	0.0120	0.0189	0.0239
C	0.0043	0.0053	0.0076	0.0135	0.0209	0.0267
D	0.0046	0.0057	0.0084	0.0149	0.0232	0.0298

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X4	X6	X8
A	0.0011	0.0013	0.0020	0.0033	0.0057	0.0073
B	0.0011	0.0013	0.0019	0.0036	0.0053	0.0071
C	0.0011	0.0013	0.0019	0.0037	0.0054	0.0073
D	0.0012	0.0014	0.0020	0.0038	0.0057	0.0082

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X4	X6	X8
A → Y↑	0.0312	0.0335	0.0334	0.0351	0.0356	0.0340
A → Y↓	0.1158	0.0965	0.0731	0.0625	0.0706	0.0647
B → Y↑	0.0328	0.0364	0.0373	0.0409	0.0408	0.0394
B → Y↓	0.1348	0.1154	0.0915	0.0816	0.0890	0.0833
C → Y↑	0.0339	0.0383	0.0400	0.0449	0.0445	0.0434
C → Y↓	0.1459	0.1261	0.1018	0.0926	0.1002	0.0944
D → Y↑	0.0347	0.0396	0.0416	0.0475	0.0475	0.0463
D → Y↓	0.1537	0.1328	0.1075	0.0991	0.1065	0.1010

Delay Table at 25°C, 1.0V, Typical Process

Description	K_{load} (ns/pF)					
	XL	X1	X2	X4	X6	X8
A → Y↑	5.6331	3.6168	2.6890	1.3750	0.9272	0.7277
A → Y↓	5.7098	3.5631	1.7364	0.8459	0.5696	0.4204
B → Y↑	5.6425	3.6253	2.6939	1.3781	0.9292	0.7292
B → Y↓	5.7084	3.5614	1.7358	0.8460	0.5694	0.4203
C → Y↑	5.6695	3.6421	2.7025	1.3833	0.9325	0.7319
C → Y↓	5.7100	3.5616	1.7360	0.8460	0.5695	0.4203
D → Y↑	5.7076	3.6682	2.7164	1.3922	0.9382	0.7365
D → Y↓	5.7113	3.5608	1.7358	0.8460	0.5695	0.4203

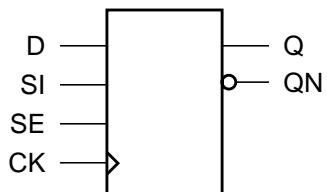
Cell Description

The SDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Functions

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	/	1	0
0	x	0	/	0	1
x	x	x	\	Q[n]	QN[n]
x	1	1	/	1	0
x	0	1	/	0	1

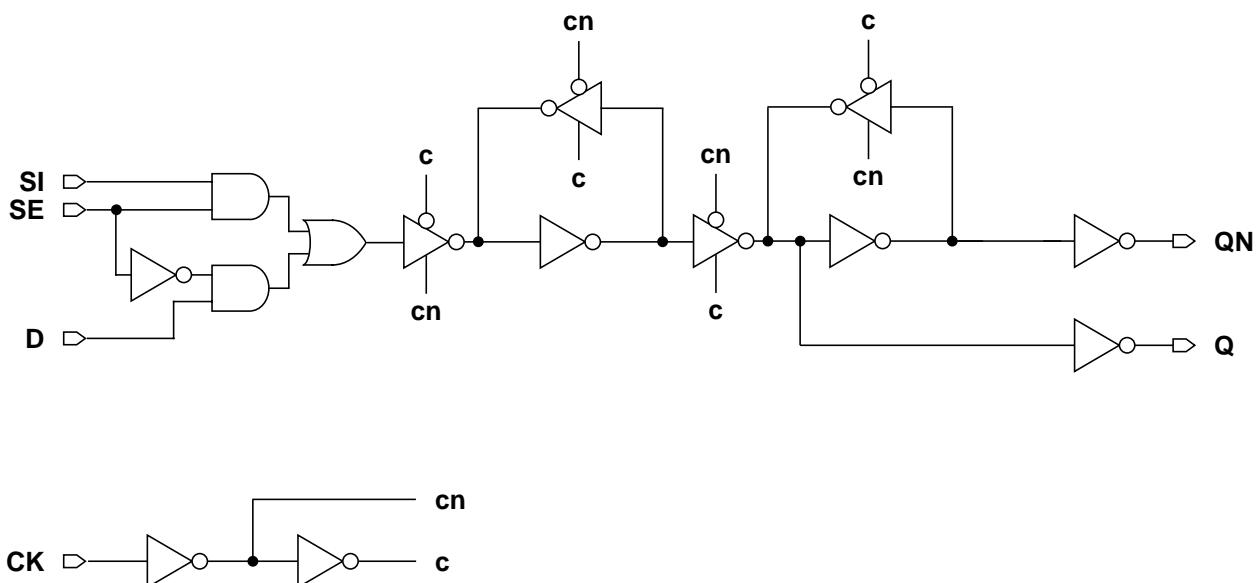
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFXL	2.52	7.56
SDFFX1	2.52	7.56
SDFFX2	2.52	7.56
SDFFX4	2.52	9.52

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
SI	0.0068	0.0070	0.0064	0.0073
SE	0.0081	0.0083	0.0077	0.0085
D	0.0060	0.0062	0.0058	0.0066
CK	0.0112	0.0113	0.0111	0.0126
Q	0.0053	0.0063	0.0077	0.0131

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0011	0.0011	0.0010	0.0010
SE	0.0029	0.0029	0.0025	0.0025
D	0.0015	0.0016	0.0010	0.0010
CK	0.0016	0.0017	0.0016	0.0018

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1080	0.1044	0.0975	0.0956	5.8470	3.7053	2.6759	1.3671
CK → Q↓	0.1244	0.1199	0.1030	0.0965	5.4301	3.4452	1.6591	0.8147
CK → QN↑	0.1532	0.1489	0.1407	0.1401	5.6813	3.6438	2.6524	1.3622
CK → QN↓	0.1473	0.1495	0.1475	0.1435	4.5999	3.1294	1.5662	0.7693

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.0820	0.0820	0.0625	0.0703
	setup↓ → CK	0.1914	0.1914	0.2070	0.2188
	hold↑ → CK	-0.0625	-0.0625	-0.0430	-0.0469
	hold↓ → CK	-0.1484	-0.1523	-0.1641	-0.1680
SE	setup↑ → CK	0.1914	0.1914	0.2148	0.2305
	setup↓ → CK	0.0938	0.0938	0.1836	0.1953
	hold↑ → CK	-0.0586	-0.0625	-0.0391	-0.0391
	hold↓ → CK	-0.0312	-0.0352	-0.0625	-0.0664
D	setup↑ → CK	0.0703	0.0703	0.0547	0.0625
	setup↓ → CK	0.0703	0.0742	0.1836	0.1992
	hold↑ → CK	-0.0547	-0.0547	-0.0391	-0.0391
	hold↓ → CK	-0.0312	-0.0352	-0.1445	-0.1523
CK	minpwh	0.1028	0.0979	0.0882	0.0833
	minpwl	0.0833	0.0833	0.0784	0.0784

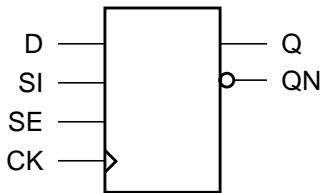
Cell Description

The SDFFH cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and fast clock-to-Q-path.

Functions

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	/	1	0
0	x	0	/	0	1
x	x	x	\	Q[n]	QN[n]
x	1	1	/	1	0
x	0	1	/	0	1

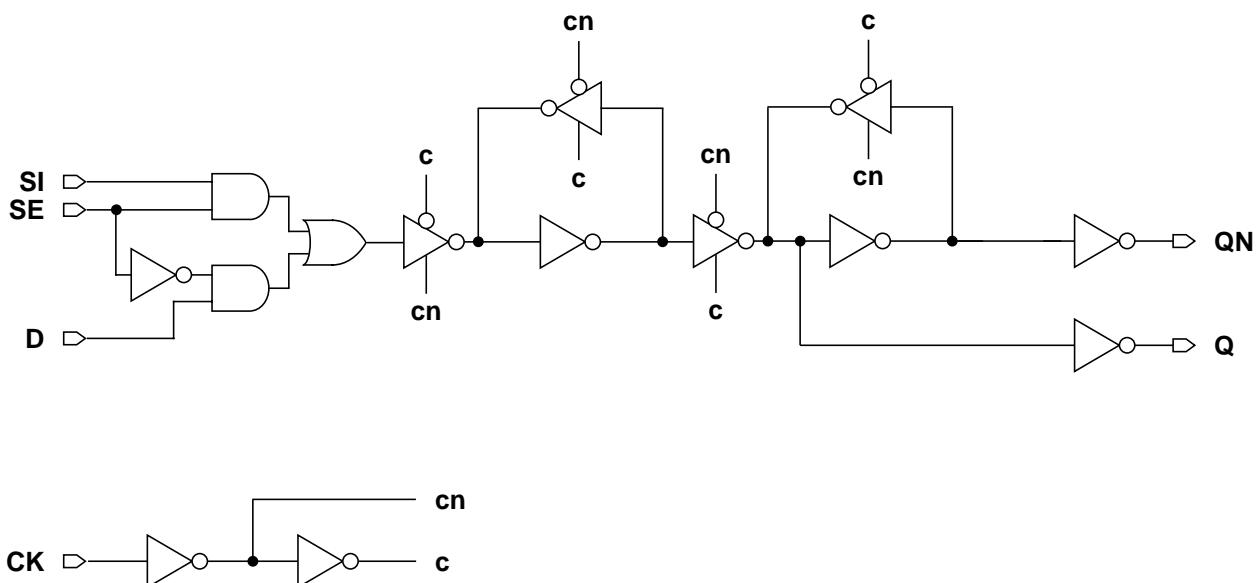
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFHX1	2.52	8.40
SDFFHX2	2.52	9.24
SDFFHX4	2.52	10.64
SDFFHX8	2.52	11.48

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
SI	0.0074	0.0089	0.0125	0.0128
SE	0.0101	0.0121	0.0147	0.0149
D	0.0085	0.0102	0.0140	0.0143
CK	0.0152	0.0179	0.0228	0.0229
Q	0.0052	0.0062	0.0082	0.0147

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0013	0.0013	0.0016	0.0016
SE	0.0030	0.0032	0.0031	0.0031
D	0.0013	0.0015	0.0019	0.0019
CK	0.0023	0.0022	0.0029	0.0029

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0769	0.0761	0.0688	0.0779	3.5775	2.6056	1.4719	0.6879
CK → Q↓	0.0805	0.0767	0.0763	0.0894	3.2213	1.5767	0.8535	0.4064
CK → QN↑	0.1090	0.1138	0.1142	0.1317	5.5264	11.1186	10.1437	10.1412
CK → QN↓	0.1309	0.1278	0.1187	0.1319	4.3202	4.1872	4.1708	4.1620

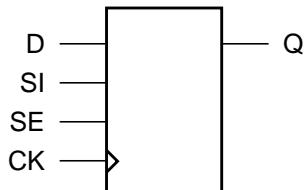
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.0703	0.0664	0.0625	0.0625
	setup↓ → CK	0.1016	0.1133	0.1055	0.1055
	hold↑ → CK	-0.0312	-0.0273	-0.0273	-0.0234
	hold↓ → CK	-0.0703	-0.0742	-0.0703	-0.0703
SE	setup↑ → CK	0.1289	0.1367	0.1289	0.1250
	setup↓ → CK	0.0938	0.0820	0.0781	0.0781
	hold↑ → CK	-0.0312	-0.0273	-0.0273	-0.0234
	hold↓ → CK	-0.0508	-0.0391	-0.0391	-0.0391
D	setup↑ → CK	0.0781	0.0664	0.0625	0.0625
	setup↓ → CK	0.0898	0.0820	0.0742	0.0742
	hold↑ → CK	-0.0352	-0.0273	-0.0273	-0.0234
	hold↓ → CK	-0.0586	-0.0469	-0.0430	-0.0391
CK	minpwh	0.0444	0.0444	0.0444	0.0444
	minpwl	0.1125	0.1076	0.0882	0.0882

Cell Description

The SDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



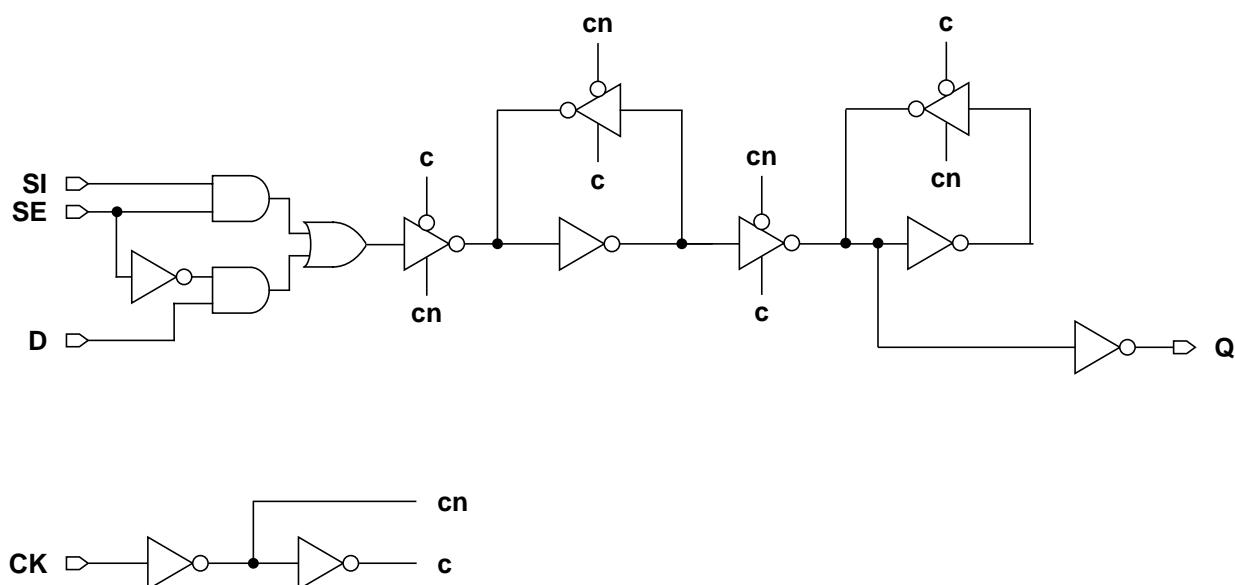
Functions

D	SI	SE	CK	Q[n+1]
1	x	0	/	1
0	x	0	/	0
x	x	x	\	Q[n]
x	1	1	/	1
x	0	1	/	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFHQX1	2.52	8.40
SDFFHQX2	2.52	8.96
SDFFHQX4	2.52	9.80
SDFFHQX8	2.52	10.92

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
SI	0.0076	0.0090	0.0134	0.0139
SE	0.0095	0.0110	0.0150	0.0151
D	0.0080	0.0093	0.0138	0.0142
CK	0.0145	0.0171	0.0230	0.0230
Q	0.0039	0.0049	0.0071	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0013	0.0012	0.0014	0.0013
SE	0.0026	0.0028	0.0033	0.0033
D	0.0015	0.0014	0.0020	0.0020
CK	0.0022	0.0022	0.0028	0.0028

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0816	0.0752	0.0691	0.0772	3.6265	2.6080	1.3421	0.6946
CK → Q↓	0.0834	0.0775	0.0716	0.0823	3.1968	1.5859	0.7752	0.3932

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.0781	0.0664	0.0664	0.0703
	setup↓ → CK	0.1172	0.1172	0.1289	0.1289
	hold↑ → CK	-0.0312	-0.0312	-0.0312	-0.0312
	hold↓ → CK	-0.0820	-0.0820	-0.0938	-0.0938
SE	setup↑ → CK	0.1328	0.1289	0.1484	0.1484
	setup↓ → CK	0.0938	0.0781	0.0742	0.0781
	hold↑ → CK	-0.0234	-0.0234	-0.0234	-0.0234
	hold↓ → CK	-0.0391	-0.0312	-0.0312	-0.0312
D	setup↑ → CK	0.0781	0.0586	0.0547	0.0586
	setup↓ → CK	0.0742	0.0742	0.0703	0.0664
	hold↑ → CK	-0.0352	-0.0234	-0.0195	-0.0195
	hold↓ → CK	-0.0391	-0.0430	-0.0391	-0.0352
CK	minpwh	0.0444	0.0444	0.0444	0.0444
	minpw1	0.1174	0.1028	0.0882	0.0930

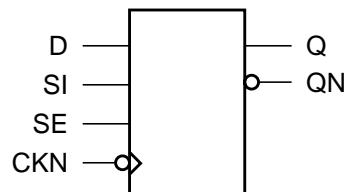
Cell Description

The SDFFNH cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and fast clock-to-Q-path.

Functions

D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	x	0	—	1	0
0	x	0	—	0	1
x	x	x	—	Q[n]	QN[n]
x	1	1	—	1	0
x	0	1	—	0	1

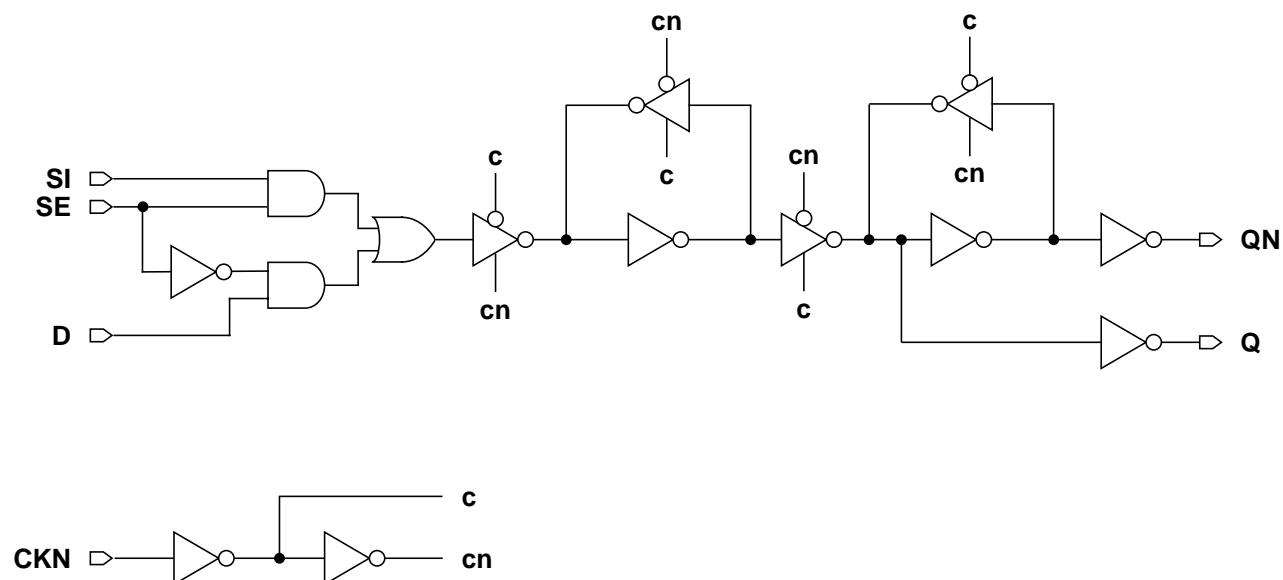
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNHNX1	2.52	8.12
SDFFNHNX2	2.52	8.68
SDFFNHNX4	2.52	10.92
SDFFNHNX8	2.52	11.76

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
SI	0.0070	0.0073	0.0121	0.0126
SE	0.0093	0.0093	0.0144	0.0149
D	0.0081	0.0084	0.0135	0.0141
CKN	0.0122	0.0125	0.0195	0.0197
Q	0.0058	0.0064	0.0093	0.0146

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0012	0.0012	0.0015	0.0015
SE	0.0027	0.0025	0.0028	0.0030
D	0.0014	0.0016	0.0019	0.0019
CKN	0.0021	0.0022	0.0025	0.0027

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CKN → Q↑	0.1506	0.1478	0.1440	0.1497	3.5778	2.6290	1.3308	0.6848
CKN → Q↓	0.1306	0.1264	0.1115	0.1311	3.2699	1.6553	0.7771	0.4023
CKN → QN↑	0.1610	0.1654	0.1492	0.1745	5.4686	11.1607	11.1261	11.1428
CKN → QN↓	0.1936	0.1875	0.1980	0.2082	4.2319	4.1718	4.1725	4.1592

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CKN	-0.0039	-0.0078	-0.0117	-0.0078
	setup↓ → CKN	0.0586	0.0742	0.0703	0.0742
	hold↑ → CKN	0.0352	0.0391	0.0352	0.0352
	hold↓ → CKN	-0.0312	-0.0430	-0.0469	-0.0469
SE	setup↑ → CKN	0.0781	0.0938	0.0938	0.0977
	setup↓ → CKN	0.0391	0.0508	0.0508	0.0391
	hold↑ → CKN	0.0391	0.0391	0.0352	0.0391
	hold↓ → CKN	0.0156	0.0195	0.0117	0.0195
D	setup↑ → CKN	0.0039	-0.0039	-0.0078	-0.0078
	setup↓ → CKN	0.0430	0.0508	0.0469	0.0430
	hold↑ → CKN	0.0273	0.0352	0.0312	0.0352
	hold↓ → CKN	-0.0195	-0.0195	-0.0234	-0.0156
CKN	minpwl	0.1368	0.1368	0.1320	0.1368
	minpwh	0.0444	0.0395	0.0444	0.0395

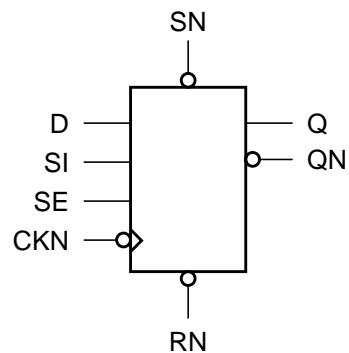
Cell Description

The SDFFNSRH cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN). This cell has a fast clock-to-Q path.

Functions

RN	SN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	1	x	0	—	1	0
1	1	0	x	0	—	0	1
1	1	x	x	x	—	Q[n]	QN[n]
1	1	x	1	1	—	1	0
1	1	x	0	1	—	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

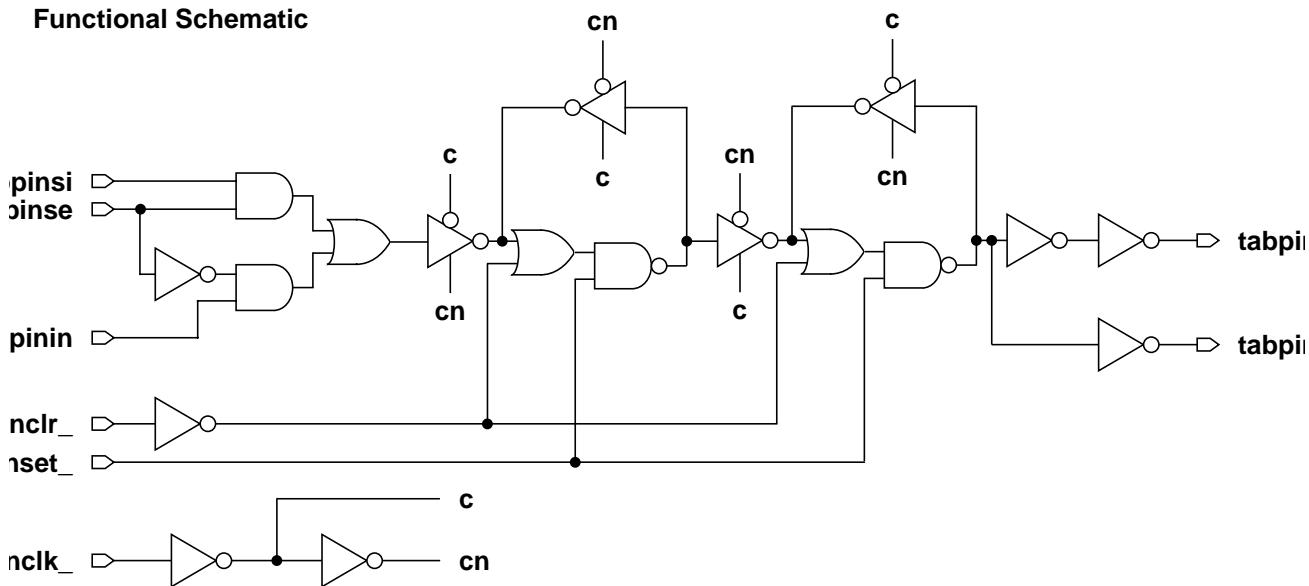
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNSRHX1	2.52	11.76
SDFFNSRHX2	2.52	12.04
SDFFNSRHX4	2.52	14.84
SDFFNSRHX8	2.52	15.68

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
SI	0.0087	0.0099	0.0153	0.0156
SE	0.0101	0.0111	0.0164	0.0167
D	0.0097	0.0109	0.0166	0.0169
CKN	0.0132	0.0144	0.0215	0.0218
SN	0.0042	0.0043	0.0054	0.0057
RN	0.0016	0.0017	0.0027	0.0029
Q	0.0070	0.0080	0.0121	0.0187

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0011	0.0011	0.0014	0.0015
SE	0.0024	0.0024	0.0027	0.0027
D	0.0013	0.0016	0.0021	0.0021
CKN	0.0021	0.0022	0.0026	0.0025
SN	0.0022	0.0023	0.0033	0.0033
RN	0.0018	0.0020	0.0030	0.0030

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CKN → Q↑	0.1688	0.1615	0.1638	0.1753	3.7153	2.6802	1.3541	0.6994
CKN → Q↓	0.1414	0.1272	0.1186	0.1323	3.3538	1.6771	0.8070	0.4149
SN → Q↑	0.1070	0.1157	0.1431	0.1632	3.6324	2.6644	1.3640	0.7041
SN → Q↓	0.1986	0.1850	0.1524	0.1862	3.8001	1.9347	0.9138	0.4779
RN → Q↓	0.1740	0.1597	0.1213	0.1549	3.8141	1.9427	0.9155	0.4788
CKN → QN↑	0.1726	0.1681	0.1588	0.1790	5.4095	10.9492	10.8204	11.0361
CKN → QN↓	0.2191	0.2076	0.2122	0.2290	4.4198	4.2773	4.2500	4.2698
SN → QN↑	0.2342	0.2356	0.2012	0.2473	5.4350	10.9600	10.8261	11.0382
SN → QN↓	0.1555	0.1615	0.1939	0.2210	4.4046	4.2730	4.2495	4.2696
RN → QN↑	0.2099	0.2109	0.1703	0.2163	5.4348	10.9565	10.8239	11.0375

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CKN	0.0117	0.0117	0.0117	0.0117
	setup↓ → CKN	0.0664	0.0859	0.0938	0.0977
	hold↑ → CKN	0.0391	0.0312	0.0273	0.0352
	hold↓ → CKN	-0.0352	-0.0469	-0.0586	-0.0586
SE	setup↑ → CKN	0.0938	0.1094	0.1211	0.1211
	setup↓ → CKN	0.0547	0.0586	0.0625	0.0625
	hold↑ → CKN	0.0352	0.0352	0.0273	0.0352
	hold↓ → CKN	0.0156	0.0156	0.0117	0.0156
D	setup↑ → CKN	0.0195	0.0117	0.0117	0.0117
	setup↓ → CKN	0.0586	0.0547	0.0586	0.0586
	hold↑ → CKN	0.0273	0.0312	0.0273	0.0352
	hold↓ → CKN	-0.0234	-0.0195	-0.0195	-0.0195
CKN	minpwl	0.1563	0.1466	0.1515	0.1612
	minpwh	0.0492	0.0492	0.0541	0.0541
SN	minpwl	0.0882	0.0979	0.1222	0.1417
	recovery	-0.0078	-0.0039	-0.0039	-0.0039
	removal	0.0273	0.0234	0.0234	0.0234
RN	minpwl	0.1709	0.1563	0.1174	0.1466
	recovery	-0.0938	-0.0898	-0.0898	-0.0938
	removal	0.1289	0.1328	0.1641	0.1641

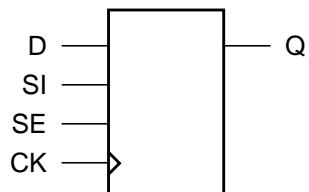
Cell Description

The SDFFQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q).

Functions

D	SI	SE	CK	Q[n+1]
1	x	0	/	1
0	x	0	/	0
x	x	x	\	Q[n]
x	1	1	/	1
x	0	1	/	0

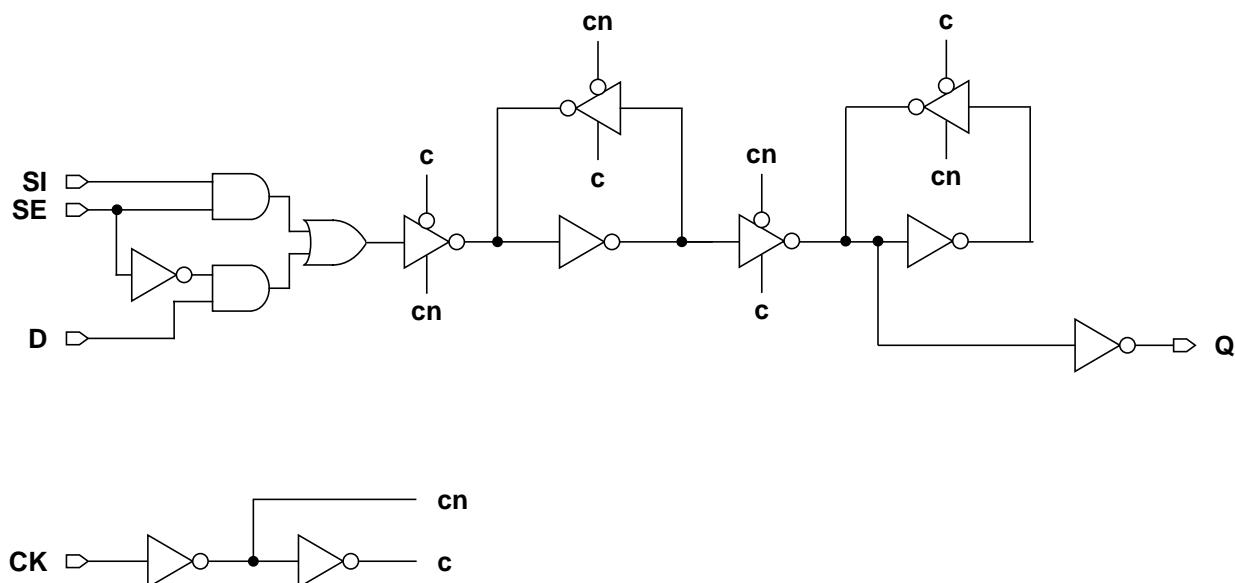
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFQXL	2.52	7.00
SDFFQX1	2.52	7.00
SDFFQX2	2.52	7.28
SDFFQX4	2.52	8.68

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
SI	0.0067	0.0068	0.0069	0.0070
SE	0.0079	0.0080	0.0080	0.0083
D	0.0058	0.0059	0.0060	0.0064
CK	0.0112	0.0114	0.0115	0.0124
Q	0.0042	0.0047	0.0059	0.0088

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0011	0.0011	0.0011	0.0010
SE	0.0029	0.0029	0.0029	0.0025
D	0.0015	0.0015	0.0015	0.0010
CK	0.0016	0.0016	0.0016	0.0017

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1055	0.1027	0.1023	0.1009	5.6654	3.5945	2.6262	1.3383
CK → Q↓	0.1250	0.1203	0.1224	0.1000	5.3321	3.4074	1.7480	0.8197

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.0781	0.0781	0.0781	0.0703
	setup↓ → CK	0.1953	0.1953	0.1953	0.2109
	hold↑ → CK	-0.0625	-0.0625	-0.0625	-0.0469
	hold↓ → CK	-0.1523	-0.1523	-0.1523	-0.1602
SE	setup↑ → CK	0.1953	0.1953	0.1953	0.2227
	setup↓ → CK	0.0898	0.0898	0.0898	0.1875
	hold↑ → CK	-0.0586	-0.0586	-0.0586	-0.0430
	hold↓ → CK	-0.0352	-0.0352	-0.0352	-0.0664
D	setup↑ → CK	0.0664	0.0664	0.0664	0.0625
	setup↓ → CK	0.0742	0.0742	0.0742	0.1914
	hold↑ → CK	-0.0508	-0.0508	-0.0508	-0.0391
	hold↓ → CK	-0.0352	-0.0352	-0.0352	-0.1445
CK	minpwh	0.0979	0.0930	0.0979	0.0736
	minpw1	0.0833	0.0833	0.0833	0.0882

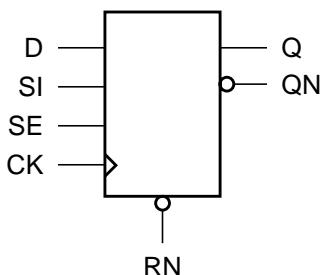
Cell Description

The SDFFR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Functions

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	/	1	0
1	0	x	0	/	0	1
1	x	x	x	/	Q[n]	QN[n]
1	x	1	1	/	1	0
1	x	0	1	/	0	1
0	x	x	x	x	0	1

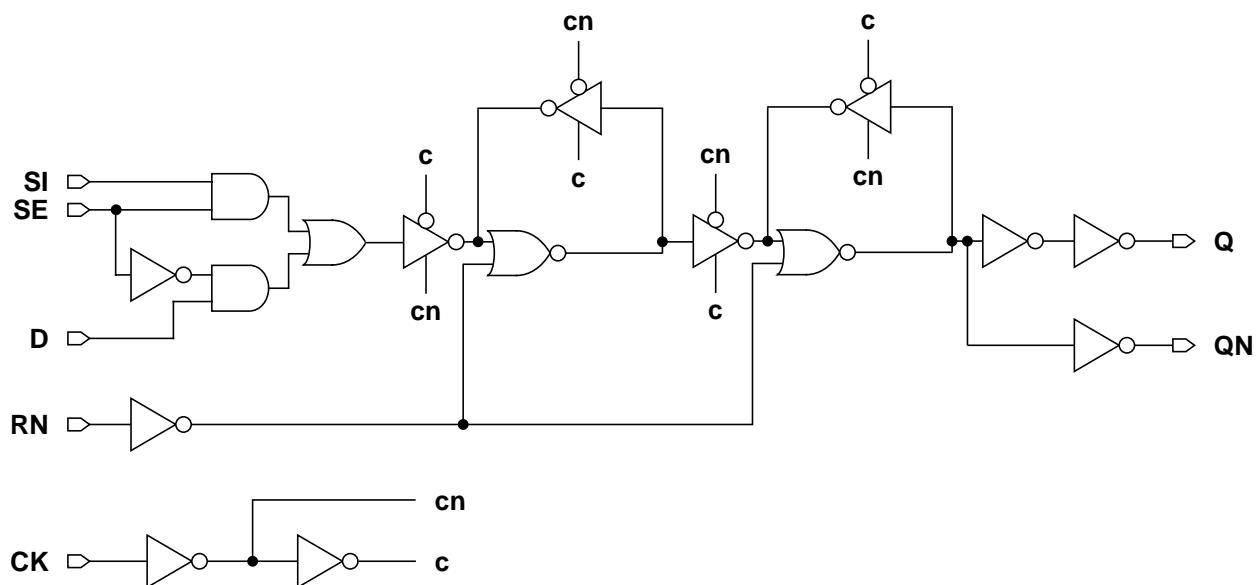
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRXL	2.52	8.12
SDFFRX1	2.52	8.40
SDFFRX2	2.52	8.40
SDFFRX4	2.52	8.96

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
SI	0.0066	0.0068	0.0067	0.0074
SE	0.0073	0.0075	0.0075	0.0081
D	0.0064	0.0066	0.0065	0.0072
CK	0.0095	0.0098	0.0097	0.0103
RN	0.0014	0.0013	0.0015	0.0021
Q	0.0051	0.0059	0.0079	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0009	0.0008	0.0008	0.0008
SE	0.0022	0.0022	0.0023	0.0022
D	0.0010	0.0010	0.0010	0.0010
CK	0.0017	0.0017	0.0016	0.0016
RN	0.0035	0.0037	0.0039	0.0044

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1303	0.1423	0.1489	0.1585	5.7367	3.6941	2.6740	1.3783
CK → Q↓	0.1440	0.1513	0.1522	0.1577	4.6792	3.1701	1.5707	0.7755
RN → Q↓	0.0710	0.0780	0.0637	0.0581	4.7108	3.1813	1.5788	0.7782
CK → QN↑	0.0913	0.0877	0.0985	0.1037	5.7587	3.6863	2.7028	1.4389
CK → QN↓	0.0887	0.0931	0.0997	0.1115	4.9688	3.3385	1.7478	0.9030
RN → QN↑	0.1205	0.1285	0.1251	0.1479	5.6775	3.6880	2.6698	1.4394

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.0820	0.0820	0.0781	0.0859
	setup↓ → CK	0.1289	0.1250	0.1289	0.1289
	hold↑ → CK	-0.0469	-0.0469	-0.0430	-0.0430
	hold↓ → CK	-0.0664	-0.0664	-0.0703	-0.0625
SE	setup↑ → CK	0.1367	0.1289	0.1328	0.1367
	setup↓ → CK	0.0938	0.0938	0.0938	0.0977
	hold↑ → CK	-0.0352	-0.0391	-0.0352	-0.0352
	hold↓ → CK	-0.0273	-0.0312	-0.0312	-0.0273
D	setup↑ → CK	0.0703	0.0742	0.0703	0.0781
	setup↓ → CK	0.0938	0.0938	0.0938	0.0977
	hold↑ → CK	-0.0391	-0.0430	-0.0391	-0.0391
	hold↓ → CK	-0.0430	-0.0469	-0.0469	-0.0391
CK	minpwh	0.0784	0.0882	0.0930	0.1028
	minpwl	0.0541	0.0590	0.0590	0.0590
RN	minpwl	0.0784	0.0833	0.0784	0.0882
	recovery	0.0781	0.0781	0.0781	0.0820
	removal	-0.0586	-0.0625	-0.0625	-0.0703

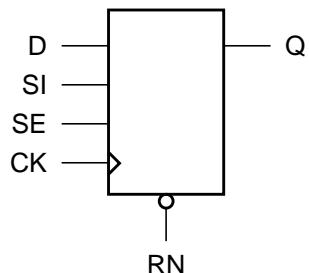
Cell Description

The SDFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Functions

RN	D	SI	SE	CK	Q[n+1]
1	1	x	0	/	1
1	0	x	0	/	0
1	x	x	x	\	Q[n]
1	x	1	1	/	1
1	x	0	1	/	0
0	x	x	x	x	0

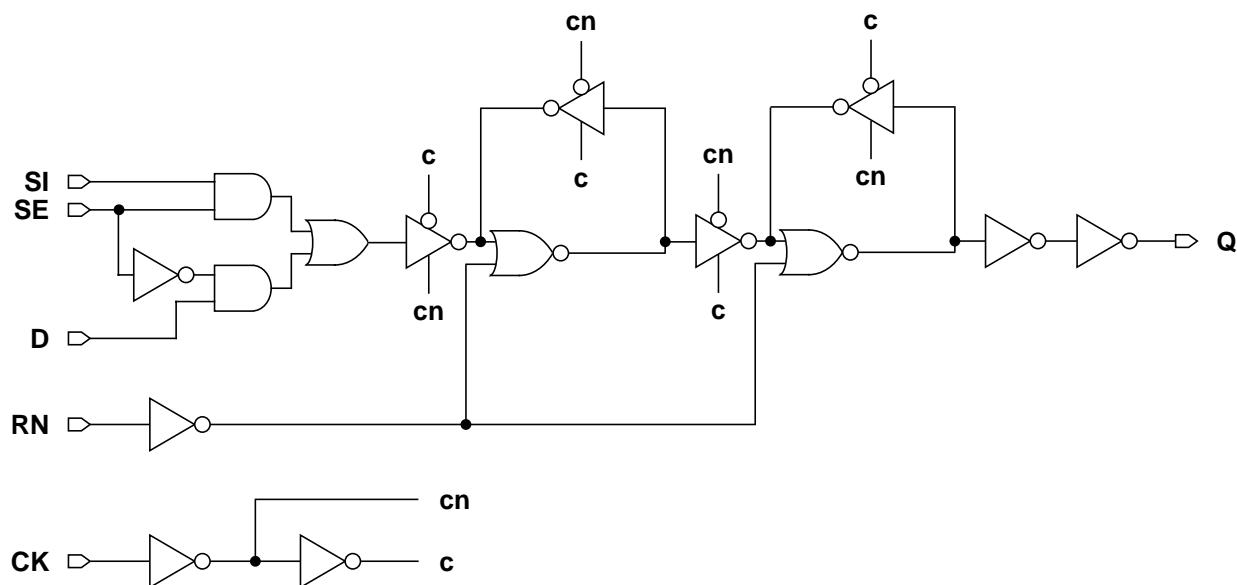
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRHQX1	2.52	9.52
SDFFRHQX2	2.52	9.52
SDFFRHQX4	2.52	11.20
SDFFRHQX8	2.52	12.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
SI	0.0085	0.0098	0.0149	0.0152
SE	0.0094	0.0107	0.0158	0.0160
D	0.0091	0.0103	0.0152	0.0155
CK	0.0149	0.0167	0.0252	0.0254
RN	0.0015	0.0017	0.0025	0.0026
Q	0.0042	0.0051	0.0081	0.0135

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0012	0.0012	0.0015	0.0015
SE	0.0026	0.0028	0.0034	0.0034
D	0.0017	0.0018	0.0022	0.0022
CK	0.0022	0.0022	0.0028	0.0028
RN	0.0019	0.0021	0.0033	0.0032

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0851	0.0844	0.0771	0.0867	3.6624	2.6375	1.3448	0.6978
CK → Q↓	0.0848	0.0812	0.0772	0.0874	3.2237	1.6018	0.7883	0.4006
RN → Q↓	0.0917	0.0902	0.0728	0.0940	3.2574	1.6655	0.8110	0.4157

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.0820	0.0742	0.0781	0.0781
	setup↓ → CK	0.1133	0.1133	0.1211	0.1172
	hold↑ → CK	-0.0312	-0.0312	-0.0352	-0.0312
	hold↓ → CK	-0.0742	-0.0781	-0.0820	-0.0820
SE	setup↑ → CK	0.1250	0.1250	0.1367	0.1367
	setup↓ → CK	0.0977	0.0781	0.0820	0.0820
	hold↑ → CK	-0.0234	-0.0234	-0.0273	-0.0273
	hold↓ → CK	-0.0312	-0.0234	-0.0273	-0.0234
D	setup↑ → CK	0.0859	0.0625	0.0586	0.0586
	setup↓ → CK	0.0703	0.0586	0.0586	0.0586
	hold↑ → CK	-0.0352	-0.0234	-0.0195	-0.0195
	hold↓ → CK	-0.0312	-0.0273	-0.0312	-0.0273
CK	minpwh	0.0492	0.0492	0.0492	0.0492
	minpwl	0.1174	0.1028	0.0930	0.0930
RN	minpwl	0.0833	0.0833	0.0687	0.0930
	recovery	-0.0156	-0.0195	-0.0195	-0.0234
	removal	0.0391	0.0469	0.0625	0.0586

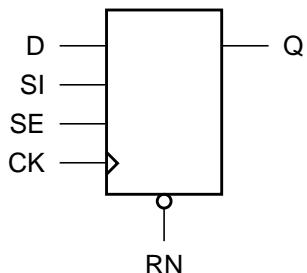
Cell Description

The SDFFRQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q).

Functions

RN	D	SI	SE	CK	$Q[n+1]$
1	1	x	0	/\	1
1	0	x	0	/\	0
1	x	x	x	_	$Q[n]$
1	x	1	1	/\	1
1	x	0	1	/\	0
0	x	x	x	x	0

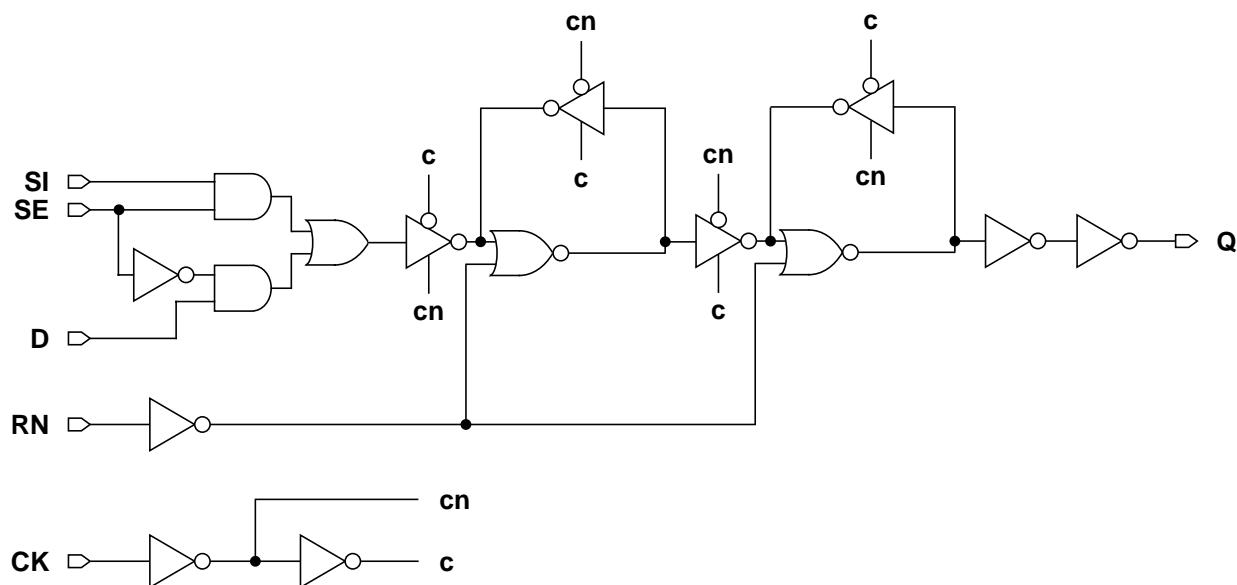
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRQXL	2.52	7.84
SDFFRQX1	2.52	7.84
SDFFRQX2	2.52	7.84
SDFFRQX4	2.52	8.40

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
SI	0.0066	0.0066	0.0066	0.0067
SE	0.0073	0.0073	0.0073	0.0075
D	0.0064	0.0064	0.0064	0.0065
CK	0.0094	0.0094	0.0094	0.0097
RN	0.0012	0.0012	0.0013	0.0015
Q	0.0036	0.0041	0.0051	0.0084

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0008	0.0008	0.0008	0.0008
SE	0.0022	0.0022	0.0022	0.0022
D	0.0010	0.0010	0.0009	0.0010
CK	0.0016	0.0016	0.0016	0.0016
RN	0.0035	0.0035	0.0035	0.0039

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1114	0.1141	0.1168	0.1155	5.6767	3.6244	2.6355	1.3502
CK → Q↓	0.1342	0.1419	0.1485	0.1550	4.4293	3.2581	1.6647	0.8229
RN → Q↓	0.0676	0.0758	0.0824	0.0838	4.4804	3.2493	1.6480	0.8085

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.0859	0.0859	0.0820	0.0820
	setup↓ → CK	0.1289	0.1250	0.1250	0.1250
	hold↑ → CK	-0.0469	-0.0469	-0.0469	-0.0469
	hold↓ → CK	-0.0664	-0.0664	-0.0703	-0.0625
SE	setup↑ → CK	0.1328	0.1328	0.1289	0.1289
	setup↓ → CK	0.0938	0.0938	0.0977	0.0977
	hold↑ → CK	-0.0391	-0.0391	-0.0391	-0.0391
	hold↓ → CK	-0.0312	-0.0312	-0.0312	-0.0273
D	setup↑ → CK	0.0742	0.0742	0.0742	0.0742
	setup↓ → CK	0.0938	0.0938	0.0938	0.0898
	hold↑ → CK	-0.0430	-0.0430	-0.0430	-0.0430
	hold↓ → CK	-0.0469	-0.0469	-0.0469	-0.0430
CK	minpwh	0.0638	0.0638	0.0687	0.0687
	minpwl	0.0541	0.0541	0.0541	0.0590
RN	minpwl	0.0687	0.0736	0.0833	0.0882
	recovery	0.0781	0.0781	0.0820	0.0820
	removal	-0.0586	-0.0586	-0.0625	-0.0625

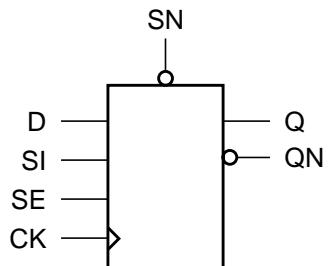
Cell Description

The SDFFS cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Functions

SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	↑	1	0
1	0	x	0	↑	0	1
1	x	x	x	↖	Q[n]	QN[n]
1	x	1	1	↑	1	0
1	x	0	1	↑	0	1
0	x	x	x	x	1	0

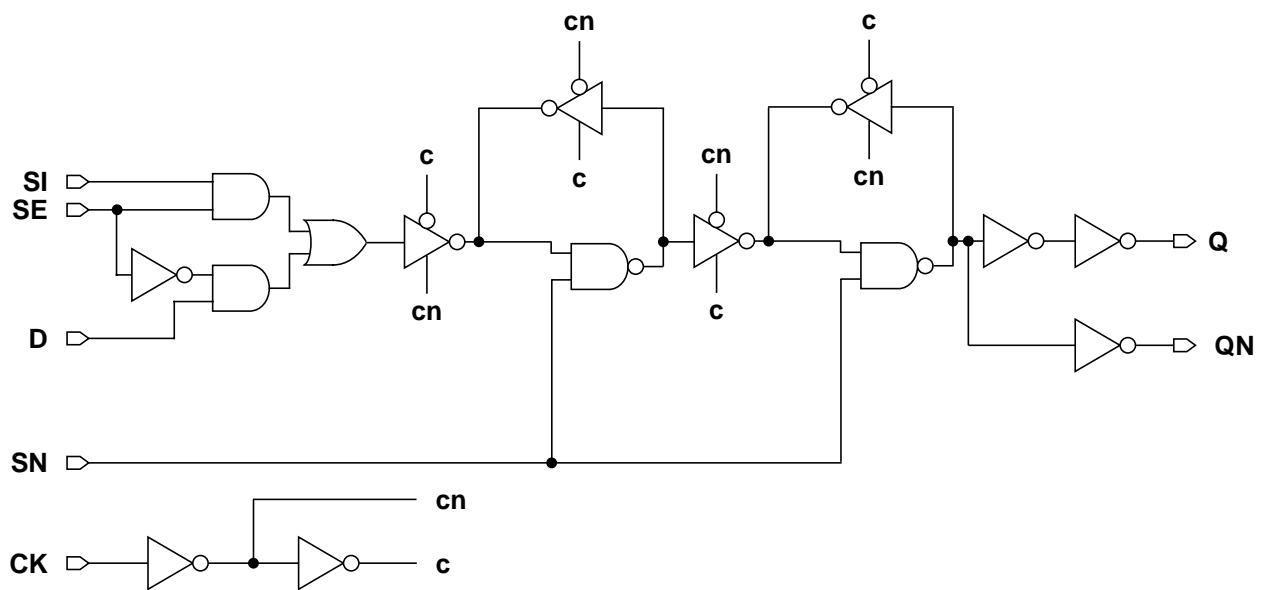
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSXL	2.52	7.56
SDFFSX1	2.52	7.56
SDFFSX2	2.52	7.56
SDFFSX4	2.52	8.68

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
SI	0.0069	0.0069	0.0075	0.0097
SE	0.0076	0.0076	0.0082	0.0103
D	0.0064	0.0064	0.0069	0.0091
CK	0.0105	0.0105	0.0109	0.0130
SN	0.0011	0.0011	0.0012	0.0015
Q	0.0055	0.0064	0.0081	0.0138

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0014	0.0014	0.0014	0.0015
SE	0.0023	0.0023	0.0022	0.0022
D	0.0011	0.0011	0.0011	0.0011
CK	0.0018	0.0018	0.0017	0.0018
SN	0.0020	0.0020	0.0021	0.0026

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1399	0.1477	0.1505	0.1574	5.6321	3.7458	2.6552	1.3728
CK → Q↓	0.1393	0.1480	0.1462	0.1677	4.1714	3.0878	1.5780	0.8184
SN → Q↑	0.1112	0.1173	0.1344	0.1912	5.6034	3.7301	2.6517	1.3728
CK → QN↑	0.0976	0.0989	0.0933	0.0898	5.8930	3.8811	2.6859	1.3989
CK → QN↓	0.1020	0.1105	0.1021	0.0946	5.2545	3.7030	1.8376	0.8662
SN → QN↓	0.0768	0.0830	0.0878	0.1172	4.5652	3.2882	1.7078	0.9189

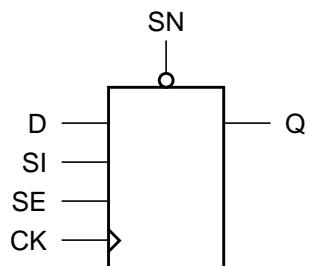
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.0898	0.0898	0.0859	0.0898
	setup↓ → CK	0.1289	0.1250	0.1289	0.1484
	hold↑ → CK	-0.0469	-0.0508	-0.0508	-0.0547
	hold↓ → CK	-0.0703	-0.0703	-0.0742	-0.0859
SE	setup↑ → CK	0.1406	0.1406	0.1406	0.1562
	setup↓ → CK	0.1172	0.1172	0.1133	0.1172
	hold↑ → CK	-0.0391	-0.0391	-0.0391	-0.0430
	hold↓ → CK	-0.0312	-0.0312	-0.0469	-0.0586
D	setup↑ → CK	0.0898	0.0898	0.0859	0.0898
	setup↓ → CK	0.0977	0.0977	0.1211	0.1406
	hold↑ → CK	-0.0508	-0.0508	-0.0508	-0.0547
	hold↓ → CK	-0.0508	-0.0508	-0.0664	-0.0781
CK	minpwh	0.0930	0.1028	0.0979	0.1028
	minpwl	0.0590	0.0590	0.0638	0.0687
SN	minpwl	0.0784	0.0833	0.0979	0.1417
	recovery	-0.0234	-0.0273	-0.0273	-0.0273
	removal	0.0430	0.0430	0.0430	0.0469

Cell Description

The SDFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



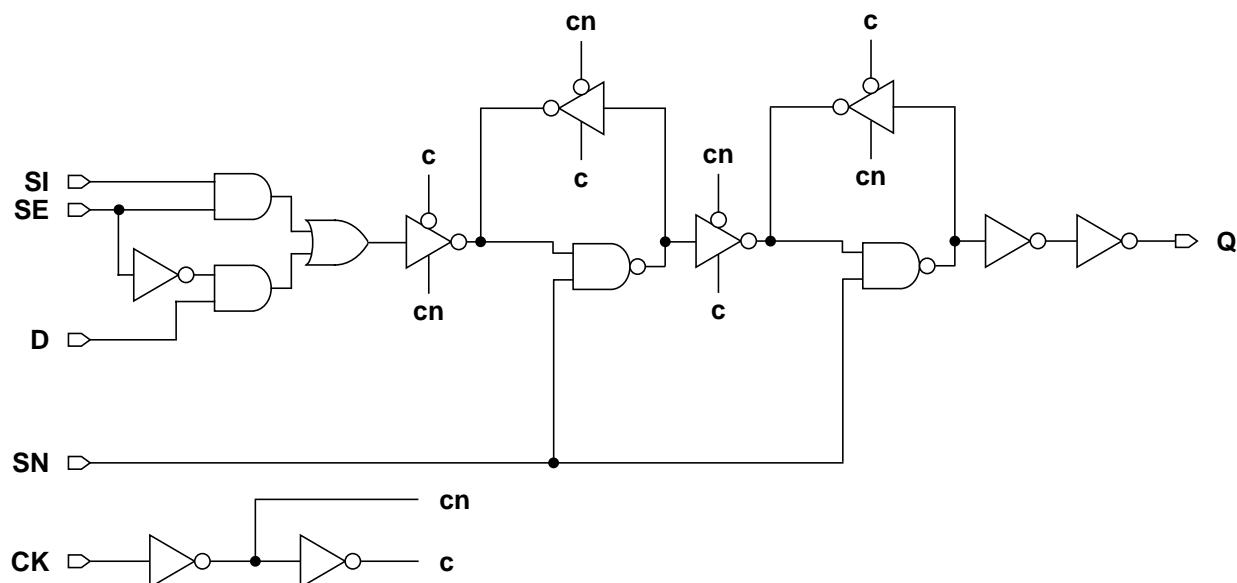
Functions

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	/\	1
1	0	x	0	/\	0
1	x	x	x	_	Q[n]
1	x	1	1	/\	1
1	x	0	1	/\	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSHQX1	2.52	9.52
SDFFSHQX2	2.52	9.52
SDFFSHQX4	2.52	11.48
SDFFSHQX8	2.52	12.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
SI	0.0080	0.0084	0.0114	0.0117
SE	0.0091	0.0096	0.0125	0.0128
D	0.0082	0.0088	0.0124	0.0127
CK	0.0142	0.0148	0.0200	0.0204
SN	0.0035	0.0037	0.0043	0.0046
Q	0.0045	0.0056	0.0085	0.0142

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0012	0.0012	0.0012	0.0012
SE	0.0026	0.0027	0.0032	0.0031
D	0.0013	0.0016	0.0022	0.0022
CK	0.0021	0.0021	0.0027	0.0026
SN	0.0023	0.0025	0.0025	0.0025

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0781	0.0828	0.0743	0.0840	3.6262	2.6645	1.3672	0.6985
CK → Q↓	0.0848	0.0873	0.0734	0.0851	3.1857	1.6384	0.7885	0.4034
SN → Q↑	0.0814	0.0930	0.1009	0.1179	3.6133	2.6544	1.3672	0.6975

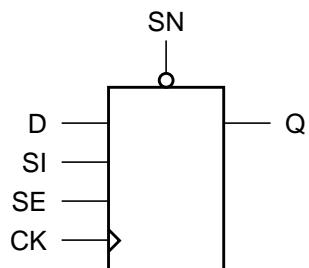
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.0820	0.0820	0.0859	0.0898
	setup↓ → CK	0.1094	0.1094	0.1367	0.1367
	hold↑ → CK	-0.0391	-0.0391	-0.0391	-0.0352
	hold↓ → CK	-0.0742	-0.0742	-0.0898	-0.0898
SE	setup↑ → CK	0.1211	0.1250	0.1562	0.1562
	setup↓ → CK	0.0938	0.0859	0.0859	0.0859
	hold↑ → CK	-0.0312	-0.0312	-0.0312	-0.0273
	hold↓ → CK	-0.0352	-0.0234	-0.0234	-0.0234
D	setup↑ → CK	0.0781	0.0703	0.0664	0.0703
	setup↓ → CK	0.0820	0.0664	0.0703	0.0703
	hold↑ → CK	-0.0391	-0.0312	-0.0195	-0.0195
	hold↓ → CK	-0.0469	-0.0352	-0.0312	-0.0312
CK	minpwh	0.0492	0.0492	0.0395	0.0444
	minpwl	0.1174	0.1174	0.1076	0.1125
SN	minpwl	0.0638	0.0784	0.0882	0.1028
	recovery	0.0234	0.0234	0.0352	0.0352
	removal	-0.0117	-0.0078	-0.0195	-0.0195

Cell Description

The SDFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol



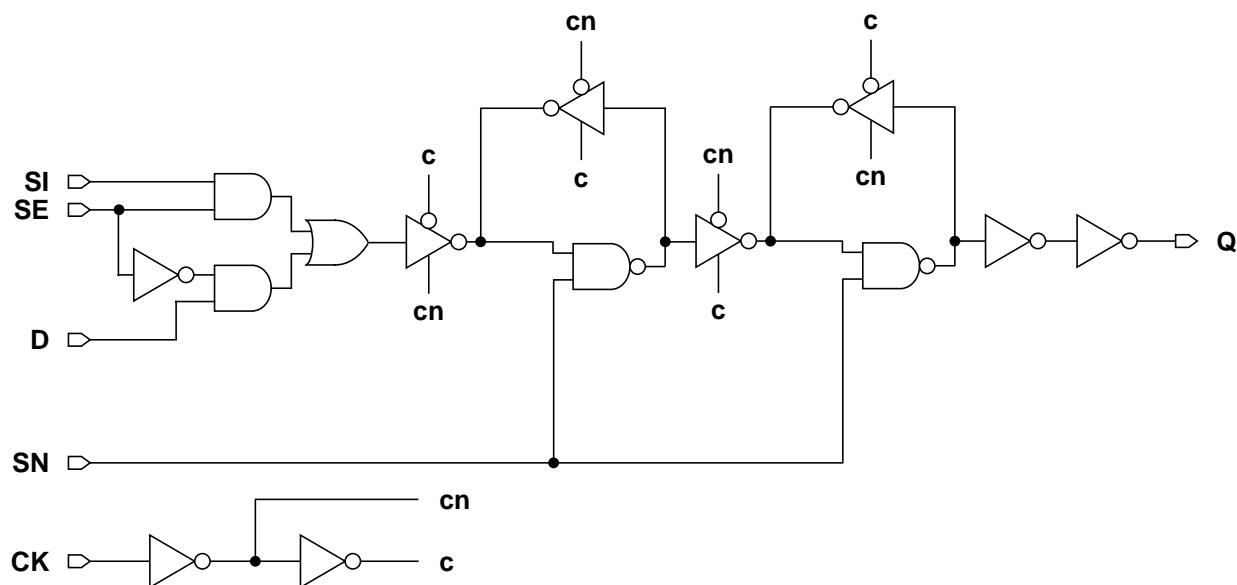
Functions

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	/\	1
1	0	x	0	/\	0
1	x	x	x	\/\	Q[n]
1	x	1	1	/\	1
1	x	0	1	/\	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSQXL	2.52	7.00
SDFFSQX1	2.52	7.28
SDFFSQX2	2.52	7.28
SDFFSQX4	2.52	7.56

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
SI	0.0070	0.0071	0.0074	0.0076
SE	0.0077	0.0078	0.0081	0.0082
D	0.0066	0.0066	0.0069	0.0070
CK	0.0103	0.0104	0.0108	0.0109
SN	0.0010	0.0011	0.0011	0.0013
Q	0.0041	0.0047	0.0056	0.0086

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0015	0.0015	0.0015	0.0015
SE	0.0023	0.0023	0.0023	0.0023
D	0.0012	0.0012	0.0012	0.0012
CK	0.0018	0.0018	0.0018	0.0018
SN	0.0019	0.0019	0.0021	0.0021

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1158	0.1188	0.1198	0.1293	5.4354	3.6028	2.6366	1.3466
CK → Q↓	0.1259	0.1334	0.1304	0.1478	4.5303	3.1402	1.5945	0.8201
SN → Q↑	0.0959	0.1007	0.1088	0.1173	5.4187	3.5941	2.6345	1.3451

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1016	0.1016	0.1094	0.1094
	setup↓ → CK	0.1328	0.1328	0.1250	0.1250
	hold↑ → CK	-0.0508	-0.0508	-0.0547	-0.0547
	hold↓ → CK	-0.0703	-0.0742	-0.0703	-0.0664
SE	setup↑ → CK	0.1445	0.1445	0.1367	0.1367
	setup↓ → CK	0.1289	0.1289	0.1367	0.1367
	hold↑ → CK	-0.0391	-0.0430	-0.0469	-0.0430
	hold↓ → CK	-0.0312	-0.0352	-0.0312	-0.0312
D	setup↑ → CK	0.1016	0.1016	0.1094	0.1094
	setup↓ → CK	0.1016	0.1016	0.0977	0.0977
	hold↑ → CK	-0.0508	-0.0547	-0.0547	-0.0547
	hold↓ → CK	-0.0508	-0.0508	-0.0508	-0.0469
CK	minpwh	0.0736	0.0784	0.0736	0.0833
	minpwl	0.0638	0.0638	0.0687	0.0687
SN	minpwl	0.0687	0.0687	0.0736	0.0784
	recovery	-0.0234	-0.0195	-0.0273	-0.0273
	removal	0.0430	0.0391	0.0430	0.0430

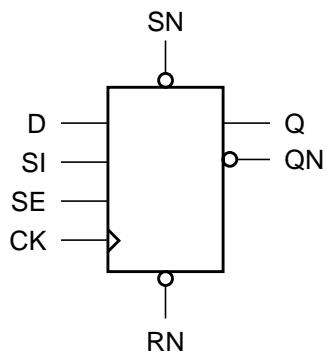
Cell Description

The SDFFSR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Functions

RN	SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	1	x	0	/\	1	0
1	1	0	x	0	/\	0	1
1	1	x	x	x	_	Q[n]	QN[n]
1	1	x	1	1	/\	1	0
1	1	x	0	1	/\	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

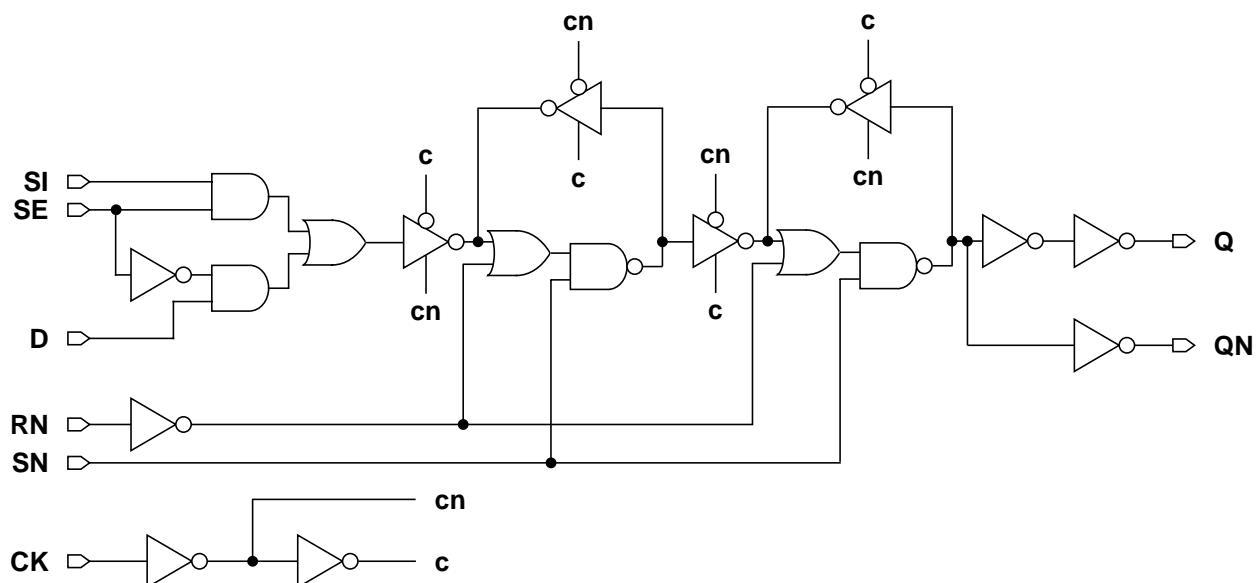
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSRXL	2.52	9.24
SDFFSRX1	2.52	9.52
SDFFSRX2	2.52	9.80
SDFFSRX4	2.52	11.76

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
SI	0.0077	0.0077	0.0083	0.0123
SE	0.0084	0.0084	0.0089	0.0126
D	0.0073	0.0073	0.0078	0.0115
CK	0.0112	0.0113	0.0119	0.0170
SN	0.0012	0.0013	0.0014	0.0018
RN	0.0027	0.0027	0.0030	0.0033
Q	0.0061	0.0072	0.0088	0.0140

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0013	0.0013	0.0013	0.0013
SE	0.0022	0.0022	0.0022	0.0022
D	0.0012	0.0012	0.0013	0.0013
CK	0.0016	0.0016	0.0017	0.0020
SN	0.0020	0.0020	0.0022	0.0029
RN	0.0011	0.0011	0.0011	0.0011

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1493	0.1567	0.1552	0.1581	5.6753	3.6599	2.6561	1.3725
CK → Q↓	0.1525	0.1606	0.1604	0.1684	4.2125	3.0991	1.5887	0.8081
SN → Q↑	0.1242	0.1298	0.1486	0.2054	5.6245	3.6318	2.6515	1.3721
SN → Q↓	0.1196	0.1269	0.1377	0.1607	4.1853	3.0873	1.5847	0.8080
RN → Q↓	0.1386	0.1459	0.1657	0.2043	4.1756	3.0835	1.5835	0.8081
CK → QN↑	0.1073	0.1083	0.1016	0.0952	6.1146	3.8969	2.7143	1.4025
CK → QN↓	0.1113	0.1205	0.1086	0.0966	5.7478	3.9658	1.8918	0.8915
SN → QN↑	0.0748	0.0755	0.0774	0.0818	5.9483	3.7983	2.6996	1.4182
SN → QN↓	0.0901	0.0966	0.1026	0.1323	4.7707	3.3728	1.7596	0.9333
RN → QN↑	0.0945	0.0953	0.1057	0.1251	5.8896	3.7720	2.6925	1.4172

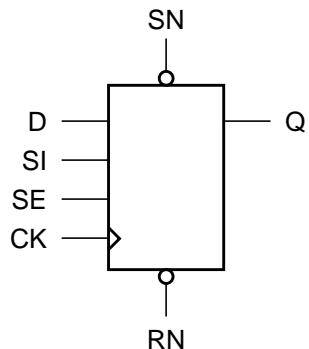
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1172	0.1133	0.0977	0.1172
	setup↓ → CK	0.1406	0.1406	0.1484	0.1680
	hold↑ → CK	-0.0508	-0.0508	-0.0508	-0.0586
	hold↓ → CK	-0.0781	-0.0781	-0.0820	-0.0898
SE	setup↑ → CK	0.1523	0.1523	0.1602	0.1797
	setup↓ → CK	0.1445	0.1406	0.1250	0.1289
	hold↑ → CK	-0.0430	-0.0430	-0.0391	-0.0508
	hold↓ → CK	-0.0391	-0.0391	-0.0430	-0.0469
D	setup↑ → CK	0.1172	0.1172	0.1016	0.1055
	setup↓ → CK	0.1133	0.1133	0.1172	0.1328
	hold↑ → CK	-0.0547	-0.0547	-0.0508	-0.0547
	hold↓ → CK	-0.0586	-0.0586	-0.0625	-0.0664
CK	minpwh	0.1028	0.1076	0.1028	0.1028
	minpwl	0.0736	0.0736	0.0687	0.0687
SN	minpwl	0.0930	0.0930	0.1076	0.1563
	recovery	-0.0195	-0.0195	-0.0234	-0.0312
	removal	0.0391	0.0391	0.0430	0.0547
RN	minpwl	0.0833	0.0882	0.0979	0.1271
	recovery	0.0703	0.0664	0.0469	0.0508
	removal	-0.0234	-0.0234	-0.0156	-0.0156

Cell Description

The SDFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



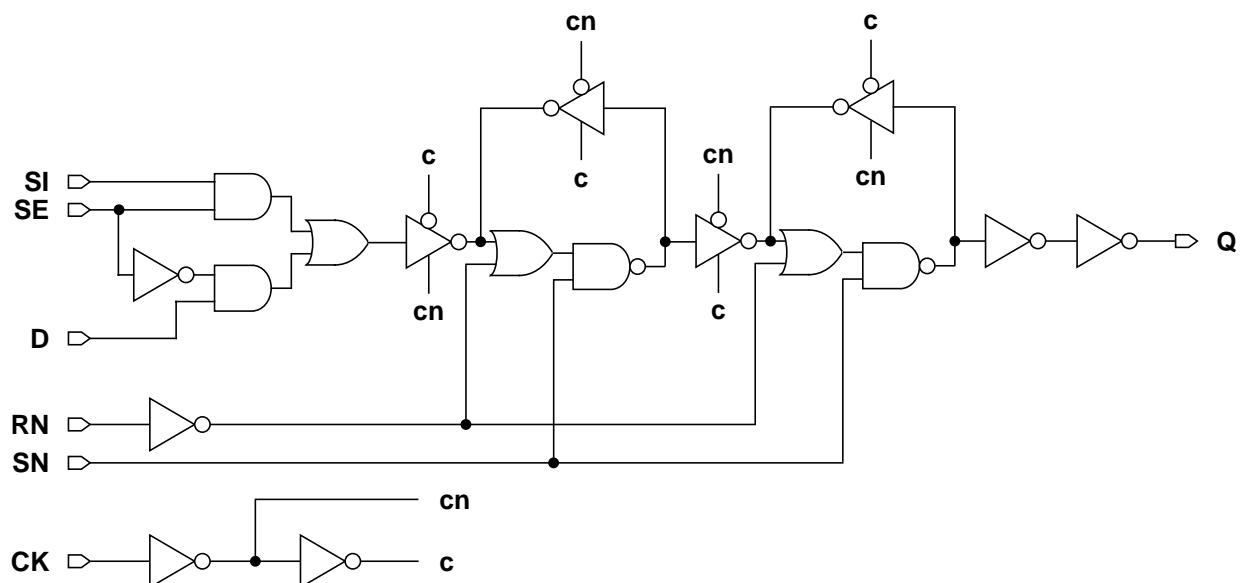
Functions

RN	SN	D	SI	SE	CK	Q[n+1]
1	1	1	x	0	/	1
1	1	0	x	0	/	0
1	1	x	x	x	/	Q[n]
1	1	x	1	1	/	1
1	1	x	0	1	/	0
0	1	x	x	x	x	0
1	0	x	x	x	x	1
0	0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSRHQX1	2.52	11.48
SDFFSRHQX2	2.52	11.48
SDFFSRHQX4	2.52	13.72
SDFFSRHQX8	2.52	14.56

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
SI	0.0086	0.0098	0.0140	0.0143
SE	0.0097	0.0108	0.0148	0.0151
D	0.0087	0.0100	0.0144	0.0147
CK	0.0151	0.0167	0.0230	0.0233
SN	0.0042	0.0044	0.0055	0.0058
RN	0.0015	0.0017	0.0025	0.0026
Q	0.0055	0.0064	0.0095	0.0154

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0013	0.0013	0.0015	0.0015
SE	0.0027	0.0027	0.0030	0.0030
D	0.0012	0.0015	0.0021	0.0021
CK	0.0022	0.0022	0.0026	0.0026
SN	0.0022	0.0024	0.0032	0.0032
RN	0.0016	0.0018	0.0031	0.0031

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0946	0.0904	0.0867	0.0983	3.7474	2.6716	1.3584	0.7043
CK → Q↓	0.0997	0.0901	0.0882	0.0987	3.4131	1.6754	0.8205	0.4207
SN → Q↑	0.1044	0.1126	0.1428	0.1643	3.6377	2.6455	1.3576	0.7019
SN → Q↓	0.2056	0.1782	0.1522	0.1881	3.6660	1.8699	0.8974	0.4687
RN → Q↓	0.1806	0.1533	0.1199	0.1553	3.6744	1.8750	0.8988	0.4692

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.0977	0.0859	0.0977	0.0977
	setup↓ → CK	0.1172	0.1133	0.1016	0.1055
	hold↑ → CK	-0.0430	-0.0391	-0.0469	-0.0430
	hold↓ → CK	-0.0742	-0.0742	-0.0625	-0.0586
SE	setup↑ → CK	0.1289	0.1250	0.1172	0.1172
	setup↓ → CK	0.1133	0.1016	0.1172	0.1172
	hold↑ → CK	-0.0312	-0.0312	-0.0391	-0.0352
	hold↓ → CK	-0.0391	-0.0352	-0.0273	-0.0234
D	setup↑ → CK	0.0977	0.0781	0.0898	0.0898
	setup↓ → CK	0.0938	0.0742	0.0586	0.0586
	hold↑ → CK	-0.0430	-0.0312	-0.0391	-0.0391
	hold↓ → CK	-0.0508	-0.0391	-0.0234	-0.0195
CK	minpwh	0.0492	0.0492	0.0541	0.0541
	minpwl	0.1271	0.1174	0.1174	0.1174
SN	minpwl	0.0882	0.0979	0.1222	0.1417
	recovery	0.0312	0.0234	0.0195	0.0195
	removal	-0.0156	-0.0078	-0.0078	-0.0078
RN	minpwl	0.1661	0.1417	0.1125	0.1466
	recovery	-0.0156	-0.0195	-0.0156	-0.0156
	removal	0.0391	0.0430	0.0508	0.0469

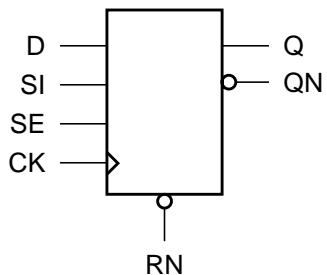
Cell Description

The SDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-low reset (RN). Scan enable (SE) dominates reset (RN).

Functions

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	0	1	/	0	1
x	x	1	1	/	1	0
0	x	x	0	/	0	1
1	0	x	0	/	0	1
1	1	x	0	/	1	0
x	x	x	x	\	Q[n]	QN[n]

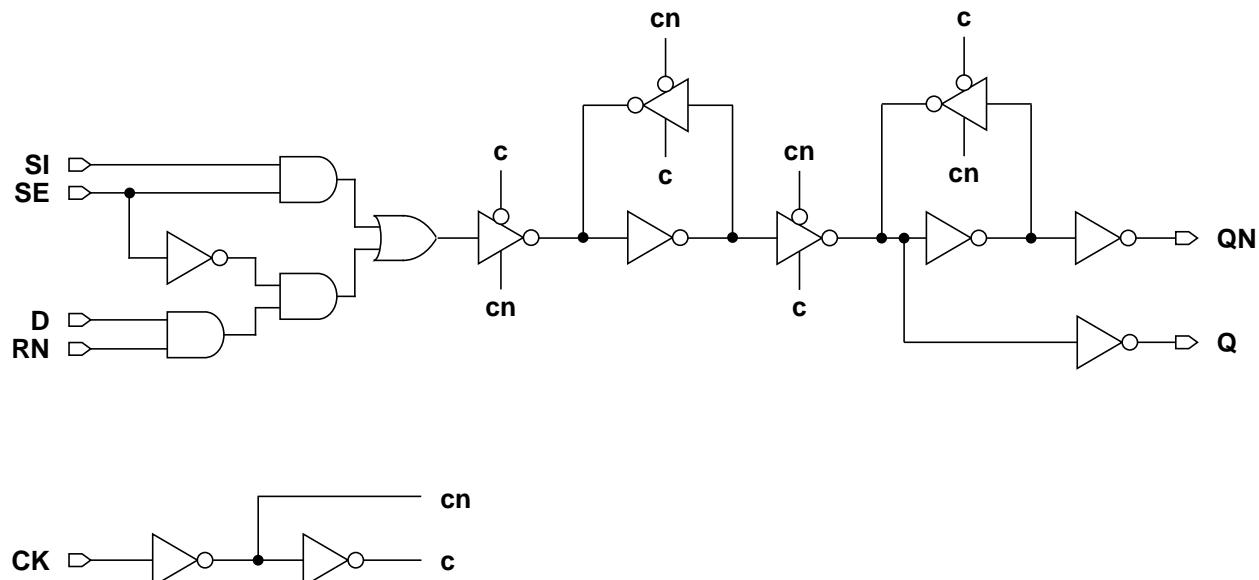
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SDFFTRXL	2.52	7.84
SDFFTRX1	2.52	8.12
SDFFTRX2	2.52	8.12
SDFFTRX4	2.52	9.80

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
SI	0.0070	0.0077	0.0086	0.0141
SE	0.0083	0.0089	0.0096	0.0137
D	0.0067	0.0073	0.0081	0.0123
CK	0.0098	0.0104	0.0112	0.0167
RN	0.0076	0.0083	0.0093	0.0157
Q	0.0054	0.0062	0.0078	0.0128

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0011	0.0011	0.0011	0.0011
SE	0.0035	0.0035	0.0035	0.0038
D	0.0010	0.0010	0.0010	0.0013
CK	0.0017	0.0017	0.0017	0.0020
RN	0.0018	0.0018	0.0018	0.0020

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1195	0.1144	0.1195	0.1185	5.6157	3.6174	2.6528	1.3633
CK → Q↓	0.1320	0.1347	0.1368	0.1355	4.1650	3.0769	1.5658	0.7710
CK → QN↑	0.0906	0.0867	0.0863	0.0864	5.7558	3.6565	2.6489	1.3707
CK → QN↓	0.0872	0.0844	0.0812	0.0777	4.9788	3.2315	1.6154	0.7902

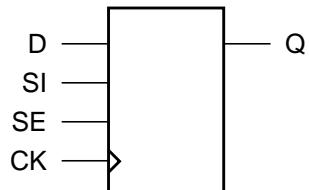
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.0781	0.0781	0.0820	0.1094
	setup↓ → CK	0.1406	0.1406	0.1445	0.1836
	hold↑ → CK	-0.0430	-0.0430	-0.0508	-0.0625
	hold↓ → CK	-0.0781	-0.0781	-0.0820	-0.0977
SE	setup↑ → CK	0.1445	0.1484	0.1523	0.1953
	setup↓ → CK	0.1094	0.1094	0.1133	0.1133
	hold↑ → CK	-0.0391	-0.0391	-0.0430	-0.0586
	hold↓ → CK	-0.0391	-0.0430	-0.0469	-0.0312
D	setup↑ → CK	0.0859	0.0898	0.0938	0.0898
	setup↓ → CK	0.1055	0.1094	0.1094	0.0938
	hold↑ → CK	-0.0508	-0.0508	-0.0547	-0.0508
	hold↓ → CK	-0.0547	-0.0547	-0.0586	-0.0469
CK	minpwh	0.0736	0.0687	0.0736	0.0687
	minpwl	0.0541	0.0541	0.0590	0.0541
RN	setup↑ → CK	0.0898	0.0938	0.0938	0.0938
	setup↓ → CK	0.1523	0.1562	0.1562	0.2109
	hold↑ → CK	-0.0508	-0.0547	-0.0586	-0.0547
	hold↓ → CK	-0.0820	-0.0820	-0.0859	-0.1094

Cell Description

The SDFFYQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and overdriven feedback loops to increase MTBF due to metastability.

Logic Symbol



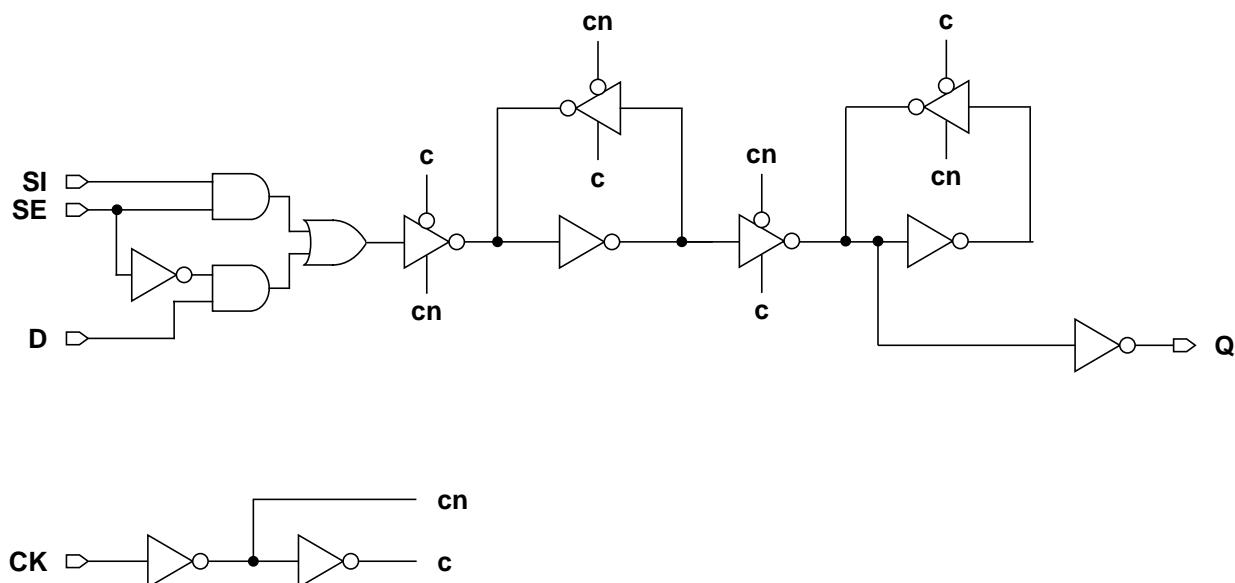
Functions

D	SI	SE	CK	Q[n+1]
1	x	0	—	1
0	x	0	—	0
x	x	x	—	Q[n]
x	1	1	—	1
x	0	1	—	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFYQX2	2.52	8.12

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)
	X2
SI	0.0121
SE	0.0134
D	0.0096
CK	0.0175
Q	0.0053

Pin Capacitance

Pin	Capacitance (pF)
	X2
SI	0.0012
SE	0.0047
D	0.0021
CK	0.0021

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	X2
CK → Q↑	0.1001	2.6112
CK → Q↓	0.1010	1.6929

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)
		X2
SI	setup↑ → CK	0.0938
	setup↓ → CK	0.2695
	hold↑ → CK	-0.0742
	hold↓ → CK	-0.2305
SE	setup↑ → CK	0.2734
	setup↓ → CK	0.0781
	hold↑ → CK	-0.0781
	hold↓ → CK	-0.0391
D	setup↑ → CK	0.0430
	setup↓ → CK	0.0781
	hold↑ → CK	-0.0352
	hold↓ → CK	-0.0391
CK	minpwh	0.0784
	minpw1	0.0638

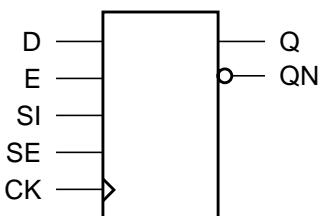
Cell Description

The SEDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E).

Functions

D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	1	1	/\	1	0
x	x	0	1	/\	0	1
x	0	x	0	/\	Q[n]	QN[n]
0	1	x	0	/\	0	1
1	1	x	0	/\	1	0
x	x	x	x	\/\	Q[n]	QN[n]

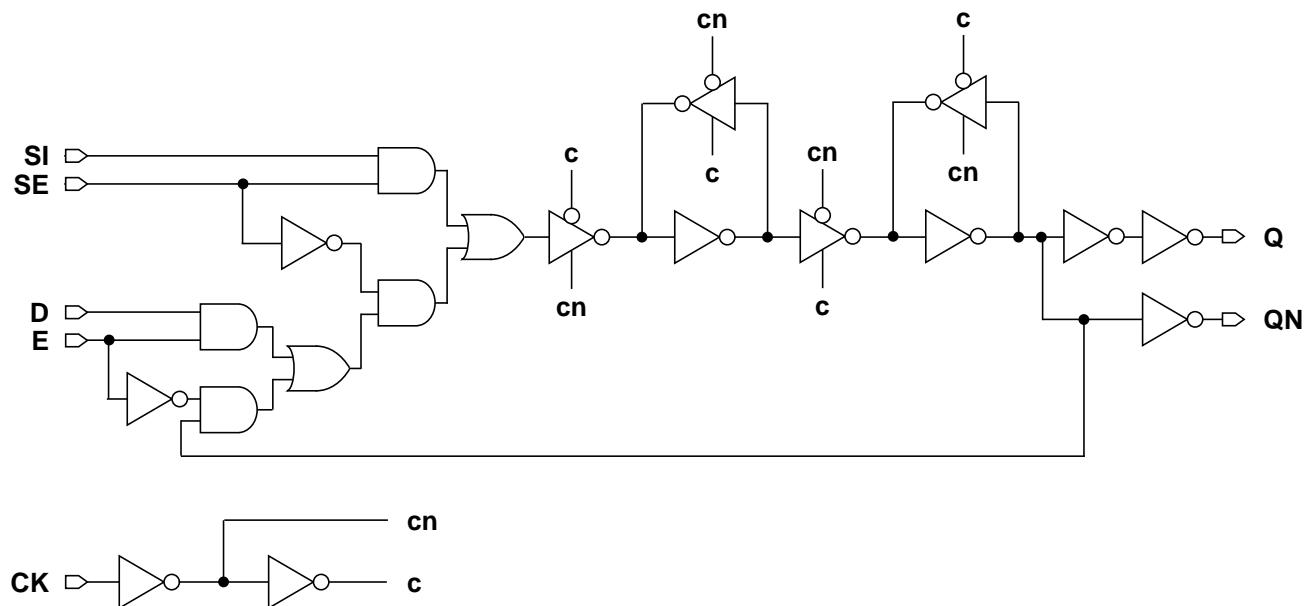
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFXL	2.52	8.68
SEDFFX1	2.52	8.96
SEDFFX2	2.52	8.96
SEDFFX4	2.52	11.20

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
SI	0.0073	0.0074	0.0076	0.0095
SE	0.0091	0.0092	0.0094	0.0112
D	0.0062	0.0063	0.0065	0.0083
CK	0.0106	0.0108	0.0110	0.0146
E	0.0083	0.0085	0.0087	0.0107
Q	0.0064	0.0071	0.0089	0.0149

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0010	0.0010	0.0010	0.0010
SE	0.0021	0.0022	0.0021	0.0021
D	0.0010	0.0010	0.0010	0.0010
CK	0.0015	0.0015	0.0015	0.0016
E	0.0024	0.0024	0.0025	0.0024

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1026	0.0953	0.0947	0.1077	5.7869	3.5602	2.6002	1.3662
CK → Q↓	0.1161	0.1088	0.0983	0.0864	4.9203	3.3444	1.6441	0.7823
CK → QN↑	0.1681	0.1539	0.1507	0.1316	5.7163	3.5928	2.6206	1.3669
CK → QN↓	0.1574	0.1573	0.1565	0.1611	4.3657	3.1976	1.6266	0.7839

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.0703	0.0742	0.0742	0.0898
	setup↓ → CK	0.2656	0.2695	0.2734	0.3047
	hold↑ → CK	-0.0586	-0.0586	-0.0586	-0.0625
	hold↓ → CK	-0.2070	-0.2070	-0.2070	-0.2070
SE	setup↑ → CK	0.2695	0.2734	0.2773	0.3086
	setup↓ → CK	0.2930	0.2930	0.2969	0.3320
	hold↑ → CK	-0.0469	-0.0469	-0.0469	-0.0508
	hold↓ → CK	-0.1016	-0.1016	-0.1016	-0.1055
D	setup↑ → CK	0.0820	0.0820	0.0859	0.1016
	setup↓ → CK	0.2695	0.2734	0.2773	0.3125
	hold↑ → CK	-0.0586	-0.0586	-0.0625	-0.0664
	hold↓ → CK	-0.2188	-0.2188	-0.2188	-0.2188
CK	minpwh	0.1125	0.0979	0.0882	0.0736
	minpwl	0.0833	0.0833	0.0882	0.1028
E	setup↑ → CK	0.3008	0.3008	0.3047	0.3398
	setup↓ → CK	0.2422	0.2422	0.2422	0.2539
	hold↑ → CK	-0.0625	-0.0625	-0.0625	-0.0664
	hold↓ → CK	-0.0977	-0.0977	-0.0977	-0.1055

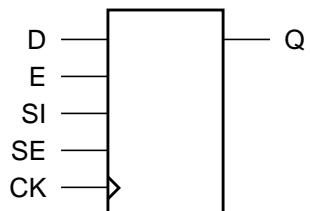
Cell Description

The SEDFFHQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (Q) and fast clock-to-output path.

Functions

D	E	SI	SE	CK	Q[n+1]
x	x	1	1	/\	1
x	x	0	1	/\	0
x	0	x	0	/\	Q[n]
0	1	x	0	/\	0
1	1	x	0	/\	1
x	x	x	x	\/\	Q[n]

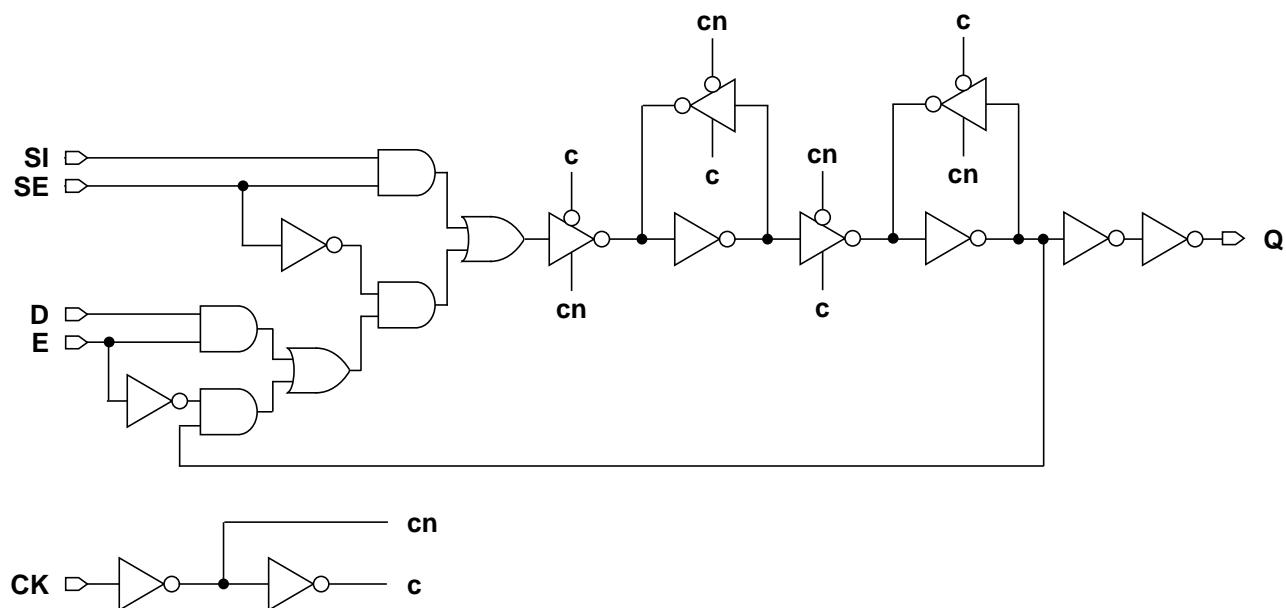
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFHQX1	2.52	11.76
SEDFFHQX2	2.52	13.16
SEDFFHQX4	2.52	14.56
SEDFFHQX8	2.52	15.12

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	X1	X2	X4	X8
SI	0.0090	0.0116	0.0154	0.0157
SE	0.0141	0.0165	0.0198	0.0201
D	0.0093	0.0118	0.0157	0.0160
CK	0.0146	0.0191	0.0235	0.0237
E	0.0146	0.0171	0.0205	0.0207
Q	0.0053	0.0065	0.0082	0.0134

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0012	0.0012	0.0012	0.0012
SE	0.0034	0.0034	0.0034	0.0034
D	0.0016	0.0016	0.0024	0.0024
CK	0.0024	0.0025	0.0031	0.0031
E	0.0024	0.0024	0.0025	0.0025

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0714	0.0718	0.0677	0.0764	3.5650	2.5949	1.3387	0.6906
CK → Q↓	0.0834	0.0822	0.0710	0.0812	3.2325	1.6192	0.7830	0.3977

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.0898	0.0938	0.1016	0.1055
	setup↓ → CK	0.1367	0.1562	0.1836	0.1836
	hold↑ → CK	-0.0547	-0.0547	-0.0625	-0.0625
	hold↓ → CK	-0.1016	-0.1172	-0.1406	-0.1367
SE	setup↑ → CK	0.1445	0.1602	0.1914	0.1914
	setup↓ → CK	0.1602	0.1523	0.1445	0.1445
	hold↑ → CK	-0.0664	-0.0703	-0.0898	-0.0859
	hold↓ → CK	-0.1055	-0.1094	-0.1094	-0.1055
D	setup↑ → CK	0.0820	0.0703	0.0625	0.0625
	setup↓ → CK	0.0703	0.0820	0.0703	0.0703
	hold↑ → CK	-0.0430	-0.0352	-0.0273	-0.0273
	hold↓ → CK	-0.0391	-0.0508	-0.0352	-0.0352
CK	minpwh	0.0492	0.0541	0.0444	0.0492
	minpwl	0.1028	0.0979	0.0833	0.0833
E	setup↑ → CK	0.1211	0.1133	0.1055	0.1094
	setup↓ → CK	0.1641	0.1797	0.1875	0.1875
	hold↑ → CK	-0.0938	-0.0977	-0.0859	-0.0859
	hold↓ → CK	-0.0977	-0.1016	-0.1055	-0.1016

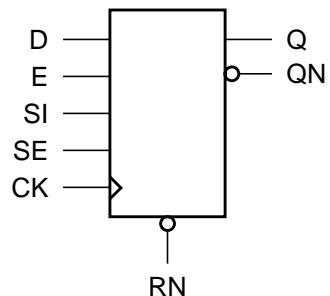
Cell Description

The SEDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), synchronous active-high enable (E) and synchronous active low reset (RN). Scan enable (SE) dominates reset (RN) and enable (E).

Functions

RN	D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	x	0	1	/	0	1
x	x	x	1	1	/	1	0
1	x	0	x	0	/	Q[n]	QN[n]
0	x	x	x	0	/	0	1
1	1	1	x	0	/	1	0
1	0	1	x	0	/	0	1
x	x	x	x	x	/	Q[n]	QN[n]

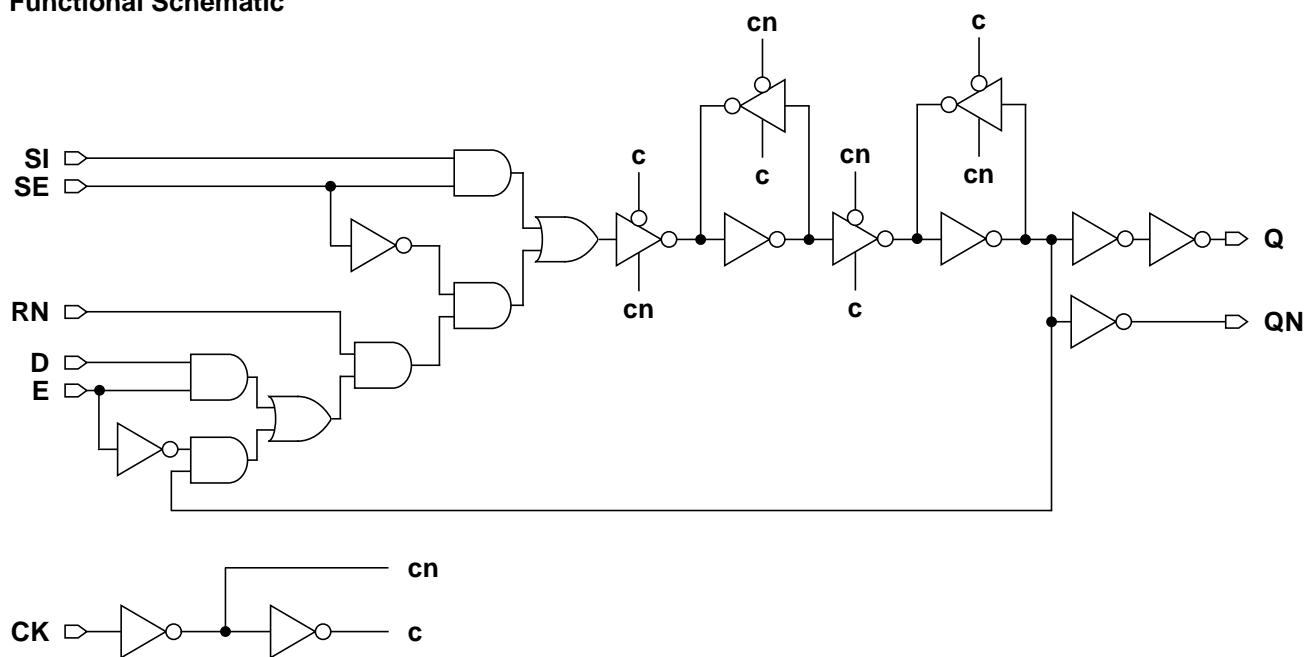
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFFTRXL	2.52	12.60
SEDFFFTRX1	2.52	12.60
SEDFFFTRX2	2.52	12.60
SEDFFFTRX4	2.52	14.56

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
SI	0.0089	0.0094	0.0099	0.0130
SE	0.0119	0.0123	0.0129	0.0160
D	0.0111	0.0114	0.0119	0.0150
CK	0.0115	0.0120	0.0127	0.0163
E	0.0129	0.0132	0.0137	0.0166
RN	0.0093	0.0097	0.0102	0.0130
Q	0.0063	0.0072	0.0090	0.0139

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0011	0.0011	0.0011	0.0011
SE	0.0023	0.0023	0.0023	0.0023
D	0.0012	0.0012	0.0011	0.0012
CK	0.0015	0.0015	0.0015	0.0015
E	0.0011	0.0011	0.0011	0.0011
RN	0.0013	0.0013	0.0013	0.0013

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q \uparrow	0.1420	0.1360	0.1330	0.1274	5.6526	3.6228	2.6517	1.3628
CK → Q \downarrow	0.1356	0.1343	0.1318	0.1295	4.1997	3.0757	1.5453	0.7624
CK → QN \uparrow	0.0930	0.0895	0.0912	0.0884	5.6983	3.6277	2.6732	1.3768
CK → QN \downarrow	0.1048	0.1040	0.0981	0.0908	4.8061	3.3152	1.6420	0.8002

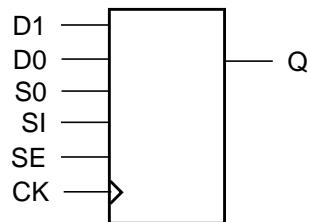
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1016	0.1016	0.1055	0.1328
	setup↓ → CK	0.1328	0.1328	0.1367	0.1406
	hold↑ → CK	-0.0664	-0.0664	-0.0664	-0.0703
	hold↓ → CK	-0.1172	-0.1172	-0.1172	-0.1172
SE	setup↑ → CK	0.1445	0.1484	0.1484	0.1680
	setup↓ → CK	0.1641	0.1680	0.1680	0.1836
	hold↑ → CK	-0.1016	-0.1016	-0.1016	-0.1094
	hold↓ → CK	-0.1094	-0.1094	-0.1094	-0.1172
D	setup↑ → CK	0.1367	0.1406	0.1406	0.1680
	setup↓ → CK	0.1602	0.1602	0.1641	0.1680
	hold↑ → CK	-0.1016	-0.1016	-0.0977	-0.1055
	hold↓ → CK	-0.1445	-0.1445	-0.1445	-0.1445
CK	minpwh	0.0930	0.0882	0.0833	0.0784
	minpwl	0.0882	0.0882	0.0882	0.1076
E	setup↑ → CK	0.1797	0.1797	0.1797	0.1992
	setup↓ → CK	0.1680	0.1641	0.1641	0.1602
	hold↑ → CK	-0.1406	-0.1367	-0.1367	-0.1445
	hold↓ → CK	-0.0703	-0.0742	-0.0820	-0.1094
RN	setup↑ → CK	0.0898	0.0938	0.0938	0.1211
	setup↓ → CK	0.1133	0.1133	0.1172	0.1211
	hold↑ → CK	-0.0508	-0.0508	-0.0508	-0.0586
	hold↓ → CK	-0.0977	-0.0977	-0.0977	-0.1016

Cell Description

The SMDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a 2-to-1 data select control (S0) for the data inputs (D1, D0), scan input (SI), and active-high scan enable (SE). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



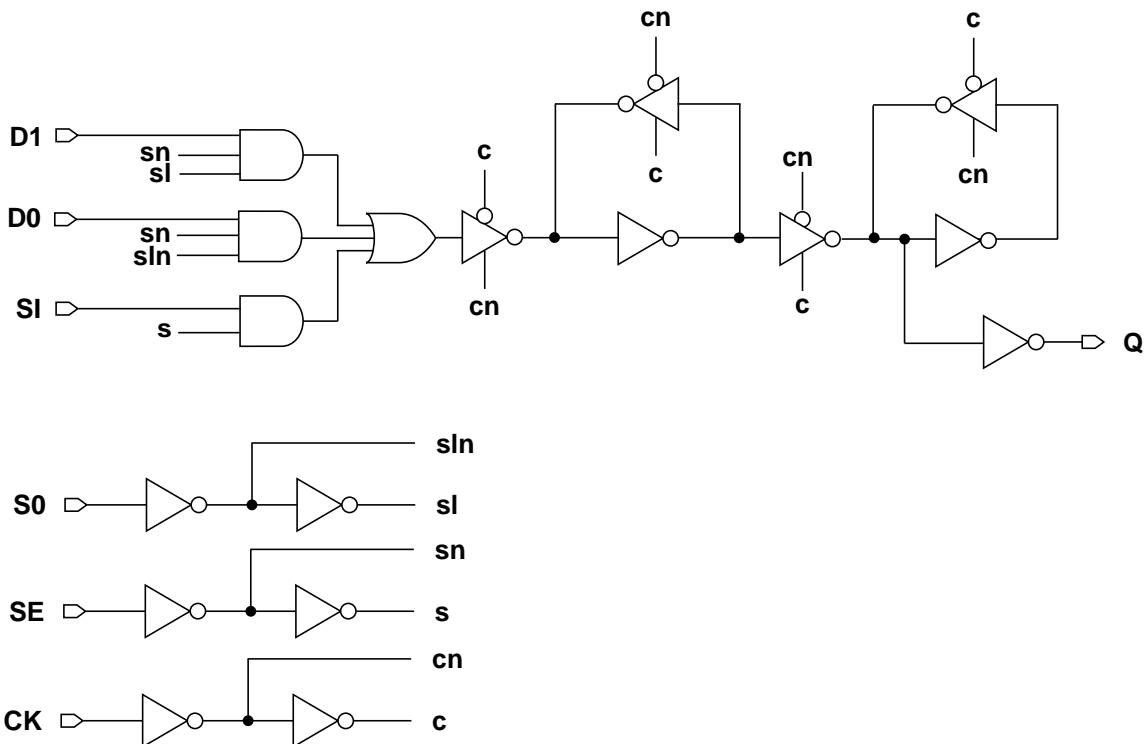
Functions

SE	SI	S0	D1	D0	CK	Q[n+1]
0	x	0	x	0	/\	0
0	x	0	x	1	/\	1
0	x	1	0	x	/\	0
0	x	1	1	x	/\	1
1	0	x	x	x	/\	0
1	1	x	x	x	/\	1
x	x	x	x	x	\/\	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SMDFFHQX1	2.52	11.20
SMDFFHQX2	2.52	12.04
SMDFFHQX4	2.52	14.00
SMDFFHQX8	2.52	14.84

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	X1	X2	X4	X8
SI	0.0086	0.0104	0.0157	0.0160
SE	0.0136	0.0152	0.0201	0.0204
D0	0.0088	0.0107	0.0162	0.0165
D1	0.0087	0.0106	0.0160	0.0163
S0	0.0139	0.0158	0.0213	0.0216
CK	0.0136	0.0166	0.0243	0.0244
Q	0.0037	0.0049	0.0074	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	X1	X2	X4	X8
SI	0.0011	0.0010	0.0012	0.0012
SE	0.0033	0.0033	0.0033	0.0033
D0	0.0012	0.0015	0.0022	0.0022
D1	0.0013	0.0015	0.0021	0.0021
S0	0.0025	0.0025	0.0025	0.0025
CK	0.0022	0.0021	0.0028	0.0028

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	X2	X4	X8	X1	X2	X4	X8
CK → Q↑	0.0742	0.0743	0.0678	0.0768	3.6001	2.6365	1.3320	0.6884
CK → Q↓	0.0824	0.0804	0.0735	0.0839	3.2017	1.5867	0.7732	0.3926

Timing Constraints at 25°C, 1.0V, Typical Process

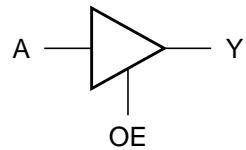
Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.0938	0.0938	0.0898	0.0898
	setup↓ → CK	0.1367	0.1484	0.1406	0.1406
	hold↑ → CK	-0.0547	-0.0547	-0.0547	-0.0547
	hold↓ → CK	-0.1016	-0.1133	-0.1094	-0.1055
SE	setup↑ → CK	0.1484	0.1602	0.1523	0.1523
	setup↓ → CK	0.1641	0.1484	0.1406	0.1406
	hold↑ → CK	-0.0547	-0.0586	-0.0664	-0.0664
	hold↓ → CK	-0.0977	-0.0898	-0.0781	-0.0781
D0	setup↑ → CK	0.0898	0.0742	0.0586	0.0586
	setup↓ → CK	0.1016	0.0859	0.0625	0.0625
	hold↑ → CK	-0.0508	-0.0391	-0.0273	-0.0273
	hold↓ → CK	-0.0703	-0.0547	-0.0352	-0.0352
D1	setup↑ → CK	0.0938	0.0742	0.0625	0.0625
	setup↓ → CK	0.1094	0.0898	0.0703	0.0703
	hold↑ → CK	-0.0508	-0.0391	-0.0273	-0.0273
	hold↓ → CK	-0.0742	-0.0586	-0.0430	-0.0430
S0	setup↑ → CK	0.1289	0.1133	0.1055	0.1055
	setup↓ → CK	0.1445	0.1328	0.1172	0.1172
	hold↑ → CK	-0.0898	-0.0781	-0.0703	-0.0703
	hold↓ → CK	-0.0898	-0.0820	-0.0742	-0.0703
CK	minpwh	0.0492	0.0492	0.0492	0.0492
	minpwl	0.1028	0.1028	0.0833	0.0833

Cell Description

The TBUF cell provides the logical buffer of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



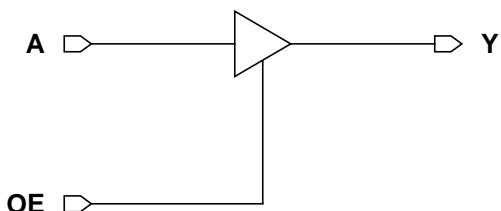
Functions

OE	A	Y
0	x	Z
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
TBUFXL	2.52	2.52
TBUFX1	2.52	2.52
TBUFX2	2.52	2.80
TBUFX3	2.52	3.08
TBUFX4	2.52	3.08
TBUFX6	2.52	3.92
TBUFX8	2.52	4.48
TBUFX12	2.52	5.04
TBUFX16	2.52	6.72
TBUFX20	2.52	8.12

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)									
	XL	X1	X2	X3	X4	X6	X8	X12	X16	X20
A	0.0043	0.0048	0.0059	0.0071	0.0084	0.0108	0.0137	0.0193	0.0260	0.0332
OE	0.0030	0.0033	0.0043	0.0050	0.0059	0.0078	0.0096	0.0141	0.0194	0.0236

Pin Capacitance

Pin	Capacitance (pF)									
	XL	X1	X2	X3	X4	X6	X8	X12	X16	X20
A	0.0012	0.0013	0.0015	0.0016	0.0019	0.0029	0.0037	0.0047	0.0064	0.0087
OE	0.0021	0.0021	0.0024	0.0026	0.0025	0.0024	0.0028	0.0036	0.0044	0.0055
Y	0.0010	0.0012	0.0016	0.0020	0.0026	0.0039	0.0047	0.0073	0.0096	0.0120

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)									
	XL	X1	X2	X3	X4	X6	X8	X12	X16	X20
A → Y↑	0.0504	0.0521	0.0468	0.0478	0.0493	0.0474	0.0453	0.0470	0.0428	0.0442
A → Y↓	0.0893	0.0944	0.0795	0.0685	0.0660	0.0634	0.0583	0.0619	0.0614	0.0565
OE → Y↑	0.0336	0.0348	0.0316	0.0335	0.0352	0.0377	0.0363	0.0396	0.0347	0.0368
OE → Y↓	0.0608	0.0629	0.0571	0.0505	0.0518	0.0523	0.0469	0.0496	0.0510	0.0471

Description	K_{load} (ns/pF)									
	XL	X1	X2	X3	X4	X6	X8	X12	X16	X20
A → Y↑	5.6380	3.7358	2.7041	1.8110	1.3980	1.0021	0.7601	0.5019	0.3938	0.3069
A → Y↓	5.1278	3.4250	1.7700	1.0939	0.8378	0.5809	0.4299	0.2879	0.2132	0.1714
OE → Y↑	5.6216	3.7263	2.7020	1.8106	1.3978	1.0024	0.7601	0.5021	0.3937	0.3068
OE → Y↓	5.1004	3.4020	1.7603	1.0873	0.8344	0.5795	0.4290	0.2871	0.2128	0.1710

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 1$$

Logic Symbol



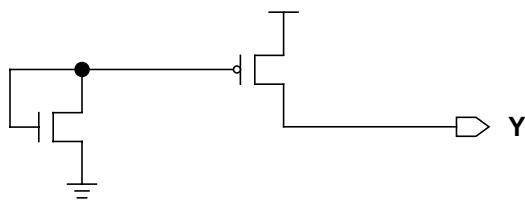
Function

Y
1

Cell Size

Drive Strength	Height (um)	Width (um)
TIEHI	2.52	0.84

Functional Schematic

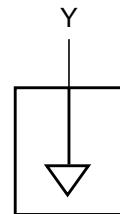


Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 0$$

Logic Symbol



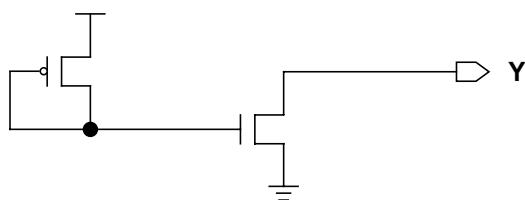
Function

Y
0

Cell Size

Drive Strength	Height (um)	Width (um)
TIELO	2.52	0.84

Functional Schematic



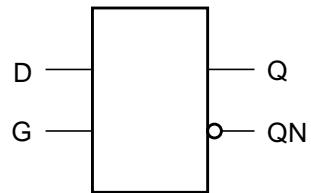
Cell Description

The TLAT cell is an active-high D-type transparent latch. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Functions

G	D	Q[n+1]	QN[n+1]
1	0	0	1
1	1	1	0
0	x	Q[n]	QN[n]

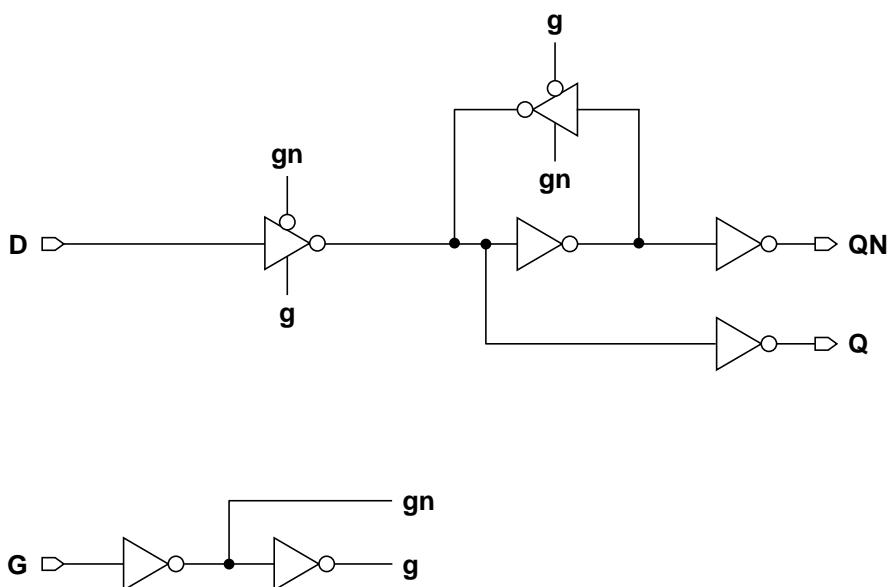
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
TLATXL	2.52	3.64
TLATX1	2.52	3.64
TLATX2	2.52	3.92
TLATX4	2.52	5.60

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0010	0.0012	0.0014	0.0028
G	0.0039	0.0040	0.0045	0.0059
Q	0.0052	0.0061	0.0081	0.0132

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0016	0.0018	0.0021	0.0040
G	0.0012	0.0012	0.0014	0.0019

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.0427	0.0403	0.0424	0.0402	5.6409	3.7254	2.6676	1.3805
D → Q↓	0.0713	0.0670	0.0660	0.0621	4.8915	3.2155	1.6085	0.7872
G → Q↑	0.0918	0.0906	0.0914	0.0916	5.6371	3.7247	2.6669	1.3801
G → Q↓	0.0819	0.0789	0.0719	0.0666	4.8916	3.2183	1.6076	0.7867
D → QN↑	0.1028	0.0991	0.0945	0.0975	5.6214	3.6026	2.6527	1.3646
D → QN↓	0.0814	0.0852	0.0906	0.0832	4.4620	3.0704	1.5661	0.7646
G → QN↑	0.1139	0.1113	0.1007	0.1024	5.6232	3.6034	2.6530	1.3647
G → QN↓	0.1308	0.1359	0.1403	0.1349	4.4637	3.0708	1.5667	0.7646

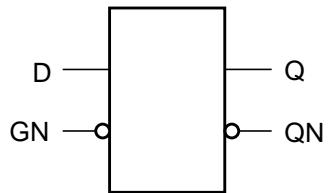
Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	-0.0078	-0.0117	-0.0039	-0.0039
	setup↓ → G	0.0469	0.0430	0.0430	0.0430
	hold↑ → G	0.0156	0.0156	0.0117	0.0117
	hold↓ → G	-0.0430	-0.0391	-0.0352	-0.0391
G	minpwh	0.0638	0.0590	0.0492	0.0541

Cell Description

The TLATN cell is an active-low D-type transparent latch. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



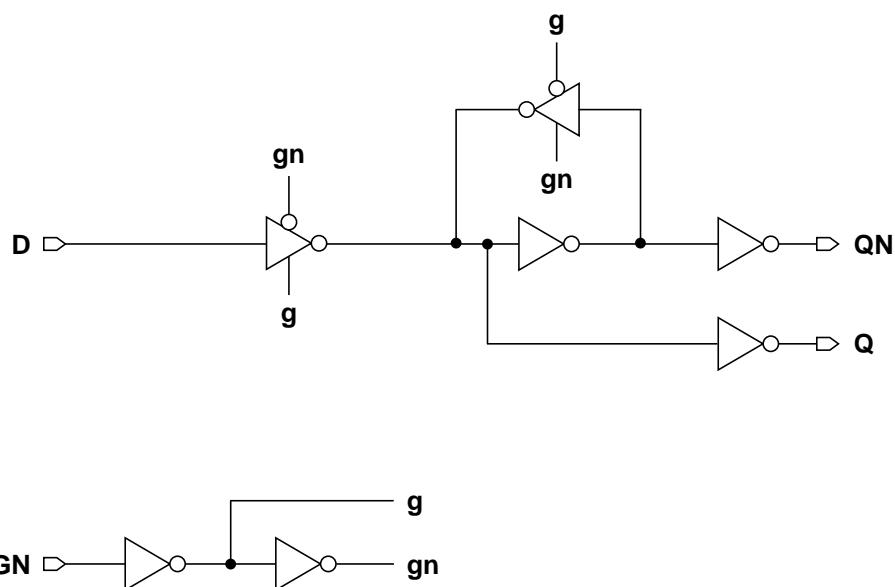
Functions

GN	D	Q[n+1]	QN[n+1]
0	0	0	1
0	1	1	0
1	x	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNXL	2.52	3.92
TLATNX1	2.52	3.92
TLATNX2	2.52	3.92
TLATNX4	2.52	5.60

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0010	0.0012	0.0014	0.0028
GN	0.0046	0.0049	0.0051	0.0077
Q	0.0052	0.0062	0.0079	0.0136

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0016	0.0019	0.0020	0.0040
GN	0.0015	0.0015	0.0015	0.0020

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.0412	0.0395	0.0407	0.0385	5.6768	3.6380	2.6670	1.3797
D → Q↓	0.0698	0.0666	0.0655	0.0622	4.8185	3.1704	1.6038	0.7852
GN → Q↑	0.0667	0.0652	0.0669	0.0618	5.6932	3.6466	2.6699	1.3814
GN → Q↓	0.1091	0.1073	0.1064	0.0984	4.8153	3.1695	1.6034	0.7850
D → QN↑	0.0980	0.0946	0.1025	0.0969	5.6253	3.6193	2.6584	1.3644
D → QN↓	0.0793	0.0831	0.0881	0.0801	4.4577	3.0612	1.5590	0.7623
GN → QN↑	0.1374	0.1355	0.1435	0.1331	5.6272	3.6199	2.6587	1.3644
GN → QN↓	0.1062	0.1104	0.1158	0.1045	4.4600	3.0621	1.5592	0.7625

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.0273	0.0234	0.0273	0.0273
	setup↓ → GN	0.0352	0.0312	0.0273	0.0273
	hold↑ → GN	-0.0234	-0.0195	-0.0234	-0.0195
	hold↓ → GN	-0.0273	-0.0195	-0.0234	-0.0195
GN	minpw1	0.0736	0.0687	0.0736	0.0638

Cell Description

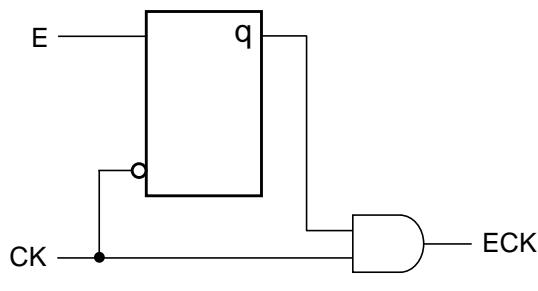
The TLATNCA cell is a positive-edge triggered clock-gating latch. The positive-edge clock (CK) is qualified by the latched enable signal (E) to create the gated positive-edge clock (ECK).

Functions

CK	E	$q[n+1]$	$ECK[n+1]$
1	x	$q[n]$	$q[n]$
0	0	0	0
0	1	1	0

Note: q is an internal node, and is not accessible.

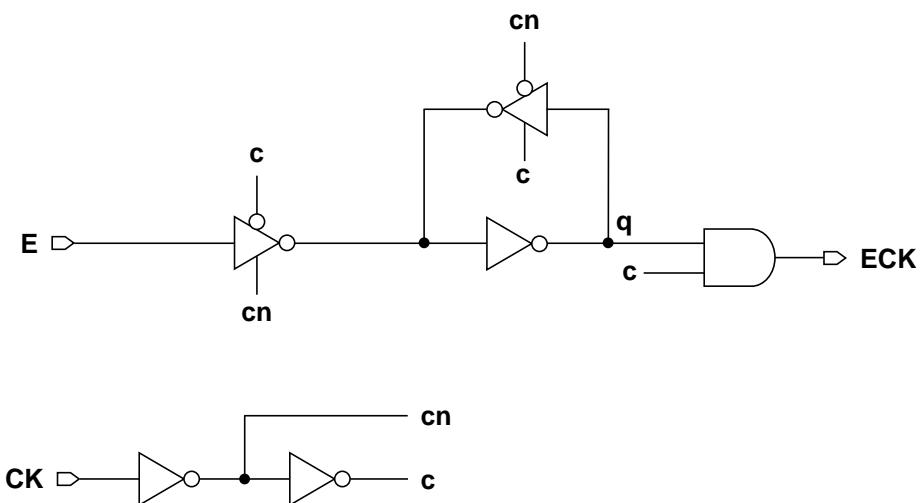
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
TLATNCAX2	2.52	3.64
TLATNCAX3	2.52	4.20
TLATNCAX4	2.52	4.20
TLATNCAX6	2.52	6.44
TLATNCAX8	2.52	7.00
TLATNCAX12	2.52	8.96
TLATNCAX16	2.52	11.48
TLATNCAX20	2.52	13.72

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)							
	X2	X3	X4	X6	X8	X12	X16	X20
E	0.0055	0.0068	0.0071	0.0111	0.0114	0.0166	0.0205	0.0242
CK	0.0057	0.0072	0.0078	0.0107	0.0123	0.0183	0.0236	0.0287
ECK	0.0059	0.0075	0.0084	0.0123	0.0144	0.0188	0.0244	0.0280

Pin Capacitance

Pin	Capacitance (pF)							
	X2	X3	X4	X6	X8	X12	X16	X20
E	0.0016	0.0020	0.0020	0.0043	0.0043	0.0067	0.0083	0.0102
CK	0.0016	0.0020	0.0025	0.0034	0.0043	0.0063	0.0084	0.0105

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X2	X3	X4	X6	X8	X12	X16	X20
CK → ECK↑	0.0486	0.0449	0.0423	0.0420	0.0423	0.0437	0.0445	0.0452
CK → ECK↓	0.0609	0.0611	0.0542	0.0517	0.0493	0.0461	0.0472	0.0460

Delays at 25°C, 1.0V, Typical Process

Description	K_{load} (ns/pF)							
	X2	X3	X4	X6	X8	X12	X16	X20
CK → ECK↑	6.0240	3.5519	2.8130	1.8353	1.3832	1.1280	0.8177	0.7084
CK → ECK↓	2.8577	2.6465	1.9656	1.2566	0.9654	0.6483	0.4818	0.3847

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)							
		X2	X3	X4	X6	X8	X12	X16	X20
E	setup↑ → CK	0.0234	0.0234	0.0273	0.0234	0.0234	0.0195	0.0234	0.0195
	setup↓ → CK	0.0195	0.0156	0.0195	0.0078	0.0156	0.0117	0.0117	0.0117
	hold↑ → CK	-0.0195	-0.0195	-0.0234	-0.0195	-0.0195	-0.0195	-0.0195	-0.0195
	hold↓ → CK	-0.0156	-0.0078	-0.0117	-0.0039	-0.0078	-0.0039	-0.0078	-0.0078
CK	minpw1	0.0687	0.0638	0.0590	0.0541	0.0492	0.0444	0.0492	0.0444

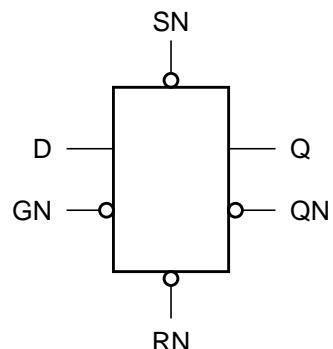
Cell Description

The TLATNSR cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Functions

RN	SN	GN	D	Q[n+1]	QN[n+1]
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

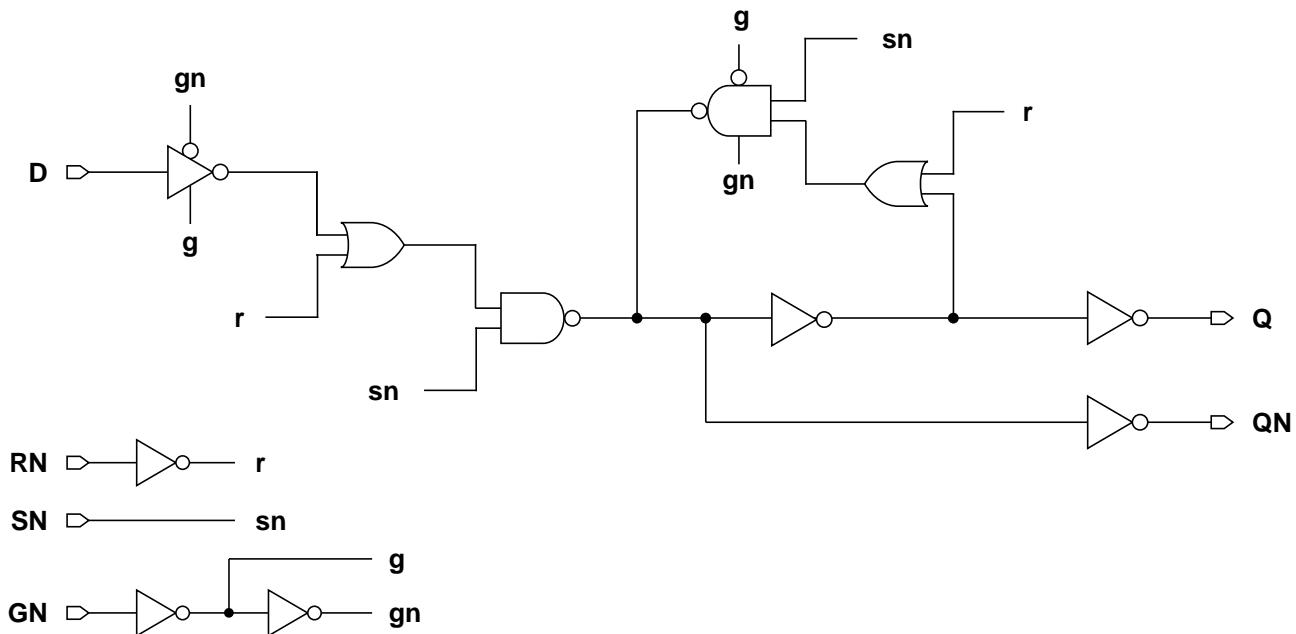
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
TLATNSRXL	2.52	5.60
TLATNSRX1	2.52	5.88
TLATNSRX2	2.52	6.16
TLATNSRX4	2.52	9.24

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
D	0.0011	0.0015	0.0017	0.0034
GN	0.0054	0.0060	0.0065	0.0106
SN	0.0033	0.0040	0.0048	0.0085
RN	0.0011	0.0015	0.0019	0.0036
Q	0.0084	0.0103	0.0151	0.0254

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0016	0.0020	0.0022	0.0043
GN	0.0015	0.0015	0.0015	0.0019
SN	0.0012	0.0015	0.0019	0.0035
RN	0.0019	0.0023	0.0027	0.0049

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.0832	0.0744	0.0815	0.0822	6.0200	3.7899	2.7437	1.4610
D → Q↓	0.1458	0.1331	0.1543	0.1356	6.1792	3.6457	2.0309	0.9605
GN → Q↑	0.0964	0.0900	0.0986	0.1052	6.0361	3.7953	2.7446	1.4609
GN → Q↓	0.1855	0.1637	0.1866	0.1660	6.1764	3.6455	2.0311	0.9606
SN → Q↑	0.1048	0.0930	0.0768	0.0746	5.7964	3.7072	2.6775	1.4280
SN → Q↓	0.1648	0.1481	0.1656	0.1440	6.1480	3.6319	2.0187	0.9534
RN → Q↑	0.0806	0.0720	0.0797	0.0797	6.0197	3.7900	2.7436	1.4610
RN → Q↓	0.1317	0.1157	0.1032	0.0922	6.6371	3.8341	1.9124	0.9218
D → QN↑	0.1885	0.1660	0.1791	0.1529	5.7094	3.6347	2.6546	1.3773
D → QN↓	0.1176	0.1016	0.1035	0.1000	4.5786	2.9079	1.5060	0.7350
GN → QN↑	0.2287	0.1969	0.2117	0.1835	5.7145	3.6361	2.6552	1.3774
GN → QN↓	0.1315	0.1176	0.1209	0.1232	4.5829	2.9092	1.5064	0.7351
SN → QN↑	0.2072	0.1808	0.1901	0.1611	5.7097	3.6345	2.6545	1.3771
SN → QN↓	0.1380	0.1197	0.0986	0.0924	4.5532	2.9005	1.4979	0.7314
RN → QN↑	0.1769	0.1495	0.1251	0.1075	5.7440	3.6452	2.6519	1.3767
RN → QN↓	0.1152	0.0993	0.1018	0.0975	4.5795	2.9081	1.5060	0.7350

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.0703	0.0586	0.0703	0.0703
	setup↓ → GN	0.1133	0.0859	0.1055	0.0938
	hold↑ → GN	-0.0625	-0.0508	-0.0586	-0.0547
	hold↓ → GN	-0.0898	-0.0703	-0.0820	-0.0742
GN	minpwl	0.1515	0.1174	0.1417	0.1271
SN	minpwl	0.0833	0.0687	0.0590	0.0590
	recovery	0.1289	0.1016	0.1094	0.0938
	removal	-0.1250	-0.0977	-0.1055	-0.0898
RN	minpwl	0.1320	0.1028	0.0882	0.0736
	recovery	0.0664	0.0547	0.0625	0.0586
	removal	-0.0625	-0.0508	-0.0586	-0.0547

Cell Description

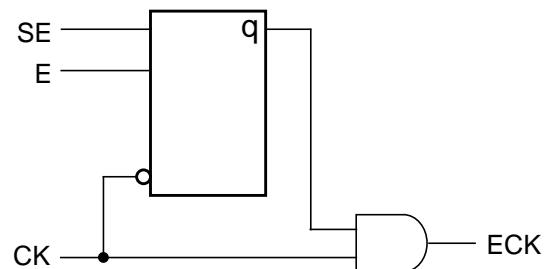
The TLATNTSCA cell is a positive-edge triggered clock-gating latch. The positive-edge clock (CK) is qualified by the latched enable signals (SE) and (E) to create the gated positive-edge clock (ECK).

Functions

CK	SE	E	q[n+1]	ECK[n+1]
1	x	x	q[n]	q[n]
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0

Note: q is an internal node, and is not accessible.

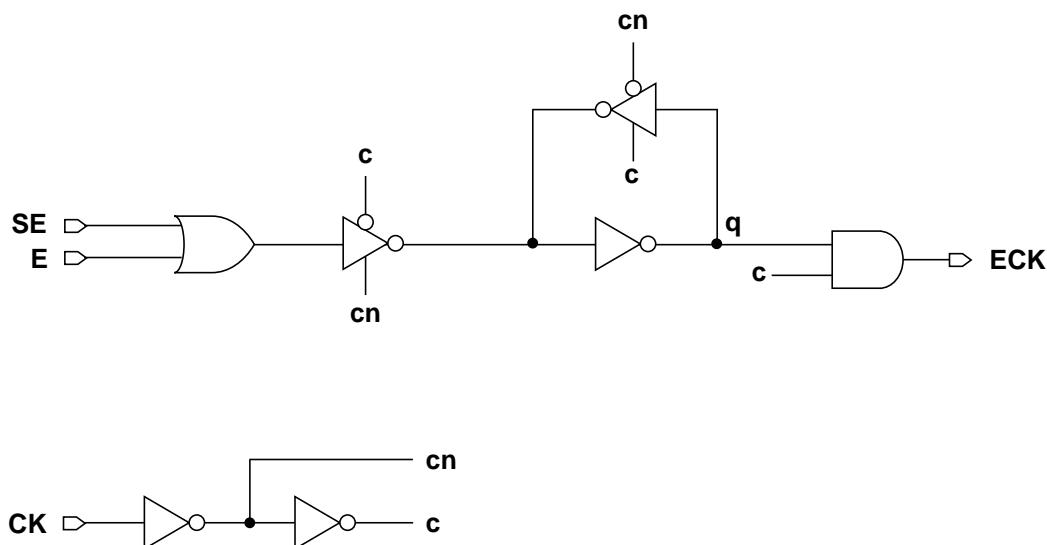
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
TLATNTSCAX2	2.52	5.04
TLATNTSCAX3	2.52	5.60
TLATNTSCAX4	2.52	5.60
TLATNTSCAX6	2.52	7.84
TLATNTSCAX8	2.52	8.68
TLATNTSCAX12	2.52	10.64
TLATNTSCAX16	2.52	13.16
TLATNTSCAX20	2.52	16.24

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)							
	X2	X3	X4	X6	X8	X12	X16	X20
E	0.0092	0.0098	0.0103	0.0152	0.0160	0.0218	0.0272	0.0327
SE	0.0094	0.0101	0.0105	0.0154	0.0163	0.0223	0.0280	0.0334
CK	0.0064	0.0076	0.0082	0.0118	0.0134	0.0187	0.0243	0.0295
ECK	0.0064	0.0074	0.0085	0.0128	0.0145	0.0188	0.0243	0.0280

Pin Capacitance

Pin	Capacitance (pF)							
	X2	X3	X4	X6	X8	X12	X16	X20
E	0.0013	0.0014	0.0014	0.0013	0.0015	0.0018	0.0021	0.0024
SE	0.0014	0.0013	0.0013	0.0013	0.0014	0.0017	0.0021	0.0024
CK	0.0015	0.0020	0.0024	0.0035	0.0044	0.0063	0.0084	0.0104

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X2	X3	X4	X6	X8	X12	X16	X20
CK → ECK↑	0.0502	0.0454	0.0428	0.0432	0.0405	0.0431	0.0447	0.0456
CK → ECK↓	0.0645	0.0624	0.0556	0.0550	0.0518	0.0466	0.0475	0.0461

Delays at 25°C, 1.0V, Typical Process

Description	K_{load} (ns/pF)							
	X2	X3	X4	X6	X8	X12	X16	X20
CK → ECK↑	5.2284	3.5941	2.7203	1.8333	1.3960	1.1282	0.8040	0.7084
CK → ECK↓	2.8326	2.7019	1.9551	1.2911	0.9843	0.6483	0.4817	0.3844

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)							
		X2	X3	X4	X6	X8	X12	X16	X20
E	setup↑ → CK	0.0703	0.0703	0.0664	0.0703	0.0625	0.0664	0.0625	0.0625
	setup↓ → CK	0.0898	0.0820	0.0938	0.0938	0.0898	0.0781	0.0742	0.0820
	hold↑ → CK	-0.0664	-0.0664	-0.0625	-0.0664	-0.0586	-0.0625	-0.0586	-0.0586
	hold↓ → CK	-0.0859	-0.0742	-0.0859	-0.0859	-0.0859	-0.0703	-0.0703	-0.0781
SE	setup↑ → CK	0.0703	0.0742	0.0664	0.0703	0.0664	0.0664	0.0664	0.0664
	setup↓ → CK	0.0977	0.0859	0.0977	0.0977	0.0938	0.0820	0.0781	0.0859
	hold↑ → CK	-0.0664	-0.0703	-0.0625	-0.0664	-0.0625	-0.0625	-0.0625	-0.0625
	hold↓ → CK	-0.0898	-0.0781	-0.0898	-0.0898	-0.0898	-0.0742	-0.0742	-0.0820
CK	minpw1	0.0736	0.0638	0.0590	0.0541	0.0541	0.0492	0.0444	0.0444

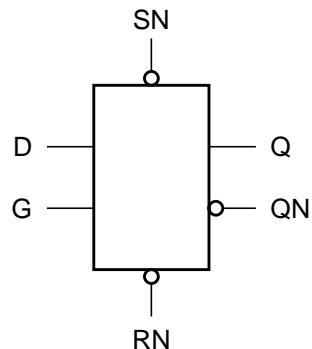
Cell Description

The TLATSR cell is an active-high D-type transparent latch with asynchronous active-low set (SN) and reset(RN), and set dominating reset. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Functions

RN	SN	G	D	Q[n+1]	QN[n+1]
1	1	1	0	0	1
1	1	1	1	1	0
1	1	0	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

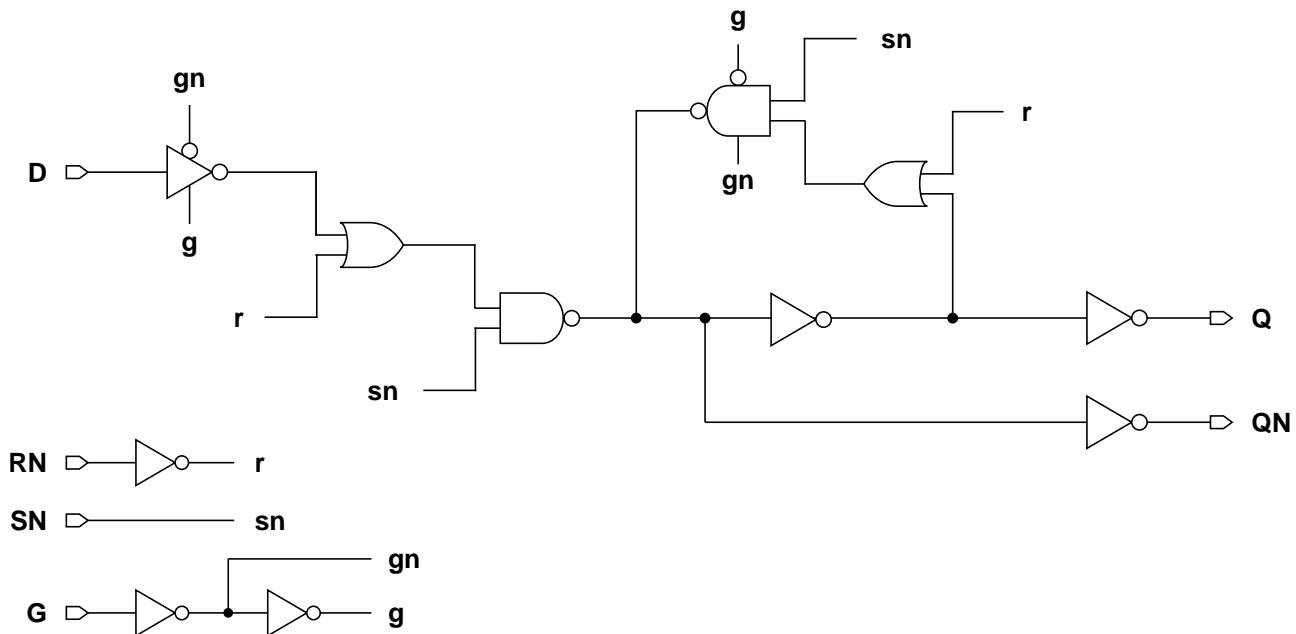
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
TLATSRXL	2.52	5.60
TLATSRX1	2.52	5.60
TLATSRX2	2.52	6.16
TLATSRX4	2.52	8.96

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
D	0.0011	0.0013	0.0016	0.0031
G	0.0047	0.0048	0.0052	0.0079
SN	0.0032	0.0034	0.0042	0.0068
RN	0.0011	0.0012	0.0016	0.0029
Q	0.0079	0.0091	0.0119	0.0191

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0015	0.0017	0.0021	0.0043
G	0.0014	0.0014	0.0015	0.0016
SN	0.0012	0.0013	0.0015	0.0024
RN	0.0018	0.0020	0.0025	0.0043

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.0868	0.0795	0.0780	0.0733	6.0570	3.8958	2.7320	1.4074
D → Q↓	0.1527	0.1414	0.1369	0.1217	6.2505	3.7621	1.9300	0.9244
G → Q↑	0.1237	0.1180	0.1192	0.1213	6.0522	3.8936	2.7306	1.4065
G → Q↓	0.1476	0.1358	0.1289	0.1120	6.2544	3.7642	1.9304	0.9238
SN → Q↑	0.1049	0.0996	0.0920	0.0922	5.7694	3.8004	2.6932	1.3975
SN → Q↓	0.1716	0.1581	0.1514	0.1356	6.2214	3.7489	1.9206	0.9191
RN → Q↑	0.0841	0.0768	0.0758	0.0695	6.0570	3.8957	2.7320	1.4075
RN → Q↓	0.1392	0.1336	0.1147	0.1033	6.7044	4.0661	1.9945	0.9929
D → QN↑	0.1943	0.1826	0.1745	0.1660	5.7067	3.7684	2.6587	1.3716
D → QN↓	0.1337	0.1319	0.1303	0.1167	4.5748	3.0252	1.5737	0.7623
G → QN↑	0.1898	0.1776	0.1670	0.1565	5.7110	3.7708	2.6592	1.3718
G → QN↓	0.1714	0.1711	0.1722	0.1651	4.5793	3.0269	1.5753	0.7627
SN → QN↑	0.2130	0.1991	0.1888	0.1793	5.7063	3.7685	2.6589	1.3717
SN → QN↓	0.1490	0.1499	0.1425	0.1353	4.5371	3.0137	1.5685	0.7610
RN → QN↑	0.1829	0.1773	0.1526	0.1500	5.7420	3.7875	2.6614	1.3735
RN → QN↓	0.1313	0.1294	0.1283	0.1131	4.5755	3.0254	1.5741	0.7624

Timing Constraints at 25°C, 1.0V, Typical Process

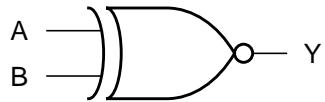
Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.0469	0.0352	0.0312	0.0156
	setup↓ → G	0.1328	0.1211	0.1133	0.1016
	hold↑ → G	-0.0312	-0.0234	-0.0195	-0.0039
	hold↓ → G	-0.1250	-0.1133	-0.1055	-0.0938
G	minpwh	0.1320	0.1174	0.1076	0.0930
SN	minpwl	0.0833	0.0784	0.0736	0.0687
	recovery	0.1523	0.1367	0.1289	0.1172
	removal	-0.1484	-0.1328	-0.1250	-0.1133
RN	minpwl	0.1417	0.1271	0.1028	0.0882
	recovery	0.0430	0.0312	0.0312	0.0039
	removal	-0.0391	-0.0273	-0.0273	0.0000

Cell Description

The XNOR2 cell provides a logical EXCLUSIVE NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B) + (\bar{A} \bullet \bar{B})$$

Logic Symbol



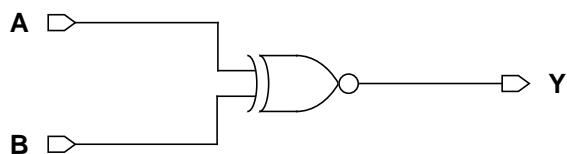
Functions

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR2XL	2.52	2.24
XNOR2X1	2.52	2.24
XNOR2X2	2.52	3.08
XNOR2X4	2.52	4.48

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A	0.0028	0.0034	0.0054	0.0098
B	0.0040	0.0050	0.0087	0.0152

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0017	0.0018	0.0024	0.0031
B	0.0013	0.0016	0.0024	0.0045

Delays at 25°C, 1.0V, Typical Process

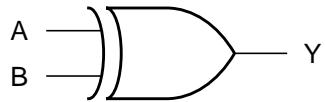
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.0271	0.0248	0.0243	0.0258	8.2668	5.9609	3.6160	1.8264
A → Y↓	0.0307	0.0317	0.0363	0.0347	5.9522	4.4689	2.2738	1.1247
B → Y↑	0.0472	0.0418	0.0457	0.0402	8.2767	5.9135	3.6045	1.8195
B → Y↓	0.0505	0.0443	0.0473	0.0416	6.3702	4.6867	2.3567	1.1883

Cell Description

The XOR2 cell provides a logical EXCLUSIVE OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet \bar{B}) + (\bar{A} \bullet B)$$

Logic Symbol



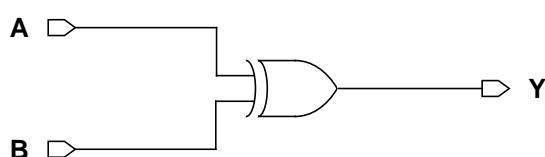
Functions

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
XOR2XL	2.52	2.24
XOR2X1	2.52	2.24
XOR2X2	2.52	3.08
XOR2X3	2.52	4.48
XOR2X4	2.52	4.76
XOR2X8	2.52	8.12

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)					
	XL	X1	X2	X3	X4	X8
A	0.0028	0.0034	0.0056	0.0081	0.0102	0.0181
B	0.0043	0.0053	0.0091	0.0128	0.0162	0.0315

Pin Capacitance

Pin	Capacitance (pF)					
	XL	X1	X2	X3	X4	X8
A	0.0018	0.0018	0.0024	0.0027	0.0034	0.0061
B	0.0013	0.0017	0.0024	0.0036	0.0045	0.0089

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	XL	X1	X2	X3	X4	X8
A → Y↑	0.0283	0.0250	0.0238	0.0275	0.0256	0.0242
A → Y↓	0.0311	0.0314	0.0367	0.0376	0.0347	0.0317
B → Y↑	0.0462	0.0408	0.0427	0.0389	0.0373	0.0365
B → Y↓	0.0511	0.0446	0.0489	0.0445	0.0432	0.0419

Description	K_{load} (ns/pF)					
	XL	X1	X2	X3	X4	X8
A → Y↑	8.2348	5.9492	3.6599	2.4244	1.7986	0.9225
A → Y↓	6.1071	4.5295	2.2998	1.4939	1.1304	0.5637
B → Y↑	8.2358	5.9021	3.6223	2.4205	1.8267	0.9354
B → Y↓	6.3415	4.6680	2.4021	1.5580	1.1737	0.5815

Synthesis Optimized Arithmetic Cells

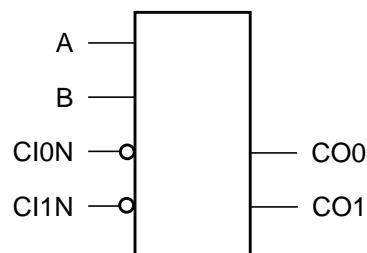
Cell Description

The ACCSHCIN cell provides a carry-select adder-carry generation function with active-low carry inputs. The function produces the carry-outs (CO0, CO1) of the operands (A, B) with active-low carry-ins (CI0N, CI1N). The outputs (CO0, CO1) are represented by the logic equations:

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet \overline{CI0N})$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

Logic Symbol



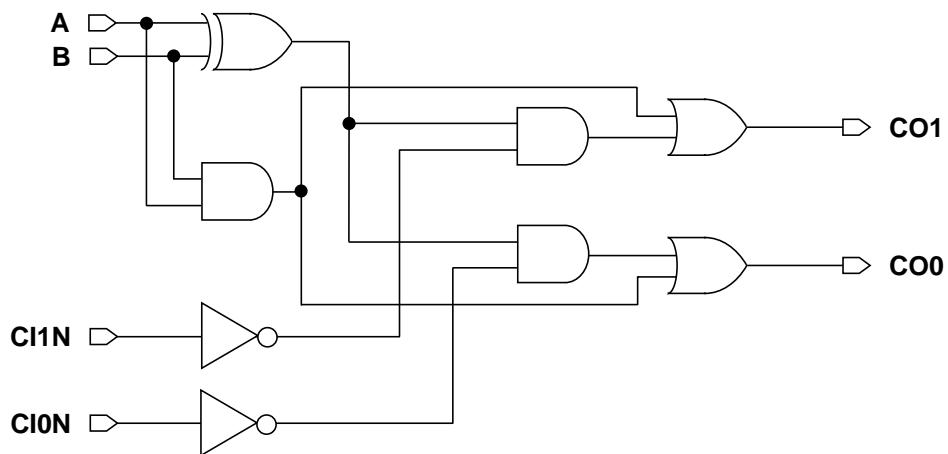
Functions

A	B	CI0N	CI1N	CO0	CO1
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ACCSHCINX2	2.52	10.08
ACCSHCINX4	2.52	12.32

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0234	0.0323
B	0.0209	0.0302
CI0N	0.0058	0.0099
CI1N	0.0063	0.0105

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0024	0.0025
B	0.0056	0.0058
CI0N	0.0024	0.0043
CI1N	0.0024	0.0046

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → CO0↑	0.0892	0.1055	3.9919	2.1646
A → CO0↓	0.1080	0.1416	2.6355	1.4198
B → CO0↑	0.0734	0.0807	3.9057	2.1008
B → CO0↓	0.0794	0.0998	2.6126	1.4103
CI0N → CO0↑	0.0270	0.0255	3.6408	1.9141
CI0N → CO0↓	0.0187	0.0191	2.2517	1.2306
A → CO1↑	0.0970	0.1136	3.7322	2.2467
A → CO1↓	0.1135	0.1484	2.4213	1.4989
B → CO1↑	0.0573	0.0781	3.7083	2.2073
B → CO1↓	0.0755	0.1017	2.3772	1.4910
CI1N → CO1↑	0.0298	0.0254	3.6048	1.7986
CI1N → CO1↓	0.0214	0.0194	2.3079	1.1751

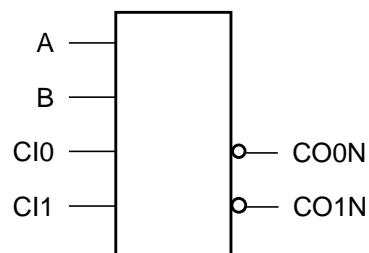
Cell Description

The ACCSHCON cell provides a carry-select adder-carry generation function that produces active-low carry-outs (CO0N, CO1N) of the operands (A, B) with carry-ins (CI0, CI1). The outputs (CO0N, CO1N) are represented by the logic equations:

$$CO0N = \overline{(A \bullet B)} + (A \bullet CI0) + (B \bullet CI0)$$

$$CO1N = \overline{(A \bullet B)} + (A \bullet CI1) + (B \bullet CI1)$$

Logic Symbol



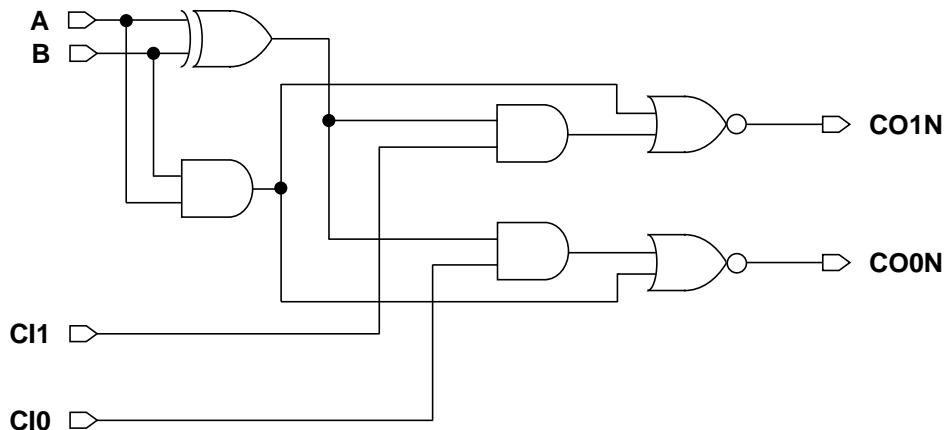
Functions

A	B	CI0	CI1	CO0N	CO1N
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	0	0
1	1	1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACCSHCONX2	2.52	8.68
ACCSHCONX4	2.52	10.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0212	0.0253
B	0.0191	0.0227
CI0	0.0052	0.0091
CI1	0.0061	0.0097

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0046	0.0047
B	0.0066	0.0064
CI0	0.0024	0.0047
CI1	0.0024	0.0046

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → CO0N↑	0.1048	0.1239	3.4815	3.5037
A → CO0N↓	0.1029	0.1261	2.5002	2.4040
B → CO0N↑	0.0831	0.1030	3.5929	3.5062
B → CO0N↓	0.0817	0.1045	2.5023	2.4062
CI0 → CO0N↑	0.0252	0.0232	3.6522	1.8277
CI0 → CO0N↓	0.0172	0.0164	2.2519	1.1651
A → CO1N↑	0.1061	0.1252	3.8352	3.8324
A → CO1N↓	0.1024	0.1245	2.4384	2.3511
B → CO1N↑	0.0856	0.1042	3.8361	3.8319
B → CO1N↓	0.0808	0.1025	2.4375	2.3494
CI1 → CO1N↑	0.0304	0.0253	3.6359	1.8935
CI1 → CO1N↓	0.0211	0.0178	2.3104	1.2108

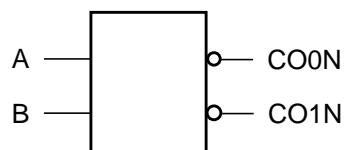
Cell Description

The ACCSIHCON cell provides a carry-select adder-carry generation function for the first stage of a carry-select adder block i.e., there are no carry-inputs). The function produces active-low carry-outs (CO0N, CO1N) of the operands (A, B).The outputs (CO0N, CO1N) are represented by the logic equations:

$$CO0N = \overline{A \bullet B}$$

$$CO1N = \overline{A + B}$$

Logic Symbol



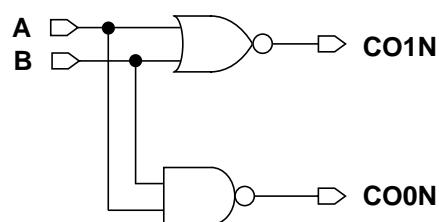
Functions

A	B	CO0N	CO1N
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACCSIHCONX2	2.52	1.96
ACCSIHCONX4	2.52	3.36

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0041	0.0077
B	0.0048	0.0091

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0038	0.0072
B	0.0043	0.0080

Delays at 25°C, 1.0V, Typical Process

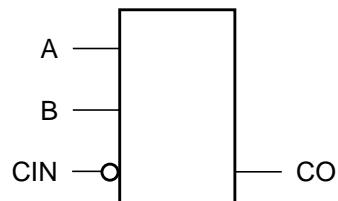
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → CO0N↑	0.0160	0.0165	2.7484	1.4955
A → CO0N↓	0.0137	0.0130	2.4475	1.2027
B → CO0N↑	0.0135	0.0133	2.6877	1.5116
B → CO0N↓	0.0125	0.0111	2.4479	1.2017
A → CO1N↑	0.0204	0.0184	5.3240	2.7166
A → CO1N↓	0.0094	0.0092	1.4527	0.8096
B → CO1N↑	0.0244	0.0237	5.3171	2.7155
B → CO1N↓	0.0103	0.0109	1.4369	0.8167

Cell Description

The ACHCIN cell is a full adder carry-generator that provides the arithmetic carry-out (CO) of two operands (A, B) with active low carry-in (CIN). The output (CO) is represented by the logic equation:

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol



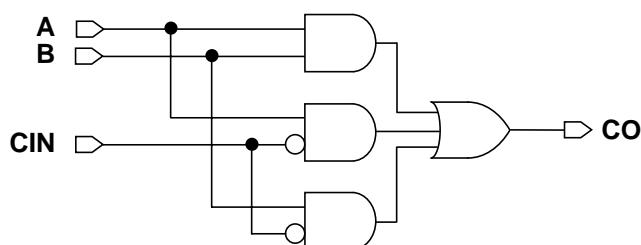
Functions

A	B	CIN	CO
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ACHCINX2	2.52	5.88
ACHCINX4	2.52	7.28

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0147	0.0183
B	0.0159	0.0187
CIN	0.0056	0.0088

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0025	0.0025
B	0.0055	0.0061
CIN	0.0025	0.0046

Delays at 25°C, 1.0V, Typical Process

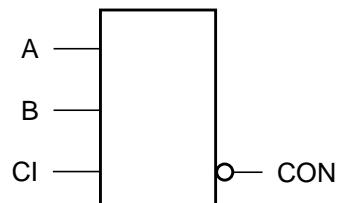
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → CO↑	0.0721	0.0827	3.8084	3.6925
A → CO↓	0.0795	0.0945	2.3760	2.2847
B → CO↑	0.0584	0.0649	3.6887	3.6504
B → CO↓	0.0662	0.0716	2.3236	2.2778
CIN → CO↑	0.0264	0.0222	3.4911	1.8584
CIN → CO↓	0.0199	0.0169	2.3041	1.2276

Cell Description

The ACHCON cell is a full adder carry-generator that provides the arithmetic active-low carry-out (CON) of two operands (A, B) with carry-in (CI). The output (CON) is represented by the logic equation:

$$CON = \overline{(A \bullet B)} + (A \bullet CI) + (B \bullet CI)$$

Logic Symbol



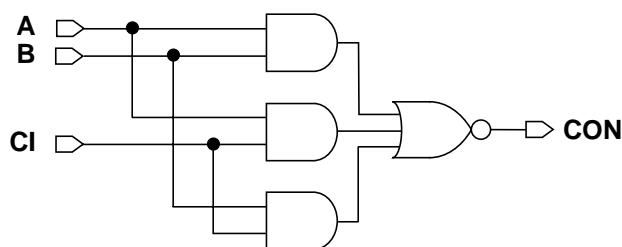
Functions

A	B	CI	CON
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACHCONX2	2.52	5.88
ACHCONX4	2.52	7.28

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0162	0.0194
B	0.0156	0.0179
Cl	0.0055	0.0087

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0025	0.0025
B	0.0074	0.0078
Cl	0.0025	0.0046

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → CON↑	0.0918	0.1012	3.5732	3.5795
A → CON↓	0.0893	0.0964	2.2748	2.2045
B → CON↑	0.0602	0.0647	3.6622	3.6265
B → CON↓	0.0533	0.0612	2.3462	2.2364
Cl → CON↑	0.0266	0.0221	3.5154	1.8577
Cl → CON↓	0.0198	0.0170	2.3041	1.2312

Cell Description

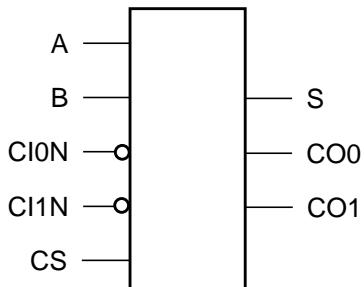
The AFCSHCIN cell provides a carry-select adder function that produces the arithmetic sum (S) and carry-outs (CO0, CO1) of the operands (A, B) with active-low carry-ins (CI0N, CI1N). The three outputs (S, CO0, CO1) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus \overline{CI1N}) + \overline{CS} \bullet (A \oplus B \oplus \overline{CI0N})$$

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet \overline{CI0N})$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

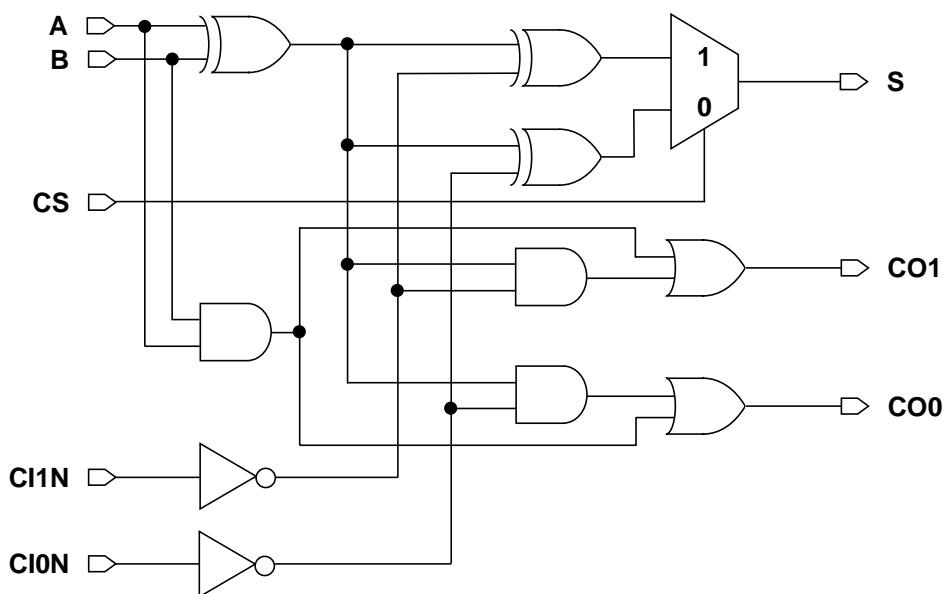
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AFCSHCINX2	2.52	15.96
AFCSHCINX4	2.52	16.80

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
CS	0.0090	0.0091
A	0.0374	0.0381
B	0.0339	0.0344
CI0N	0.0184	0.0205
CI1N	0.0191	0.0211

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0019	0.0019
A	0.0025	0.0025
B	0.0056	0.0057
CI0N	0.0042	0.0065
CI1N	0.0046	0.0066

Functions

A	B	CI0N	CI1N	CS	S	CO0	CO1
0	0	0	0	0	1	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0
0	0	1	0	1	1	0	0
0	0	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	1	1
0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	0
0	1	0	1	1	1	1	0
0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	1	0	0
0	1	1	1	1	1	0	0

Functions (cont.)

A	B	CI0N	CI1N	CS	S	CO0	CO1
1	0	0	0	0	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	0	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	0	1	0	1
1	0	1	0	1	0	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	0	1	1
1	1	1	1	1	0	1	1

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
CS → S↑	0.0795	0.0787	2.6174	2.6539
CS → S↓	0.0735	0.0772	1.5969	1.5250
A → S↑	0.2197	0.2185	2.6211	2.6552
A → S↓	0.2158	0.2161	1.5986	1.5230
B → S↑	0.1791	0.1785	2.6209	2.6551
B → S↓	0.1795	0.1827	1.5991	1.5238
CI0N → S↑	0.1371	0.1348	2.6210	2.6553
CI0N → S↓	0.1375	0.1385	1.5979	1.5228
CI1N → S↑	0.1253	0.1259	2.6112	2.6522
CI1N → S↓	0.1174	0.1194	1.5971	1.5250
A → CO0↑	0.1055	0.1072	3.9648	3.8534
A → CO0↓	0.1232	0.1271	2.6493	2.5405
B → CO0↑	0.0810	0.0844	3.9115	3.8200
B → CO0↓	0.0871	0.0907	2.6210	2.5321
CI0N → CO0↑	0.0293	0.0227	3.7206	2.6563
CI0N → CO0↓	0.0192	0.0157	2.2794	1.7870
A → CO1↑	0.1024	0.1067	4.0357	3.9083
A → CO1↓	0.1294	0.1336	2.7034	2.6033
B → CO1↑	0.0716	0.0741	3.9758	3.8904
B → CO1↓	0.0880	0.0924	2.6893	2.5971
CI1N → CO1↑	0.0283	0.0220	3.7174	2.6472
CI1N → CO1↓	0.0194	0.0156	2.3422	1.8112

Cell Description

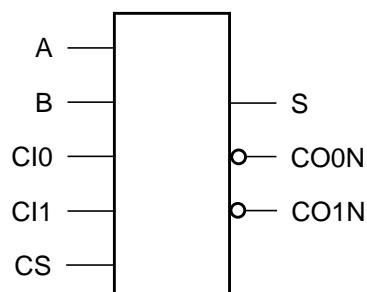
The AFCSHCON cell provides a carry-select adder function that produces the arithmetic sum (S) and active-low carry-outs (CO0N, CO1N) of two operands (A, B) with carry-ins (CI0, CI1). The three outputs (S, CO0N, CO1N) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus CI1) + \overline{CS} \bullet (A \oplus B \oplus CI0)$$

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol



Cell Size

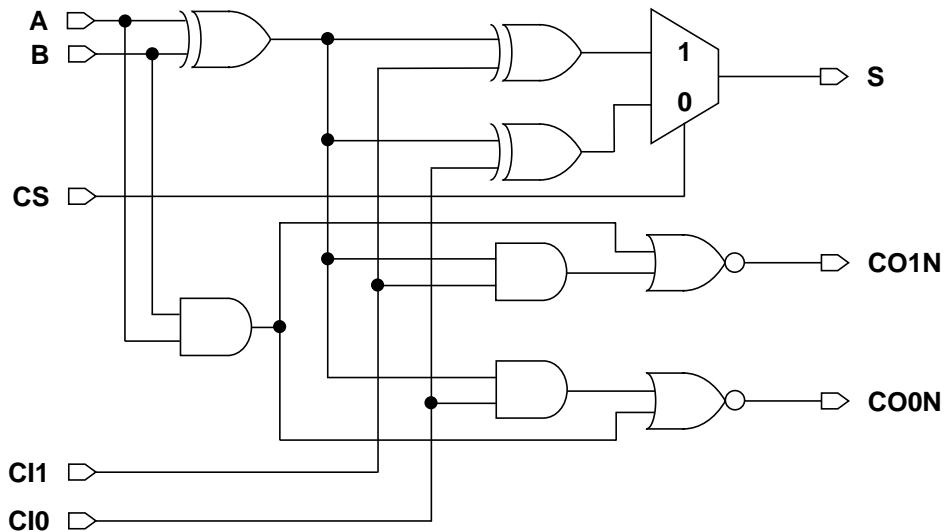
Drive Strength	Height (um)	Width (um)
AFCSHCONX2	2.52	14.84
AFCSHCONX4	2.52	15.68

Functions

A	B	CI0	CI1	CS	S	CO0N	CO1N
0	0	0	0	0	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	0	0	1	1
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1
0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1
0	1	0	0	1	1	1	1
0	1	0	1	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	0	0	0
0	1	1	1	1	1	0	0

A	B	CI0	CI1	CS	S	CO0N	CO1N
1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	0	1	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	0	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	1	0	0

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
CS	0.0089	0.0090
A	0.0348	0.0354
B	0.0343	0.0352
CI0	0.0167	0.0189
CI1	0.0176	0.0195

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0038	0.0037
A	0.0046	0.0046
B	0.0053	0.0054
CI0	0.0042	0.0066
CI1	0.0047	0.0068

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
CS → S↑	0.0792	0.0784	2.6227	2.5891
CS → S↓	0.0754	0.0772	1.6023	1.5280
A → S↑	0.2661	0.2707	2.6260	2.5902
A → S↓	0.2506	0.2561	1.6003	1.5262
B → S↑	0.2529	0.2574	2.6258	2.5901
B → S↓	0.2374	0.2429	1.6003	1.5262
Cl0 → S↑	0.1338	0.1354	2.6265	2.5904
Cl0 → S↓	0.1343	0.1376	1.5982	1.5251
Cl1 → S↑	0.1258	0.1267	2.6186	2.5874
Cl1 → S↓	0.1180	0.1205	1.6024	1.5279
A → CO0N↑	0.1150	0.1154	3.7239	3.7846
A → CO0N↓	0.1609	0.1721	2.7545	2.5470
B → CO0N↑	0.1015	0.1042	3.8605	3.7819
B → CO0N↓	0.1474	0.1587	2.7525	2.5465
Cl0 → CO0N↑	0.0260	0.0191	3.9661	2.9550
Cl0 → CO0N↓	0.0185	0.0158	2.3787	1.8938
A → CO1N↑	0.1232	0.1199	4.1062	3.6647
A → CO1N↓	0.1641	0.1752	2.7214	2.5224
B → CO1N↑	0.1023	0.1047	3.6643	3.6870
B → CO1N↓	0.1507	0.1617	2.7184	2.5206
Cl1 → CO1N↑	0.0255	0.0190	4.0252	3.0076
Cl1 → CO1N↓	0.0191	0.0163	2.5873	2.1029

Cell Description

The AFCSIHCON cell provides a carry-select adder function for the initial stage of carry-select adder block. The function produces the arithmetic sum (S) and active-low carry-outs (CO0N, CO1N) of two operands (A, B). The three outputs (S, CO0N, CO1N) are represented by the logic equations:

$$S = A \oplus B \oplus CS$$

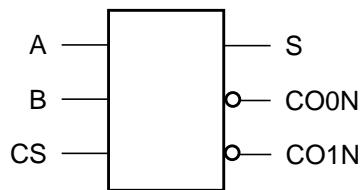
$$CO0N = \overline{A \bullet B}$$

$$CO1N = \overline{A + B}$$

Functions

A	B	CS	S	CO0N	CO1N
0	0	0	0	1	1
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	1	0	0

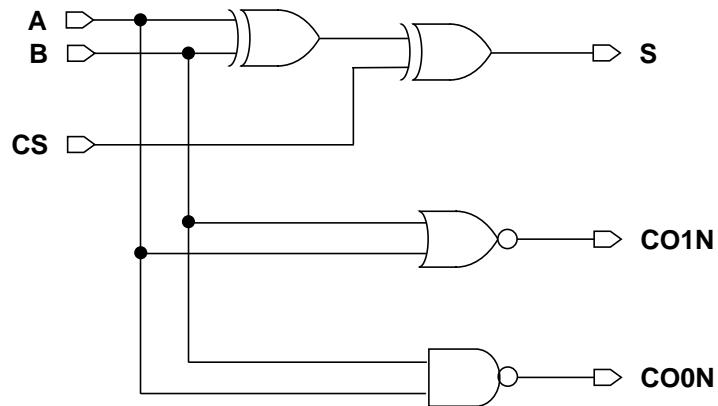
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
AFCSIHCONX2	2.52	6.16
AFCSIHCONX4	2.52	9.24

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0173	0.0275
B	0.0171	0.0291
CS	0.0081	0.0154

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0058	0.0094
B	0.0077	0.0111
CS	0.0037	0.0059

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.1250	0.1490	2.6279	1.3556
A → S↓	0.1351	0.1824	1.8086	1.0255
B → S↑	0.1164	0.1472	2.6796	1.4197
B → S↓	0.1412	0.1575	1.5950	1.0067
CS → S↑	0.0716	0.0734	2.6236	1.3501
CS → S↓	0.0575	0.0849	1.7734	1.0203
A → CO0N↑	0.0131	0.0136	2.6667	1.6428
A → CO0N↓	0.0134	0.0116	2.7977	1.3514
B → CO0N↑	0.0159	0.0163	2.7236	1.6027
B → CO0N↓	0.0150	0.0132	2.7975	1.3516
A → CO1N↑	0.0204	0.0217	5.7789	3.0614
A → CO1N↓	0.0097	0.0103	1.6727	0.7966
B → CO1N↑	0.0259	0.0258	5.7785	3.0586
B → CO1N↓	0.0113	0.0104	1.6705	0.7928

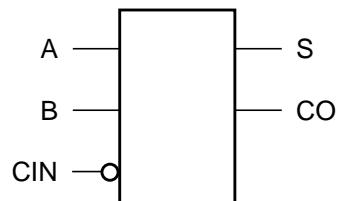
Cell Description

The AFHCIN cell is a full adder that provides the arithmetic sum (S) and carry-out (CO) of two operands (A, B) with active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

$$S = A \oplus B \oplus \overline{CIN}$$

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol



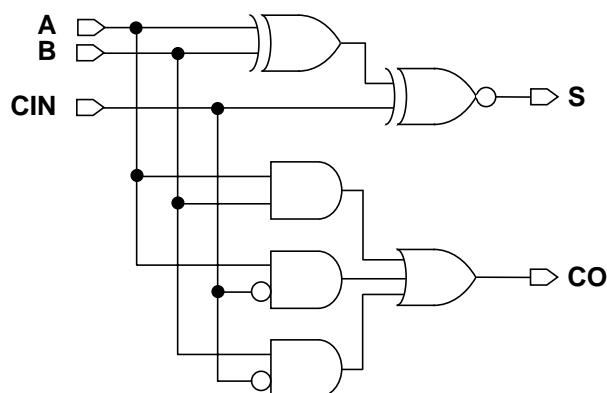
Functions

A	B	CIN	S	CO
0	0	0	1	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
AFHCINX2	2.52	8.96
AFHCINX4	2.52	9.80

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0206	0.0222
B	0.0215	0.0230
CIN	0.0152	0.0186

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0024	0.0025
B	0.0059	0.0059
CIN	0.0046	0.0068

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.1147	0.1215	2.8585	2.8765
A → S↓	0.1268	0.1358	1.6091	1.5216
B → S↑	0.1015	0.1086	2.8600	2.8770
B → S↓	0.0988	0.1074	1.6081	1.5208
CIN → S↑	0.0664	0.0697	2.8540	2.8736
CIN → S↓	0.0731	0.0789	1.6120	1.5221
A → CO↑	0.0768	0.0864	3.8053	3.8674
A → CO↓	0.0910	0.1014	2.4801	2.4854
B → CO↑	0.0635	0.0697	3.7133	3.8387
B → CO↓	0.0733	0.0824	2.4286	2.4759
CIN → CO↑	0.0260	0.0200	3.5652	1.9279
CIN → CO↓	0.0218	0.0178	2.4165	1.2861

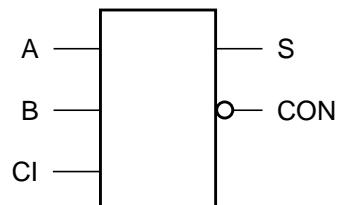
Cell Description

The AFHCON cell is a full adder that provides the arithmetic sum (S) and active-low carry-out (CON) of two operands (A, B) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus B \oplus CI$$

$$CON = \overline{(A \bullet B)} + (A \bullet CI) + (B \bullet CI)$$

Logic Symbol



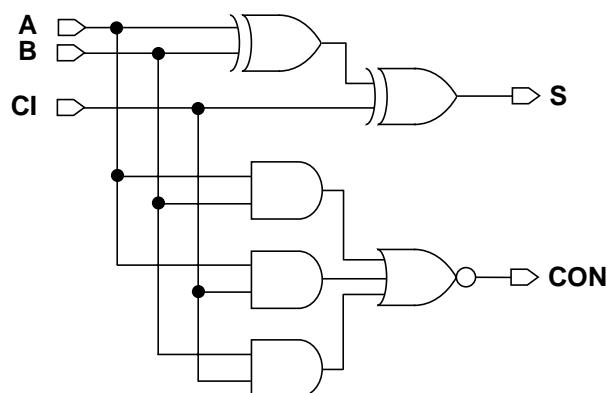
Functions

A	B	CI	S	CON
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AFHCONX2	2.52	8.96
AFHCONX4	2.52	9.80

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0218	0.0236
B	0.0205	0.0223
Cl	0.0156	0.0189

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0025	0.0025
B	0.0070	0.0071
Cl	0.0046	0.0069

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.1149	0.1194	2.8512	2.8745
A → S↓	0.1280	0.1354	1.6103	1.5241
B → S↑	0.0859	0.0894	2.8533	2.8751
B → S↓	0.0992	0.1067	1.6100	1.5238
Cl → S↑	0.0675	0.0685	2.8451	2.8724
Cl → S↓	0.0757	0.0799	1.6121	1.5243
A → CON↑	0.1009	0.1101	3.5922	3.7360
A → CON↓	0.0877	0.0993	2.3757	2.4157
B → CON↑	0.0736	0.0835	3.6478	3.7603
B → CON↓	0.0591	0.0698	2.3925	2.4374
Cl → CON↑	0.0287	0.0226	3.6099	1.8604
Cl → CON↓	0.0215	0.0177	2.4053	1.1856

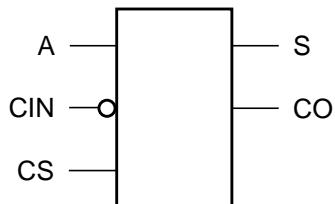
Cell Description

The AHCSHCIN cell provides a carry-select half-adder function that produces the arithmetic sum (S) and carry-out (CO) of a single operand (A) with active-low carry-in (CIN). The outputs (S, CO) are represented by the following equations:

$$S = CS \bullet (A \oplus \overline{CIN}) + \overline{CS} \bullet (A)$$

$$CO = A \bullet \overline{CIN}$$

Logic Symbol



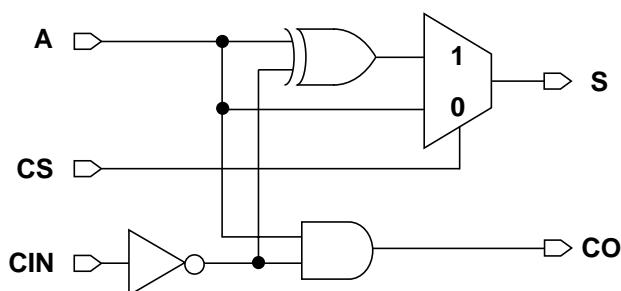
Functions

A	CIN	CS	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHCSHCINX2	2.52	5.32
AHCSHCINX4	2.52	6.16

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
CS	0.0079	0.0110
A	0.0155	0.0232
CIN	0.0146	0.0215

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0036	0.0036
A	0.0023	0.0024
CIN	0.0063	0.0083

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
CS → S↑	0.0582	0.0633	2.6187	1.3401
CS → S↓	0.0630	0.0759	1.7828	0.9323
A → S↑	0.1094	0.1281	2.6610	1.3674
A → S↓	0.1400	0.1615	1.8030	0.9377
CIN → S↑	0.1056	0.1134	2.6602	1.3668
CIN → S↓	0.1046	0.1213	1.8021	0.9378
A → CO↑	0.0516	0.0561	5.3639	2.7278
A → CO↓	0.0603	0.0712	1.5944	0.8373
CIN → CO↑	0.0204	0.0188	5.3613	2.7197
CIN → CO↓	0.0094	0.0088	1.4525	0.7107

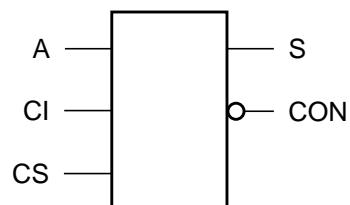
Cell Description

The AHCSHCON cell provides a carry-select half-adder function that produces the arithmetic sum (S) and active-low carry-out (CON) of a single operand (A) with carry-in (CI). The outputs (S, CON) are represented by the following equations:

$$S = CS \bullet (A \oplus CI) + \overline{CS} \bullet (A)$$

$$CON = \overline{A \bullet CI}$$

Logic Symbol



Functions

A	CI	CS	S	CON
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

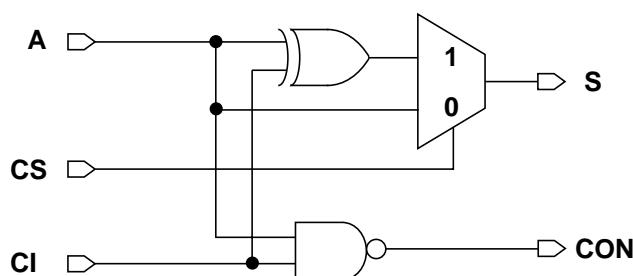
Cell Size

Drive Strength	Height (um)	Width (um)
AHCSHCONX2	2.52	5.32
AHCSHCONX4	2.52	6.16

AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
CS	0.0076	0.0106
A	0.0156	0.0218
CI	0.0116	0.0164

Functional Schematic



Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0036	0.0036
A	0.0043	0.0070
Cl	0.0053	0.0068

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
CS → S↑	0.0575	0.0631	2.6274	1.3398
CS → S↓	0.0625	0.0755	1.7868	0.9446
A → S↑	0.1028	0.1108	2.6719	1.3712
A → S↓	0.1367	0.1583	1.8072	0.9511
Cl → S↑	0.0820	0.0901	2.6556	1.3596
Cl → S↓	0.1260	0.1472	1.8069	0.9511
A → CON↑	0.0159	0.0157	2.7445	1.3720
A → CON↓	0.0135	0.0133	2.4373	1.2067
Cl → CON↑	0.0134	0.0130	2.6745	1.3956
Cl → CON↓	0.0124	0.0115	2.4385	1.2065

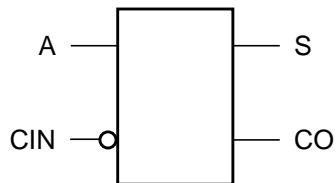
Cell Description

The AHHCIN cell is a half adder that provides the arithmetic sum (S) and carry-out (CO) of the input operand (A) with an active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

$$S = A \oplus \overline{CIN}$$

$$CO = A \bullet \overline{CIN}$$

Logic Symbol



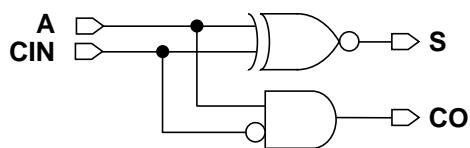
Functions

A	CIN	S	CO
0	0	1	0
0	1	0	0
1	0	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHHCINX2	2.52	4.20
AHHCINX4	2.52	5.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0116	0.0145
CIN	0.0102	0.0138

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0036	0.0043
CIN	0.0062	0.0081

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.0426	0.0416	3.4082	3.4523
A → S↓	0.0461	0.0466	2.2876	2.2812
CIN → S↑	0.0270	0.0275	3.4856	3.4838
CIN → S↓	0.0405	0.0370	2.0203	2.1399
A → CO↑	0.0337	0.0342	5.1392	2.6453
A → CO↓	0.0404	0.0373	1.5058	0.7339
CIN → CO↑	0.0244	0.0246	5.1348	2.6435
CIN → CO↓	0.0105	0.0102	1.4753	0.7306

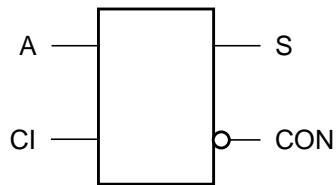
Cell Description

The AHHCON cell is a half adder that provides the arithmetic sum (S) and active-low carry-out (CON) of the input operand (A) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus CI$$

$$CON = \overline{A \bullet CI}$$

Logic Symbol



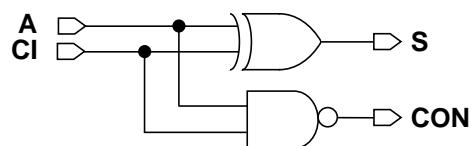
Functions

A	CI	S	CON
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHHCONX2	2.52	3.92
AHHCONX4	2.52	6.16

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
A	0.0116	0.0227
Cl	0.0071	0.0134

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0043	0.0090
Cl	0.0063	0.0115

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.0381	0.0376	3.7036	1.8472
A → S↓	0.0463	0.0434	2.3381	1.1720
Cl → S↑	0.0246	0.0256	3.6356	1.8478
Cl → S↓	0.0374	0.0348	2.2427	1.1268
A → CON↑	0.0160	0.0165	2.7629	1.3933
A → CON↓	0.0135	0.0139	2.4424	1.2248
Cl → CON↑	0.0135	0.0140	2.6841	1.3721
Cl → CON↓	0.0125	0.0127	2.4440	1.2251

Cell Description

The booth encoder block, BENC, cell performs a 2-bit multiplier recoding per a modified Booth's algorithm. Each BENC cell examines 3 bits of the multiplier (M0, M1, M2) and generates the appropriate control signals to adjust the multiplicand for subsequent partial product reduction. The outputs (S, A, X2) are represented by the logic equations:

$$A = M2 + (\overline{M0} \bullet \overline{M1})$$

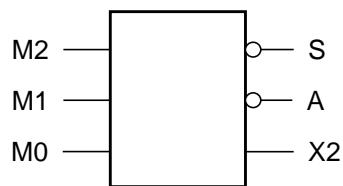
$$S = \overline{M2} + (M0 \bullet M1)$$

$$X2 = M1 \oplus M0$$

Functions

M2	M1	M0	X2	A	S
0	0	0	1	1	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

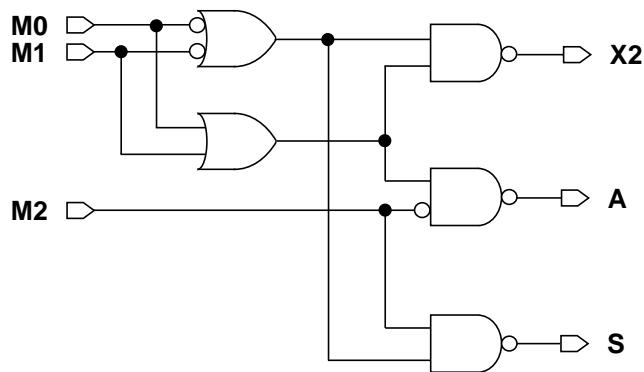
Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
BENCX1	2.52	11.20
BENCX2	2.52	14.28
BENCX4	2.52	19.04

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)		
	X1	X2	X4
M2	0.0109	0.0179	0.0313
M1	0.0195	0.0343	0.0591
M0	0.0209	0.0365	0.0611

Pin Capacitance

Pin	Capacitance (pF)		
	X1	X2	X4
M2	0.0031	0.0042	0.0044
M1	0.0043	0.0058	0.0059
M0	0.0038	0.0054	0.0054

Delays at 25°C, 1.0V, Typical Process

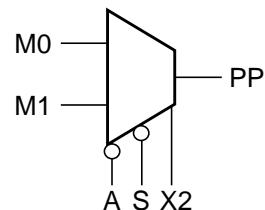
Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1	X2	X4	X1	X2	X4
M2 → A↑	0.0982	0.0929	0.1080	1.3896	0.7137	0.3635
M2 → A↓	0.0948	0.0921	0.0986	0.9083	0.4552	0.2249
M1 → A↑	0.1026	0.0978	0.1126	1.3912	0.7140	0.3635
M1 → A↓	0.0912	0.0803	0.0886	0.9135	0.4560	0.2259
M0 → A↑	0.1004	0.0946	0.1089	1.3904	0.7137	0.3635
M0 → A↓	0.0874	0.0767	0.0840	0.9109	0.4552	0.2253
M2 → S↑	0.0854	0.0812	0.0973	1.3829	0.7141	0.3635
M2 → S↓	0.0688	0.0636	0.0698	0.9077	0.4551	0.2251
M1 → S↑	0.1277	0.1220	0.1377	1.3841	0.7146	0.3636
M1 → S↓	0.1378	0.1300	0.1409	0.9137	0.4563	0.2261
M0 → S↑	0.1202	0.1101	0.1263	1.3833	0.7142	0.3635
M0 → S↓	0.1216	0.1059	0.1149	0.9105	0.4549	0.2253
M1 → X2↑	0.0899	0.0881	0.0973	1.3932	0.7202	0.3671
M1 → X2↓	0.1020	0.1062	0.1132	0.9134	0.4656	0.2290
M0 → X2↑	0.1143	0.1067	0.1182	1.3928	0.7200	0.3671
M0 → X2↓	0.1150	0.1117	0.1183	0.9132	0.4659	0.2291

Cell Description

The BMX cell performs the shifting and 2's complement inversion of the multiplicand bits (M1, M0) based on the recode control signals (X2, A, S) from the booth encoder block cell. The partial product output (PP) is represented by the logic equation:

$$PP = X2 \bullet ((M0 \bullet \bar{A}) + (\bar{M0} \bullet \bar{S})) + \bar{X2} \bullet ((M1 \bullet \bar{A}) + (\bar{M1} \bullet \bar{S}))$$

Logic Symbol



Functions¹

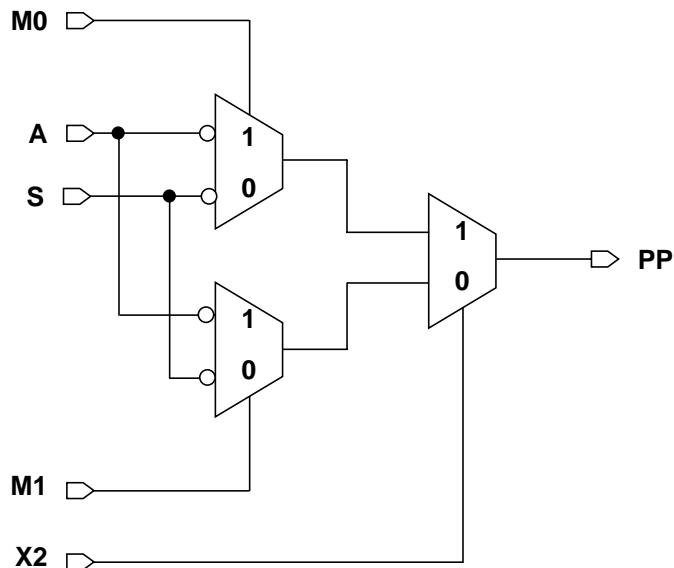
X2	A	S	M0	M1	PP
0	0	0	x	x	x
0	0	1	x	0	0
0	0	1	x	1	1
0	1	0	x	0	1
0	1	0	x	1	0
0	1	1	x	x	0
1	0	0	x	x	x
1	0	1	0	x	0
1	0	1	1	x	1
1	1	0	0	x	1
1	1	0	1	x	0
1	1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
BMXX2	2.52	7.56
BMXX4	2.52	9.80

¹ Shaded areas represent illegal conditions.

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
X2	0.0077	0.0145
M0	0.0120	0.0201
A	0.0111	0.0197
S	0.0148	0.0255
M1	0.0103	0.0179

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
X2	0.0022	0.0031
M0	0.0034	0.0035
A	0.0020	0.0039
S	0.0021	0.0040
M1	0.0028	0.0035

Delays at 25°C, 1.0V, Typical Process

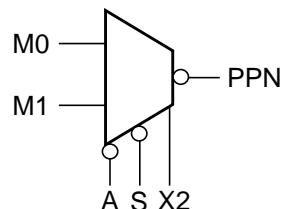
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
X2 → PP↑	0.0584	0.0585	2.6122	1.3407
X2 → PP↓	0.0521	0.0536	1.6214	0.7953
M0 → PP↑	0.0943	0.0834	2.6170	1.3415
M0 → PP↓	0.1120	0.1090	1.6248	0.7965
A → PP↑	0.1020	0.0894	2.6169	1.3420
A → PP↓	0.0970	0.0868	1.6240	0.7962
S → PP↑	0.1100	0.0993	2.6188	1.3423
S → PP↓	0.1056	0.0931	1.6261	0.7971
M1 → PP↑	0.0855	0.0831	2.6149	1.3421
M1 → PP↓	0.1030	0.1050	1.6213	0.7947

Cell Description

The BMXI cell performs the shifting and 2's complement inversion of the multiplicand bits (M1, M0) based on the recode control signals (X2, A, S) from the booth encoder block cell. The inverted partial product output (PPN) is represented by the logic equation:

$$PPN = \overline{X2} \bullet ((M0 \bullet \bar{A}) + (\bar{M0} \bullet \bar{S})) + \bar{X2} \bullet ((M1 \bullet \bar{A}) + (\bar{M1} \bullet \bar{S}))$$

Logic Symbol



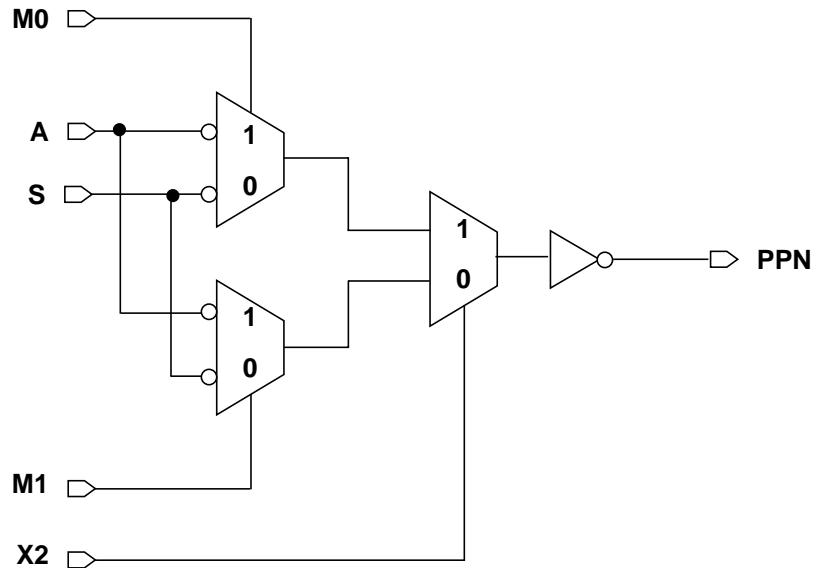
Functions¹

X2	A	S	M0	M1	PPN
0	0	0	x	x	x
0	0	1	x	0	1
0	0	1	x	1	0
0	1	0	x	0	0
0	1	0	x	1	1
0	1	1	x	x	1
1	0	0	x	x	x
1	0	1	0	x	1
1	0	1	1	x	0
1	1	0	0	x	0
1	1	0	1	x	1
1	1	1	x	x	1

Drive Strength	Height (um)	Width (um)
BMXIX2	2.52	6.72
BMXIX4	2.52	10.08

¹ Shaded areas represent illegal conditions.

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)	
	X2	X4
X2	0.0071	0.0128
M0	0.0101	0.0178
A	0.0117	0.0212
S	0.0127	0.0230
M1	0.0086	0.0156

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
X2	0.0031	0.0048
M0	0.0036	0.0055
A	0.0023	0.0045
S	0.0025	0.0045
M1	0.0031	0.0049

Delays at 25°C, 1.0V, Typical Process

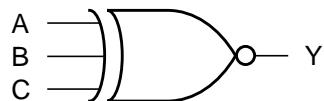
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
X2 → PPN↑	0.0649	0.0692	2.6464	1.3543
X2 → PPN↓	0.0608	0.0650	1.7713	0.8749
M0 → PPN↑	0.0833	0.0863	2.6508	1.3568
M0 → PPN↓	0.0904	0.0855	1.7681	0.8774
A → PPN↑	0.0676	0.0645	2.6482	1.3548
A → PPN↓	0.0954	0.0890	1.7845	0.8805
S → PPN↑	0.0766	0.0731	2.6512	1.3564
S → PPN↓	0.0991	0.0907	1.7873	0.8864
M1 → PPN↑	0.0815	0.0845	2.6498	1.3559
M1 → PPN↓	0.0827	0.0782	1.7568	0.8791

Cell Description

The XNOR3 cell provides a logical EXCLUSIVE NOR of three inputs (A, B, C). The output (Y) is represented by the following equation:

$$Y = \overline{A \oplus B \oplus C}$$

Logic Symbol



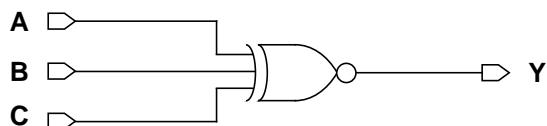
Functions

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR3XL	2.52	4.76
XNOR3X1	2.52	5.32
XNOR3X2	2.52	5.32
XNOR3X4	2.52	6.16

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)			
	XL	X1	X2	X4
A	0.0121	0.0149	0.0174	0.0251
B	0.0100	0.0119	0.0138	0.0213
C	0.0052	0.0062	0.0077	0.0106

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0019	0.0024	0.0024	0.0024
B	0.0020	0.0023	0.0024	0.0024
C	0.0018	0.0018	0.0021	0.0021

Delays at 25°C, 1.0V, Typical Process

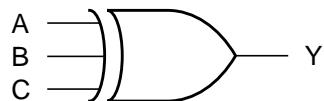
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.1237	0.1112	0.1086	0.1233	5.6708	3.5944	2.6226	1.3846
A → Y↓	0.1419	0.1291	0.1186	0.1389	5.0278	3.2310	1.7408	0.9484
B → Y↑	0.1060	0.0968	0.1017	0.1202	5.6691	3.6574	2.6697	1.3840
B → Y↓	0.1429	0.1311	0.1186	0.1279	5.0284	3.2309	1.5947	0.9480
C → Y↑	0.0598	0.0635	0.0652	0.0751	5.7154	3.6341	2.6589	1.3794
C → Y↓	0.0678	0.0608	0.0502	0.0634	5.0212	3.2276	1.7146	0.9082

Cell Description

The XOR3 cell provides a logical EXCLUSIVE OR of three inputs (A, B, C). The output (Y) is represented by the following equation:

$$Y = A \oplus B \oplus C$$

Logic Symbol



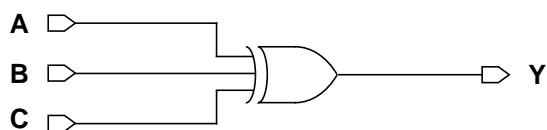
Functions

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XOR3XL	2.52	4.76
XOR3X1	2.52	5.32
XOR3X2	2.52	5.32
XOR3X4	2.52	6.16

Functional Schematic



AC Power

Pin	Power (μ W/MHz)			
	XL	X1	X2	X4
A	0.0128	0.0156	0.0180	0.0259
B	0.0100	0.0117	0.0140	0.0221
C	0.0053	0.0064	0.0077	0.0103

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0019	0.0024	0.0024	0.0024
B	0.0020	0.0023	0.0025	0.0025
C	0.0028	0.0030	0.0034	0.0035

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.1258	0.1119	0.1102	0.1221	5.7006	3.5987	2.6260	1.3847
A → Y↓	0.1399	0.1273	0.1178	0.1398	5.0138	3.2385	1.7646	0.9503
B → Y↑	0.1080	0.0973	0.1010	0.1194	5.6994	3.6126	2.6754	1.3840
B → Y↓	0.1416	0.1302	0.1179	0.1289	5.0127	3.2392	1.6179	0.9500
C → Y↑	0.0733	0.0705	0.0590	0.0602	5.6722	3.5896	2.6213	1.3395
C → Y↓	0.0663	0.0599	0.0561	0.0664	4.9734	3.2210	1.7598	0.9282

Advanced Arithmetic Cells

Cell Description

The CMPR42 cell takes in 4 bits of the partial product (A, B, C, D) and compresses them into 2-bits of partial product (S, CO). The cell requires an intermediate carry-in input (ICI) from the n-1 compressor and an intermediate carry-out output (CO) to the n+1 compressor. The CMPR42 cell also contains an internal sum IS. The internal sum IS, carry-in output (ICO), and the two outputs (S, CO) are represented by the logic equations:

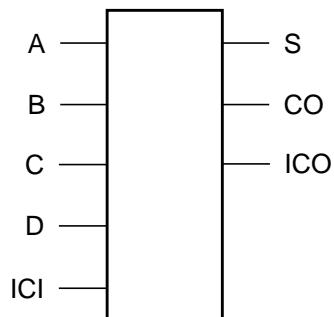
$$IS = A \oplus B \oplus C$$

$$ICO = (A \bullet B) + (A \bullet C) + (B \bullet C)$$

$$S = IS \oplus D \oplus ICI$$

$$CO = (IS \bullet D) + (IS \bullet ICI) + (D \bullet ICI)$$

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
CMPR42X1	2.52	12.88
CMPR42X2	2.52	13.44
CMPR42X4	2.52	18.48

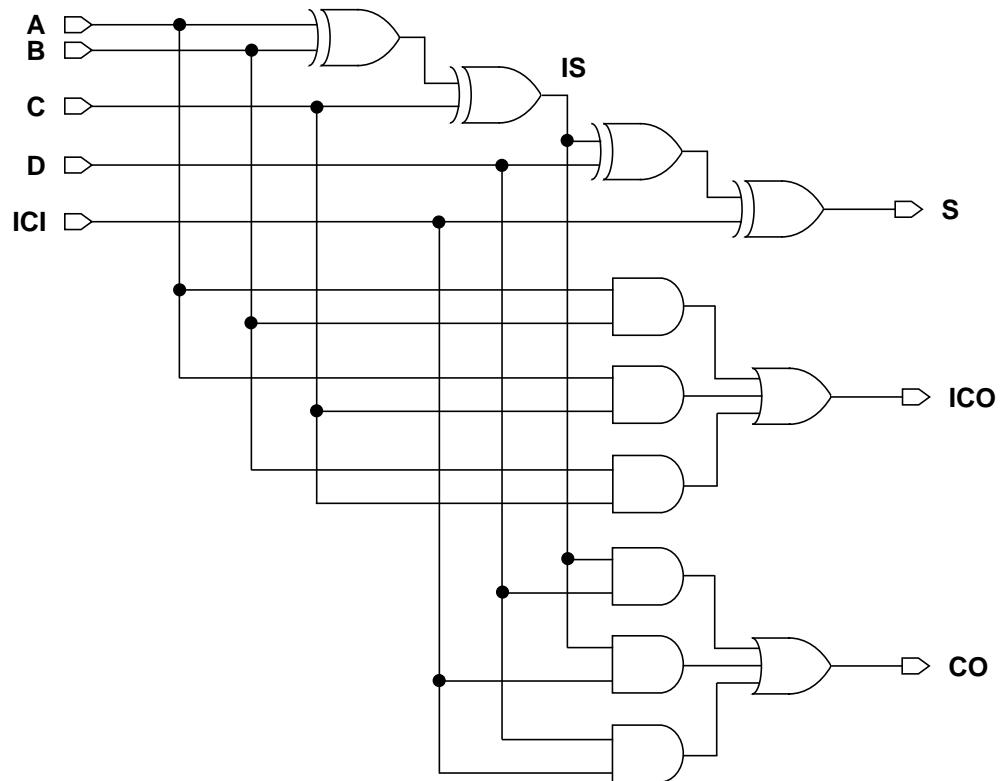
Functions

A	B	C	IS	ICO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Functions (cont.)

IS	D	ICI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)		
	X1	X2	X4
A	0.0293	0.0366	0.0566
B	0.0286	0.0356	0.0549
C	0.0264	0.0329	0.0512
D	0.0221	0.0276	0.0466
IC1	0.0116	0.0155	0.0267

Pin Capacitance

Pin	Capacitance (pF)		
	X1	X2	X4
A	0.0045	0.0055	0.0086
B	0.0052	0.0063	0.0101
C	0.0042	0.0048	0.0060
D	0.0028	0.0033	0.0032
IC1	0.0017	0.0023	0.0023

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1	X2	X4	X1	X2	X4
A → S↑	0.2391	0.2408	0.2779	3.7729	2.6762	1.3631
A → S↓	0.2942	0.2845	0.3136	3.2617	1.5906	0.7940
B → S↑	0.2034	0.1994	0.2358	3.7724	2.6760	1.3629
B → S↓	0.2585	0.2431	0.2717	3.2620	1.5905	0.7940
C → S↑	0.1792	0.1808	0.2104	3.7717	2.6752	1.3625
C → S↓	0.2349	0.2253	0.2480	3.2624	1.5907	0.7940
D → S↑	0.1628	0.1567	0.1863	3.7255	2.6606	1.3607
D → S↓	0.2002	0.1846	0.2111	3.2619	1.5905	0.7926
ICI → S↑	0.0861	0.0802	0.1054	3.7461	2.6685	1.3565
ICI → S↓	0.1051	0.0928	0.1080	3.2685	1.5929	0.7953
A → ICO↑	0.0457	0.0425	0.0413	3.6279	2.6627	1.3608
A → ICO↓	0.0869	0.0737	0.0736	3.1802	1.5847	0.7909
B → ICO↑	0.0459	0.0425	0.0414	3.6426	2.6695	1.3642
B → ICO↓	0.0829	0.0703	0.0682	3.1813	1.5852	0.7973
C → ICO↑	0.0399	0.0376	0.0369	3.6271	2.6626	1.3607
C → ICO↓	0.0686	0.0616	0.0631	3.1921	1.6028	0.7909
A → CO↑	0.2293	0.2347	0.2741	3.5788	2.6470	1.4293
A → CO↓	0.2700	0.2662	0.3116	3.1428	1.5770	0.8203
B → CO↑	0.1997	0.2064	0.2455	3.5788	2.6471	1.4292
B → CO↓	0.2404	0.2380	0.2830	3.1426	1.5770	0.8203
C → CO↑	0.1809	0.1812	0.2225	3.5778	2.6467	1.4292
C → CO↓	0.1985	0.1918	0.2393	3.1434	1.5772	0.8203
D → CO↑	0.1506	0.1405	0.1619	3.5501	2.6350	1.4139
D → CO↓	0.1445	0.1388	0.1738	3.1175	1.5787	0.8182
ICI → CO↑	0.0467	0.0460	0.0635	3.5846	2.6477	1.4266
ICI → CO↓	0.0682	0.0621	0.0852	3.2242	1.6129	0.8608

Register File Cells

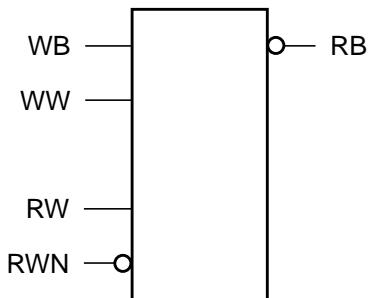
Cell Description

The RF1R1W register file cell is an active-high D-type transparent latch with an active-high tri-state output. The output (RB) is inverted.

Functions for Write Operations

WW	WB	q[n+1]
0	x	q[n]
1	0	0
1	1	1

Logic Symbol



Functions for Read Operations¹

RW	RWN	q	RB
0	0	0	1
0	0	1	Hi-Z
0	1	0	Hi-Z
0	1	1	Hi-Z
1	0	0	1
1	0	1	0
1	1	0	Hi-Z
1	1	1	0

¹ Shaded areas represent operations that are legal only during RW/ RWN transitions.

Cell Size

Drive Strength	Height (um)	Width (um)
RF1R1WX1	2.52	3.36

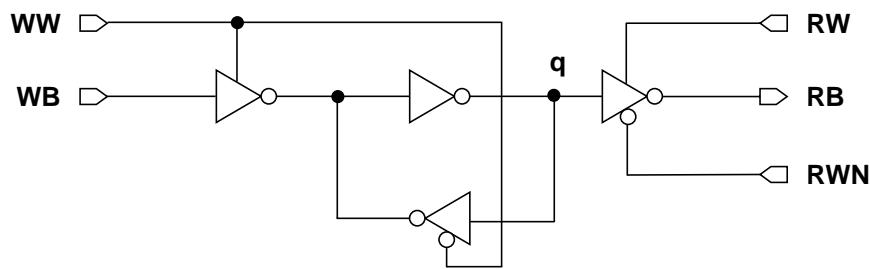
AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)
X1	
WW	0.0040
WB	0.0043
RW	0.0003
RB	0.0015

Pin Capacitance

Pin	Capacitance (pF)
X1	
WW	0.0022
WB	0.0011
RW	0.0007
RWN	0.0003
RB	0.0015

Functional Schematic



Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
WW → RB↑	0.1225	12.7051
WW → RB↓	0.0714	6.2075
WB → RB↑	0.1074	12.7049
WB → RB↓	0.0815	6.2084
RW → RB↑	0.0169	12.6927
RW → RB↓	0.0100	6.1877

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)
		X1
WW	minpwh	0.0638
WB	setup↑ → WW	0.0508
	setup↓ → WW	0.0469
	hold↑ → WW	-0.0430
	hold↓ → WW	-0.0430

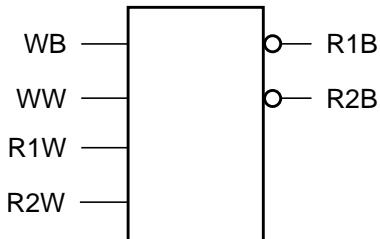
Cell Description

The RF2R1W register file cell is an active-high D-type transparent latch with two independently controlled, active-high tri-state outputs. The cell has two read ports and one write port. The outputs (R1B, R2B) are inverted.

Functions for Write Operations

WW	WB	$q[n+1]$
0	0	$q[n]$
0	1	$q[n]$
1	0	0
1	1	1

Logic Symbol



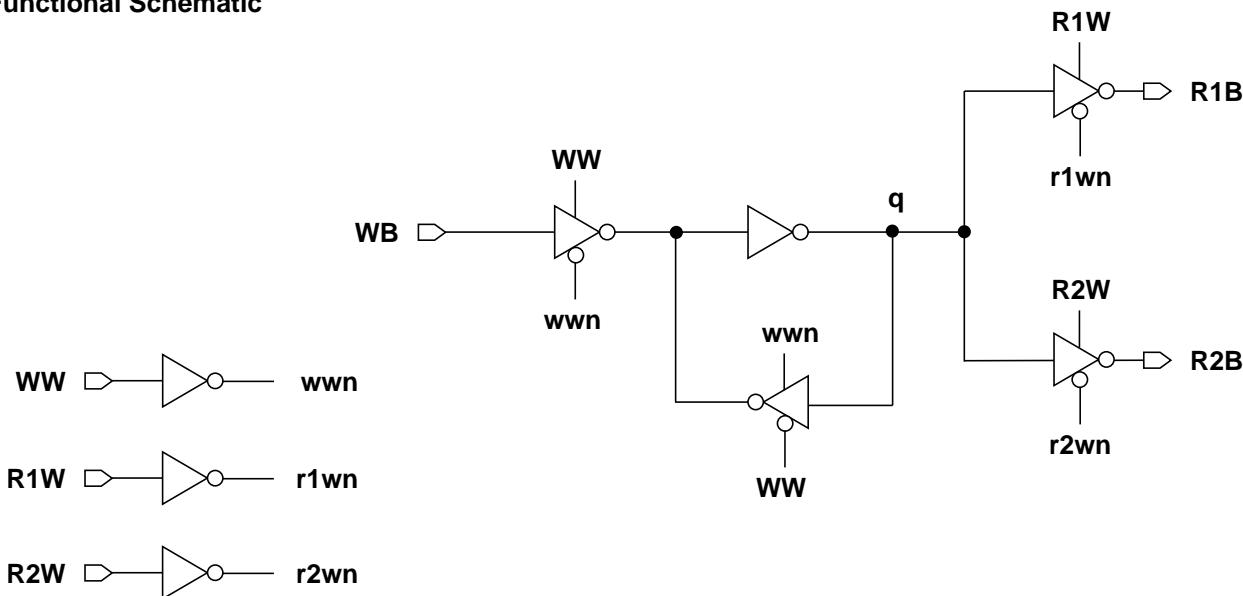
Cell Size

Drive Strength	Height (um)	Width (um)
RF2R1WX1	2.52	5.32

Functions for Read Operations

R1W/ R2W	q	R1B/ R2B
0	0	Hi-Z
0	1	Hi-Z
1	0	1
1	1	0

Functional Schematic



AC Power

Pin	Power ($\mu\text{W}/\text{MHz}$)
	X1
WB	0.0047
WW	0.0027
R1W	0.0016
R2W	0.0015
R1B	0.0073

Pin Capacitance

Pin	Capacitance (pF)
	X1
WB	0.0010
WW	0.0019
R1W	0.0014
R2W	0.0016
R1B	0.0011
R2B	0.0010

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
WB → R1B↑	0.1337	12.6915
WB → R1B↓	0.0972	6.2203
WW → R1B↑	0.1505	12.6925
WW → R1B↓	0.0892	6.2202
R1W → R1B↑	0.0354	12.6611
R1W → R1B↓	0.0090	6.1650
WB → R2B↑	0.1316	12.6033
WB → R2B↓	0.0968	6.2447
WW → R2B↑	0.1484	12.6034
WW → R2B↓	0.0888	6.2437
R2W → R2B↑	0.0345	12.5821
R2W → R2B↓	0.0087	6.1839

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)
		X1
WB	setup↑ → WW	0.0508
	setup↓ → WW	0.0664
	hold↑ → WW	-0.0430
	hold↓ → WW	-0.0547
WW	minpwh	0.0833