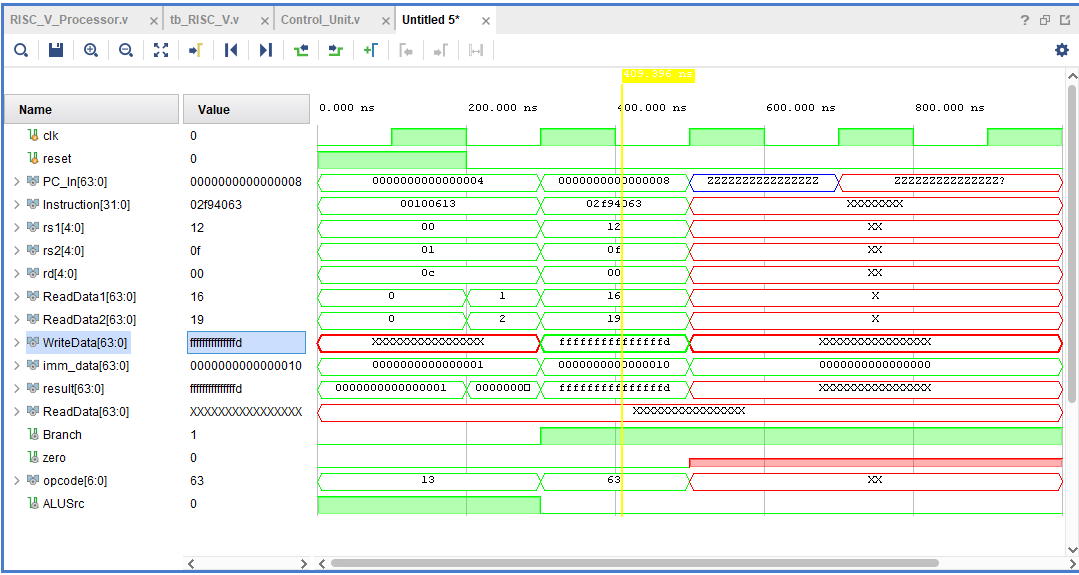
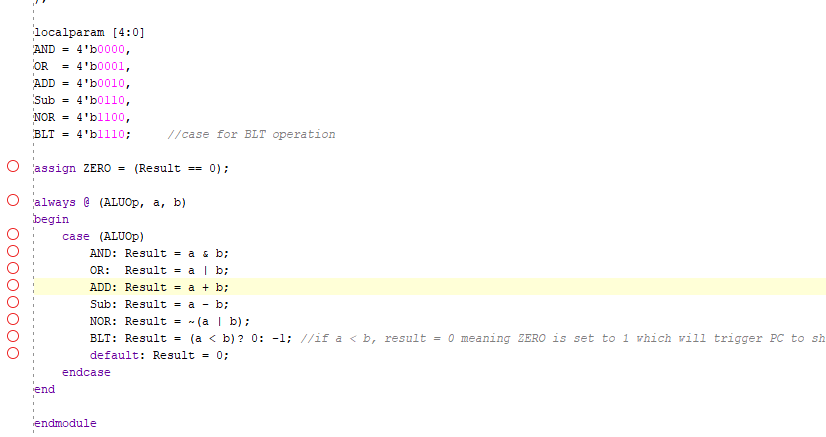
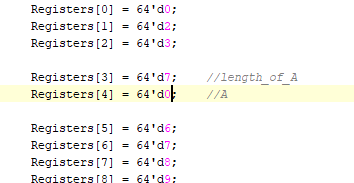
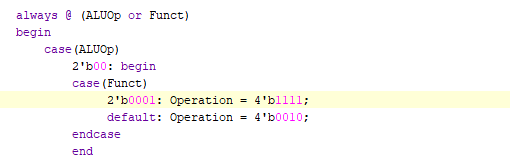
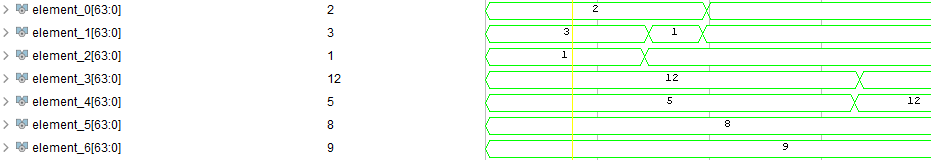
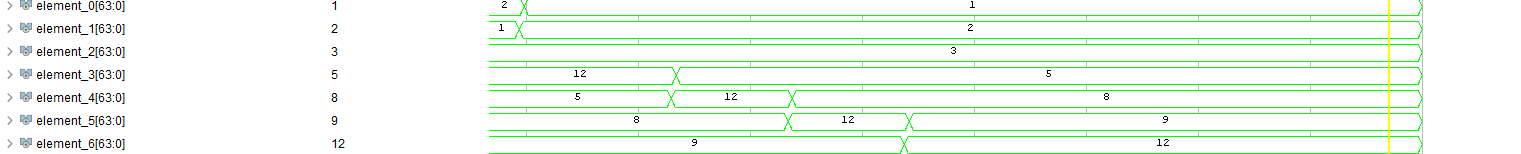
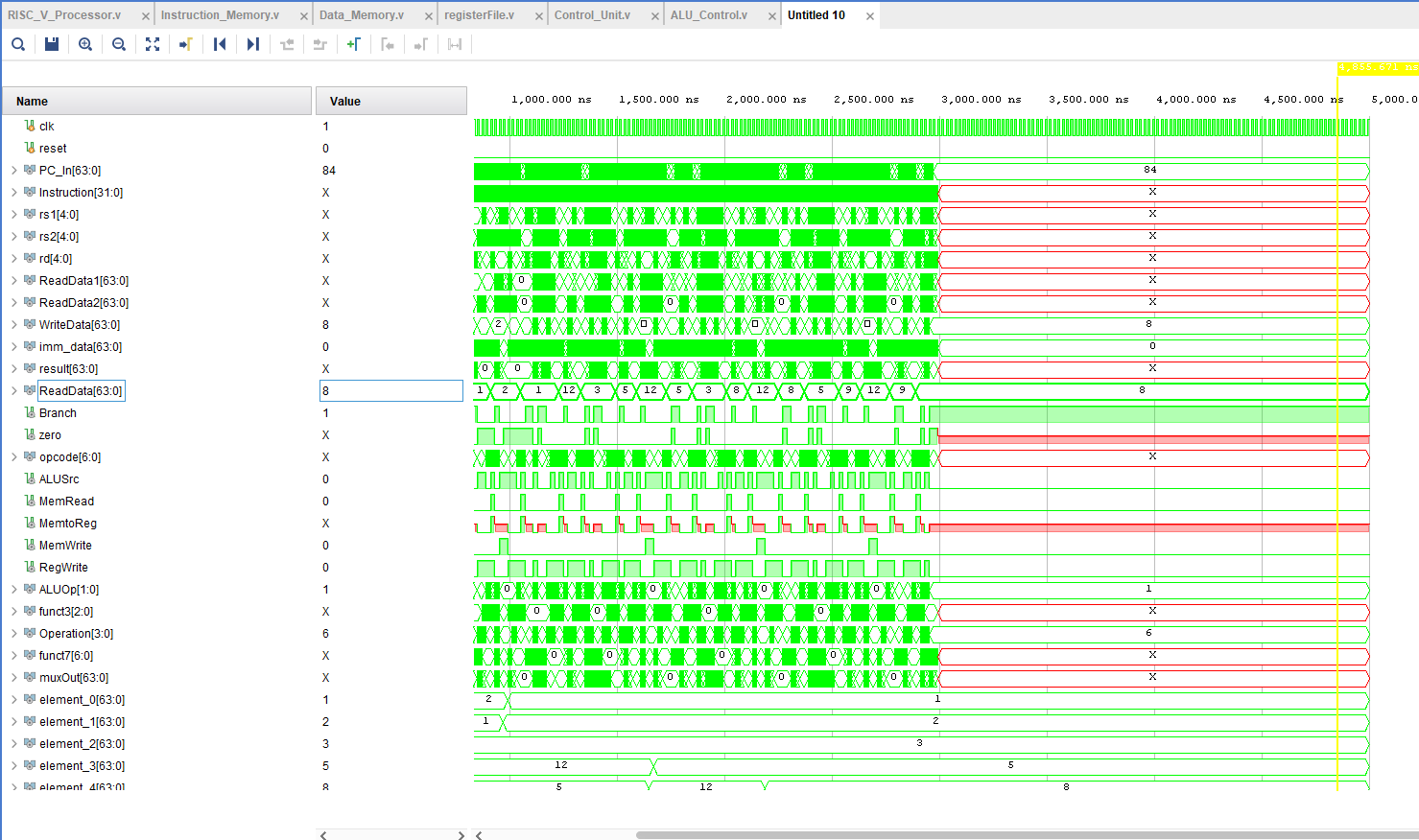
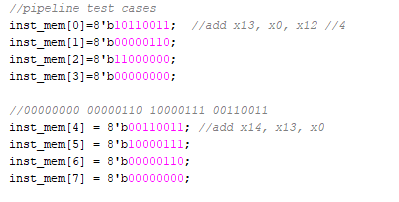
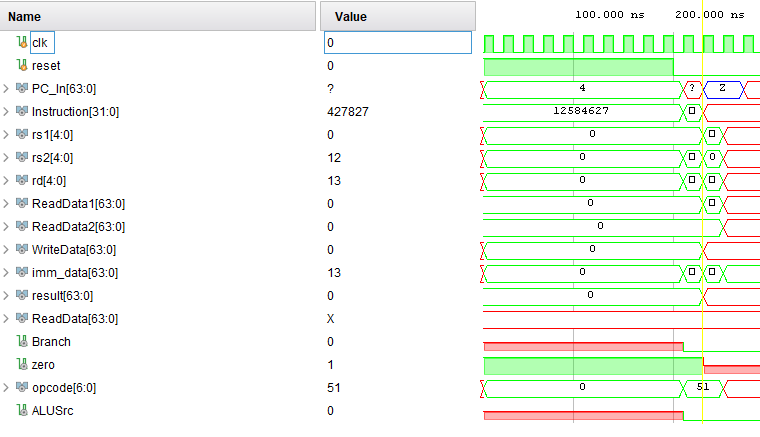
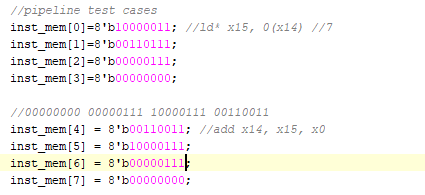
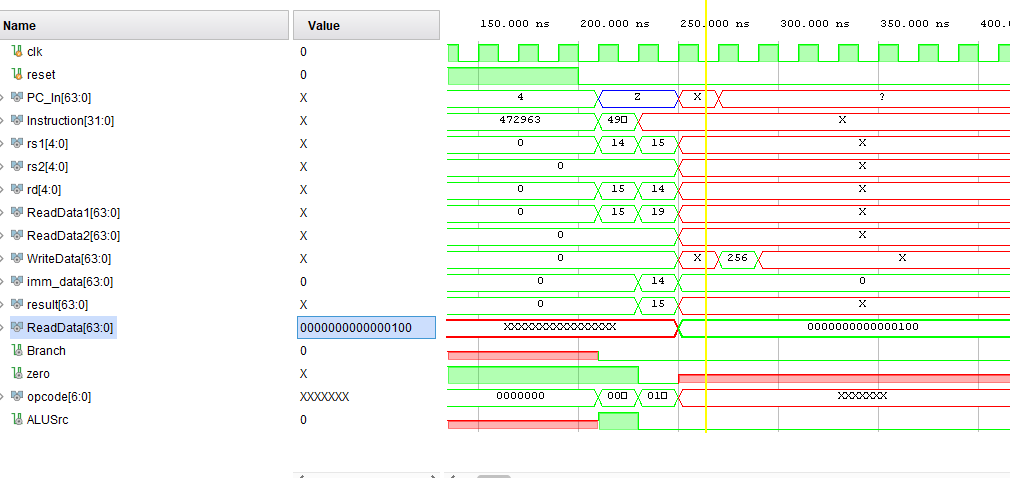
**Task 1**

* Will have to go back to using 8 bits for each entry of instruction and data memory.
* Need to find an alternative to blt or implement it in Verilog
* This is what I did:
* Got chat gpt to convert 32 bit instructions to 8 bit.
* Issues with PC\_In because of blt instruction



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* No slli support so I made it myself:
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**Task 2**

* Testcase1 (add-add):
* ****
* ****
* Load use data hazard:
* ****
* ****