ECE 3300L.02 Lab 8

Group H
Mohamed Hamida
Sherwin Sathish

Lab Objective

- Create ALU along with barrel shifter with verilog
- Switch between different “profile”, between ASM (addition subtraction multiplication) and barrel shifter using a button and FSM
- Display on 7seg display
- Use clock manager to control frequency
- Top file to combine it all together

Code Breakdown

- SEGDRIVE.v
  - File to drive the 7 segment display
- UPDOWN.v
  - File to manage counting up and down using switches
- BARSHI.v
  - Barrel shifter
- ALU
  - Arithmetic Logic Unit
- FSM
  - FInite State Machine used for controlling “profile” or state of use
- CLKMANAGER.v
  - FIles to create artificial clock
- Top.v
  - File used to bring it all together and link inputs and outputs
- lab8.xdc
  - XDC file used to manage hardware connections to Nexys A7 board

Challenges

- Our biggest challenge was creating the barrel shifter, figuring out how to “cascade” it was difficult. We were trying to use the general way of building it but we eventually decided to hardcode the values in due to time constraints

Contribution

7seg driver - Mohamed Hamida

Up-Down Counter - Sherwin Sathish

Clock Manager - Mohamed Hamida & Sherwin Sathish

Top FIle - Mohamed Hamida and Sherwin Sathish

FSM - Sherwin Sathish

ALU - Sherwin Sathish and Mohamed Hamida

UPDOWN - Sherwin Sathish

Lab Report - Sherwin Sathish

Powerpoint Slides - Mohamed Hamida

Demonstration - Sherwin Sathish

Project compiling and uploading - Mohamed Hamida