ECE 3300L.02 Lab 1

Group H
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Lab Objective

- Using gate-level modeling, design a 2x4 decoder (including enable) using Verilog
- Then, make the circuit flexible enough to run different configurations of decoders including a 3x8 and 4x16.
- Generate testbenches to verify that the 2x4, 3x8, and 4x16 decoders work as planned as well as test for various corner cases.
- Lastly, we run the synthesis on a Nexys A7 FGPA board.

Code Breakdown

- Code is broken down into 4 different files.
- We have the original 2x4 decoder file named DECO.v with its corresponding simulation testbench file named DECO_tb.v
- We also have the more flexible decoder files named GenericDECO.v with its corresponding simulation testbench file named GenericDECO_tb.v

Contribution

2x4 decoder and testbench - Mohamed Hamida

3x8 and 4x16 decoder - Sherwin Sathish

Lab Report - Sherwin Sathish and Mohamed Hamida

Powerpoint Slides - Mohamed Hamida

Demonstration Video - Sherwin Sathish

Challenges

- Our biggest challenge during the lab was figuring out the more generic decoder. We initially made the mistake of trying to accomplish a completely modular, flexible system which was nearly impossible using the gate-level modeling system. We bypassed this challenging by using the behavioural modeling method and aiming for a less flexible system.