ECE 3300L.02 Lab 10

Group H
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Code Breakdown

- SEGDRIVE.v - File to drive the 7 segment display
- UPCOUNT.v - File to manage counting up and down using switches
- CLKMANAGER.v - FIles to create artificial clock
- Top.v - File used to bring it all together and link inputs and outputs
- Bin2bcd.v - File used to convert from binary to bcd using the double dabble algorithm.
- Pwm.v - PWM module controller
- FSM - FInite State Machine used for controlling “profile” or state of use
- Lab10.xdc - XDC file used to manage hardware connections to Nexys A7 board
- Comparator.v - Compares two values and outputs boolean number
- Debounce.v - debounces the input signal

Challenges

- Our biggest issue in this lab was figuring the serializer out, thankfully with the use of a few tutorials and professor’s guidance we were able to figure it out

Contribution

7seg driver - Mohamed Hamida

UpCounter - Sherwin Sathish

Clock Manager - Mohamed Hamida & Sherwin Sathish

Binary to BCD Converter - Mohamed Hamida

Top FIle - Mohamed Hamida and Sherwin Sathish

Load Functionality - Sherwin Sathish

Lab Report - Sherwin Sathish

Powerpoint Slides - Mohamed Hamida

Demonstration - Sherwin Sathish

Project compiling and uploading - Mohamed Hamida