ECE 3300L.02 Lab 3

Group H
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Lab Objective

- Create a clock manager that creates artificial clock signals and sends them off to the UP-DOWN counter and 7seg driver
- Create an UP-DOWN that automatically iterates from 0 to 9 using switches.
- Create 7 segment display driver to take signal from UP-DOWN counter to demonstrate values on the 7 segment display

Code Breakdown

- SEGDRIVE.v
  - File to drive the 7 segment display
- UPDOWN.v
  - File to manage counting up and down using switches
- CLKMANAGER.v
  - FIles to create artificial clock
- Top.v
  - File used to bring it all together and link inputs and outputs
- Segnew.xdc
  - XDC file used to manage hardware connections to Nexys A7 board

Challenges

- Our biggest challenge this lab was figuring out the clock manager, we had difficulty conceptualizing what the 32 different combinations should do with the 5 different switches.
- Our other big issue was trying to debut the 7seg driver code

Contribution

7seg driver - Mohamed Hamida & Sherwin Sathish

Up-Down Counter - Sherwin Sathish

Clock Manager - Mohamed Hamida & Sherwin Sathish

Top FIle - Mohamed Hamida and Sherwin Sathish

Testbench Simulations - Sherwin Sathish

Lab Report - Sherwin Sathish

Demonstration Video - Mohamed Hamida and Sherwin Sathish

Powerpoint Slides - Mohamed Hamida

Project compiling and uploading - Mohamed Hamida