ECE 3300L.02 Lab 2

Group H
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Lab Objective

- Create a clock manager that creates artificial clock signals and sends them off to the UP counter and 7seg driver
- Create an UP that automatically iterates from 0 to 99 using switches to dictate frequency along with reset and enable switch.
- Create 7 segment display driver to take signal from UP counter to demonstrate values on the 7 segment display using 2 different anode displays

Code Breakdown

- seg7driver.v
  - File to drive the 7 segment display using multiple displays
- upcounter.v
  - File to manage counting up using switches to dictate frequency
- clkmanager.v
  - FIles to create artificial clock
- top.v
  - File used to bring it all together and link inputs and outputs
- constraints.xdc
  - XDC file used to manage hardware connections to Nexys A7 board

Challenges

- During this lab our biggest challenge was figuring out the specifics of the 7segdriver. We were tasked with creating a more generic 7segdriver which proved to be difficult because of the concept of anode and cathode and timing. Luckily with the help of the Professor and the Digilent documentation, we were able to prevail and figure out how to make a generic 7segdriver.

Contribution

7seg driver - Mohamed Hamida & Sherwin Sathish

Up Counter - Sherwin Sathish

Clock Manager - Mohamed Hamida & Sherwin Sathish

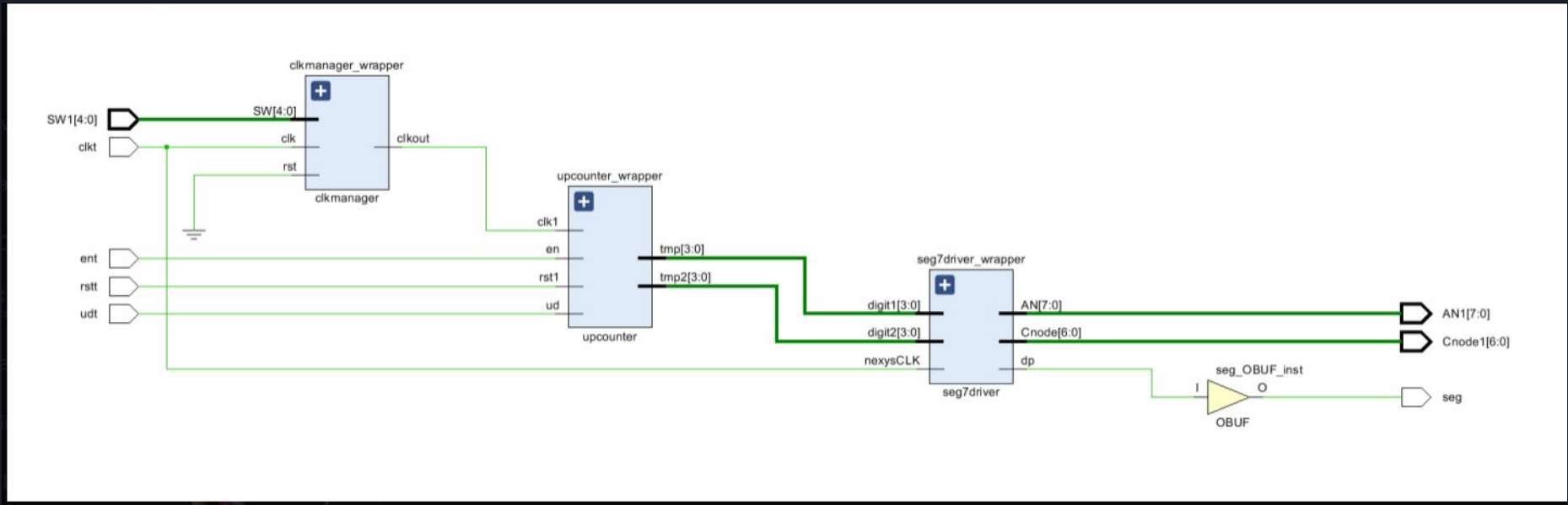
Top FIle - Mohamed Hamida and Sherwin Sathish

Demonstration Video - Mohamed Hamida and Sherwin Sathish

Powerpoint Slides - Mohamed Hamida and Sherwin Sathish

Project compiling and uploading - Mohamed Hamida

Schematic


clkmanager_wrapper
SW1[4:0]
clkt
SW[4:0]
clk
rst
clkout
clkmanager
upcounter_wrapper
clk1
en
rst1
ud
tmp[3:0]
tmp2[3:0]
upcounter
ent
rstt
udt
seg7driver_wrapper
digit1[3:0]
digit2[3:0]
nexysCLK
AN[7:0]
Cnode[6:0]
dp
seg7driver
AN1[7:0]
Cnode1[6:0]
seg_OBUF_inst
I
O
OBUF
seg