ECE 3300L.02 Lab 2

Group H
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Lab Objective

- Utilize majority decoder to modularize full adder by separating Cout from Sum aspect of full adder
- Build full adder with using majority decoder
- Build n-bit full adder using the modular full adder. Completely flexible
- Demonstrate use with testbench
- Demonstrate use with Nexys A7 FGPA

Code Breakdown

- Code is broken down into 6 different files.
- We have the original majority decoder file named MAJORITY.v with its corresponding simulation testbench file named MAJORITY_tb.v
- We also have the Full Adder node file named FA.v with its corresponding simulation testbench file named FA_tb.v
- We finally have the n-bit full adder built from the Full Adder node named FAnbit.v and it’s corresponding testbench file named FAnbit_tb.v

Challenges

- Thankfully this time around we didn't have much challenges with help from Professor Aly. At the beginning, it was difficult understanding the purpose of the majority decoder and how it came into play when using the Full Adder and n-bit full adder. Other than that, Professor Aly went through the full adder and n-bit full adder code in class so it was quite simple to follow.

Contribution

Verilog Code Writing - Sherwin Sathish

Lab Report - Sherwin Sathish

Powerpoint Slides - Mohamed Hamida

Hardware Demonstration - Mohamed Hamida

Software Demonstration - Sherwin Sathish

Project compiling and uploading - Mohamed Hamida