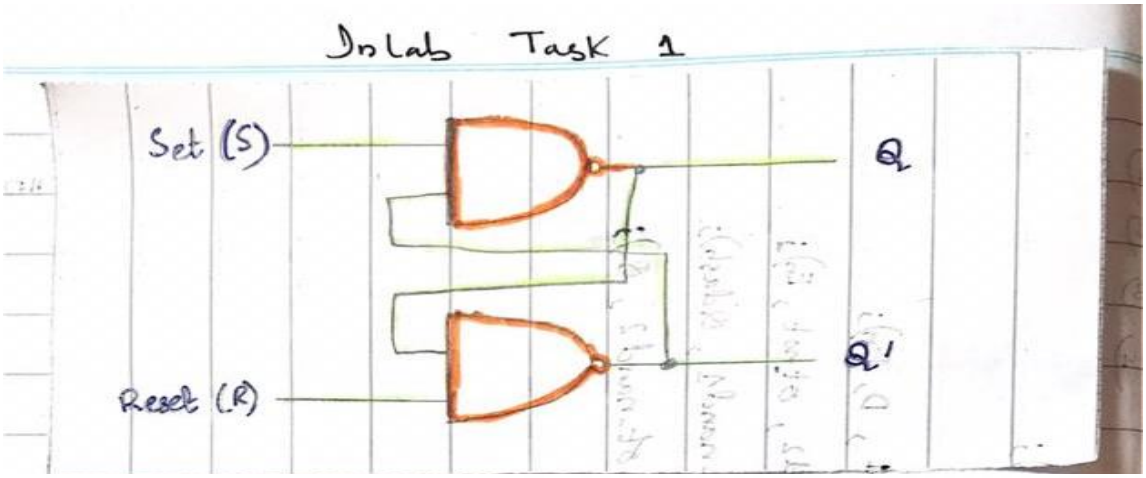
Computer Organization and Architecture

In-Lab

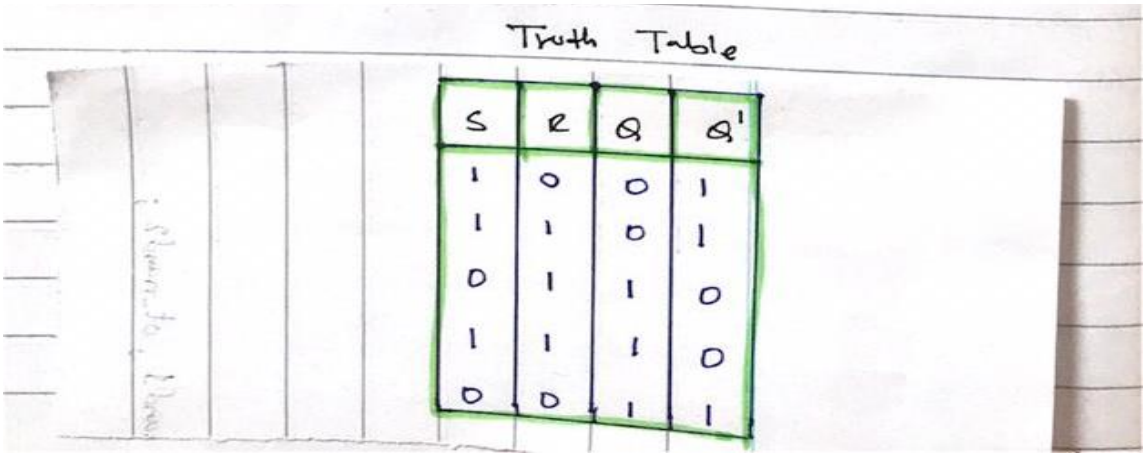
Lab 06

Group Members Name & Reg #:	**Muhammad Haris Irfan** **(FA18-BCE-090)**
Class	Computer Organization and Architecture CPE343(**BCE-5B**)
Instructor's Name	Dr. Adeel Israr

Inlab: Task 1 (1)

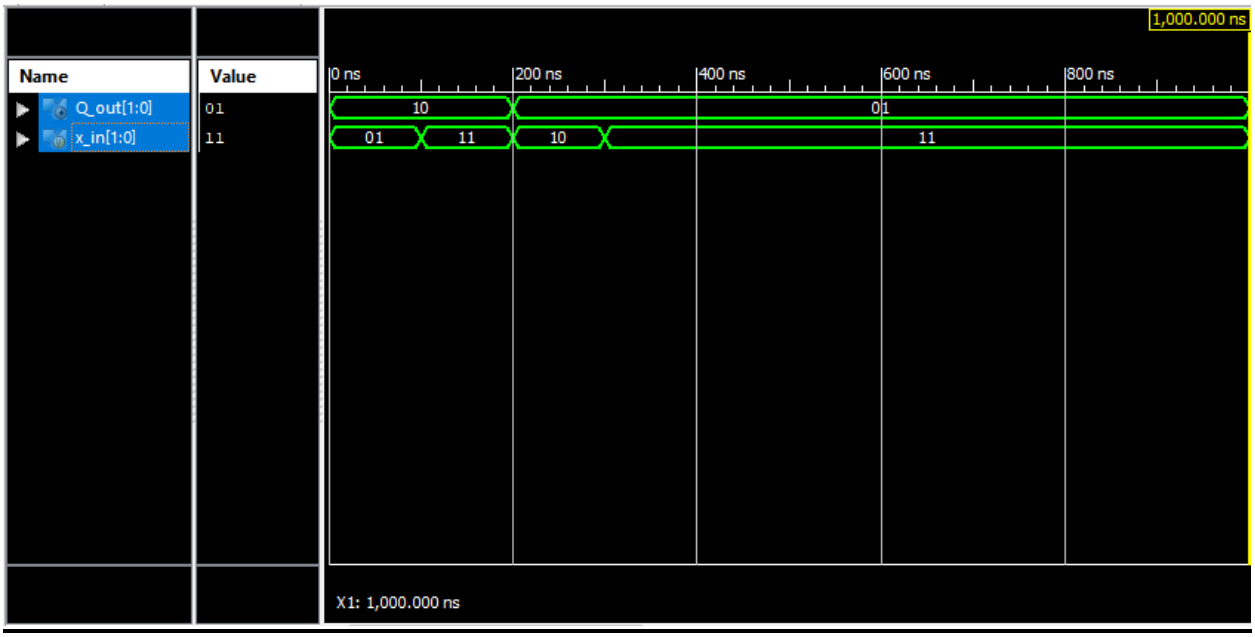



```
mode    SRLATCH continuous ( Q_out , x_in);

input   [1:0] x_in;
output  [1:0] Q_out;

assign  Q_out [0] = ~ (Q_out [1] & x_in [0]);
assign  Q_out [1] = ~ (Q_out [0] & x_in [1]);

endmodule
```

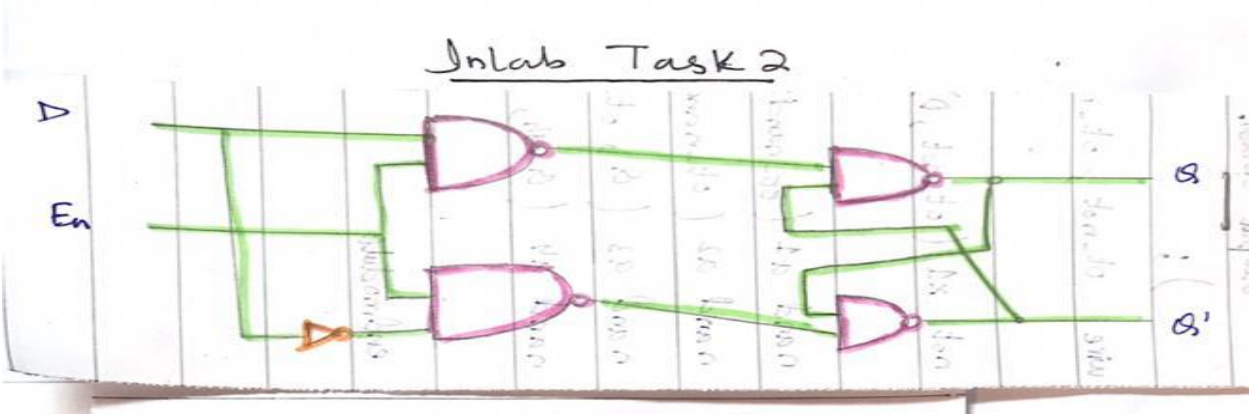


S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

Task1 Output Waveform:



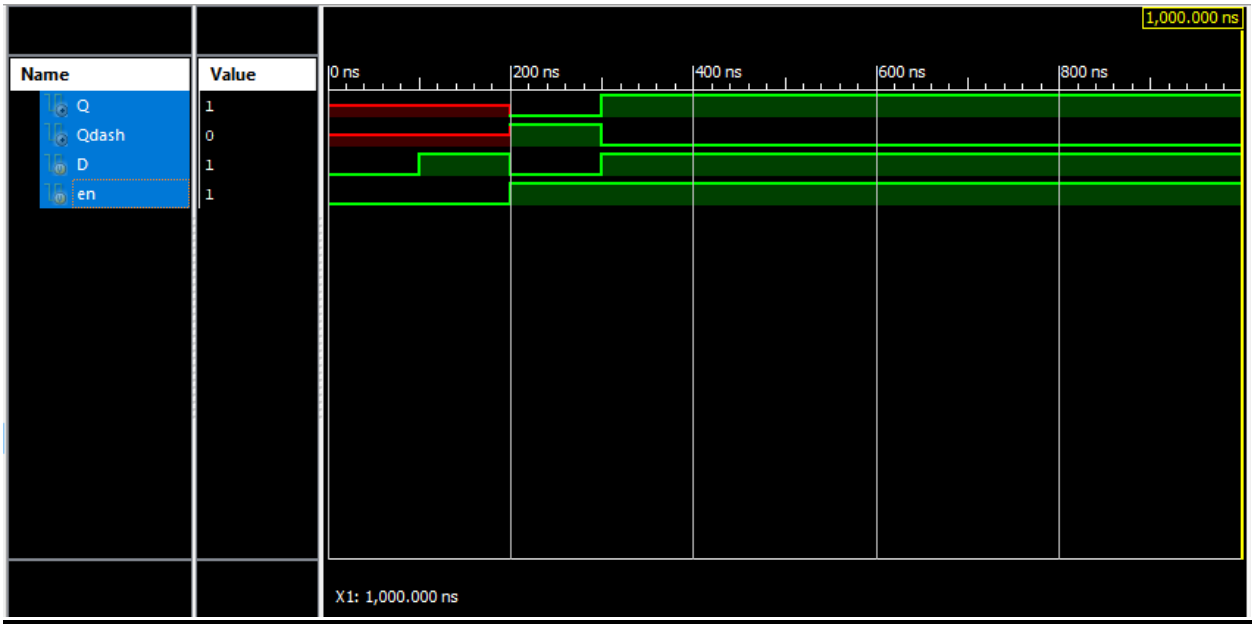
Inlab: Task 1(2)




```
module DLatchcontinuous (Q, Qdash, D, en);

    input D, en;

wire nand1 = ~ (D & en);
wire nand2 = ~ (en & ~(D));

 assign Q = ~ (nand1 & Qdash);
 assign Qdash = ~ (Q & nand2);

endmodule.
```

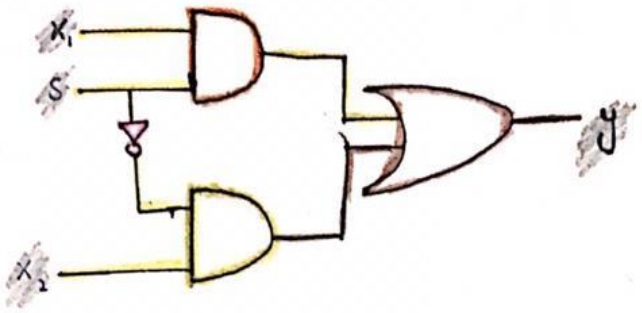
En	D	Next state of Q
0	x	No change
1	0	Q = 0
1	1	Q = 1

Task2 Waveform:



Inlab: Task 2(1)

L-06 MUX




```
module  Mux (y, s, x1, x2);
input   s, x1, x2;
output  y;
assign  y = ((~s) & x2) | (s & x1);
endmodule
```

s	x_2	x_1	y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Task2 Waveform: