Computer Organization and Architecture

Post-Lab

Lab 10

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Class	Computer Organization and Architecture CPE343(**BCE-5B**)
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Postlab:

Lab - 10 Postlab

Muhammad Haris Irfan
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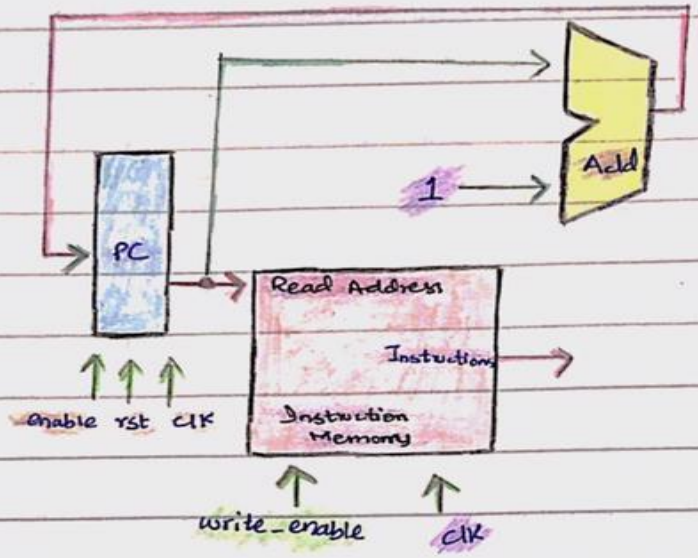

* Diagram of ciruit

```
module    get_instruction (
input     clk, reset, enable,
output    [31:0] inst );

wire      [31:0] pc ;

ProgramCounter  PC (clk, reset, enable, pc);
instruction_mem  m (pc, inst);

endmodule
```

* Code

Critical Analysis

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In this Lab, we made verilog modules for program counter, instruction memory and get instruction. In this lab we learnt about Instruction memory and the mechanism to get next instruction on every cycle of clock, we constructed a program counter which was a 32-bit register that holds the address of next instruction.

Output Waveform: