Computer Organization and Architecture

Post-Lab

Lab 08

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Class	Computer Organization and Architecture CPE343(**BCE-5B**)
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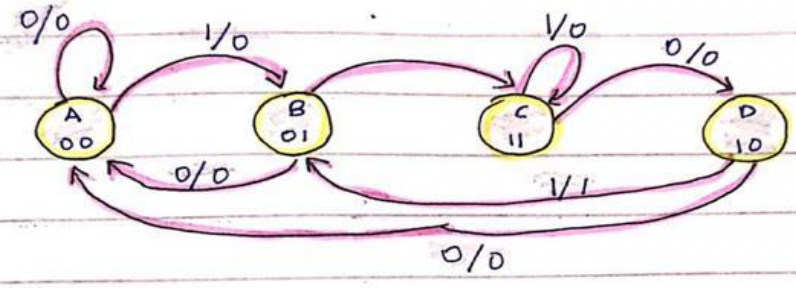
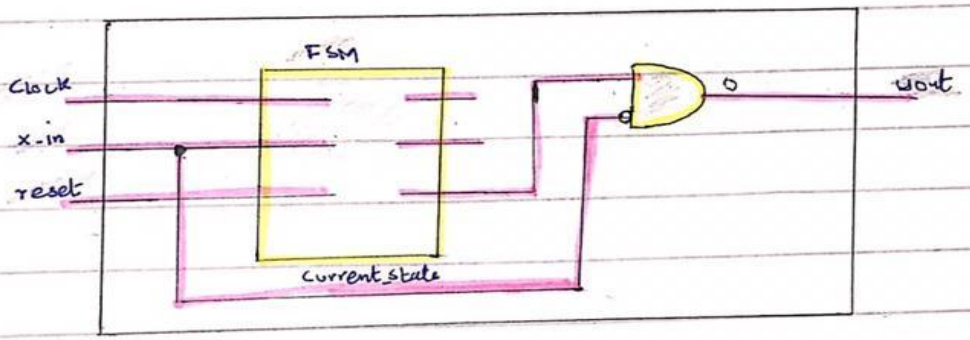
Postlab

Lab - 08 - Postlab



★ Bubble Diagram



★ Circuit Diagram.

Module Code

```
module PostLabFSM ( output reg y_out,
input x_in, clock, reset
);
reg [1:0] current state, next_state ;
parameter S0 = 2'00, S1 = 2'b01, S2= 2'b11, S3=2'10;

always @(current state , x_in)
begin
next_state = S0;
case (current state)
S0 : if (x_in)
S1 : if (x_in)
S2 : if (~x_in)
S2 : if (x_in)
S3 : if (x_in)
S3 : if (x_in)
endcase
end

always @ (posedge clock, negedge reset)
if (~reset) currentstate <= S0;
else currentstate <= next_state ;
```

```
always @ (currentstate, x_in)
case (currentstate)
S0, S1, S3 : y_out = 0;
S2 : y_out = ~x_in;
endcase

endmodule
```


Task Output Waveform: