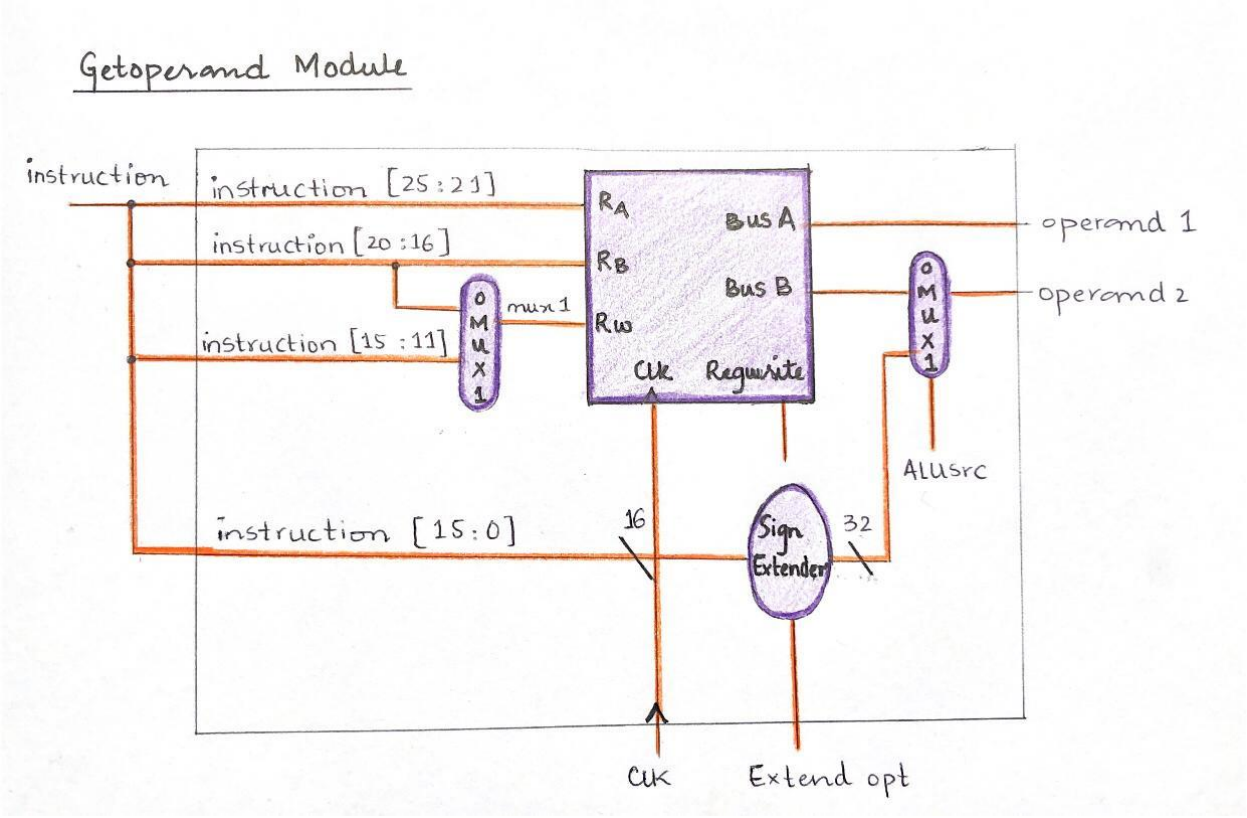
Computer Organization and Architecture

Lab 11

Group Members Name & Reg #:	**Muhammad Haris Irfan** **(FA18-BCE-090)**
Class	Computer Organization and Architecture CPE343(**BCE-5B**)
Instructor's Name	Dr. Adeel Israr

Diagram


Getoperand Module
instruction
instruction [25:21]
instruction [20:16]
instruction [15:11]
instruction [15:0]
MUX 1
mux1
RA
RB
Rw
Clk
Bus A
Bus B
Requisite
operand 1
operand 2
ALUsrc
16
Sign Extender
32
Clk
Extend opt

Code:

```
module getOperand(
output reg [31:0] operand1, operand2,
input [31:0] instruction, write_data,
input RegDst, clk, reset, extendopt, regwrite, ALUsrc
);
reg [4:0] mux1;
wire [31:0] ALUsrc, ext_out;
registerfile reg1(clock, reset, regwrite, instruction[25:21],
instruction[20:16], mux1, write_data, operanad1, ALUsrc0);
always @(*)
begin
   if (extendopt)
      extendout = {16{instructions[15]}, instruction[15:0]};
   else
      extendout = {16'd0, instruction[15:0]};
   if (RegDst)
      mux1 = instruction[15:11];
   else
      mux 1 = instruction[20:16];
  if (ALUsrc)
    operand2 = extend_out;
  else
    operand2 = ALUsrc0;
end
endmodule
```