Computer Organization and Architecture

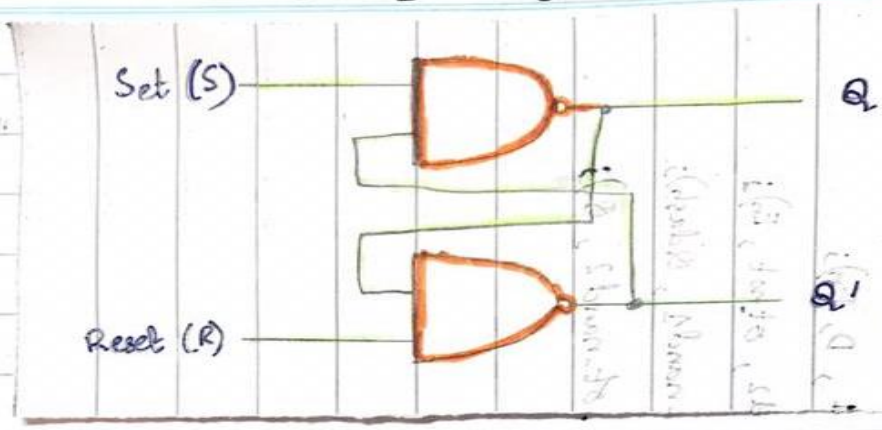
In-Lab

Lab 05

Group Members Name & Reg #:	**Muhammad Haris Irfan** **(FA18-BCE-090)**
Class	Computer Organization and Architecture CPE343(**BCE-5B**)
Instructor's Name	Dr. Adeel Israr

Inlab: Task 1

Inlab Task 1

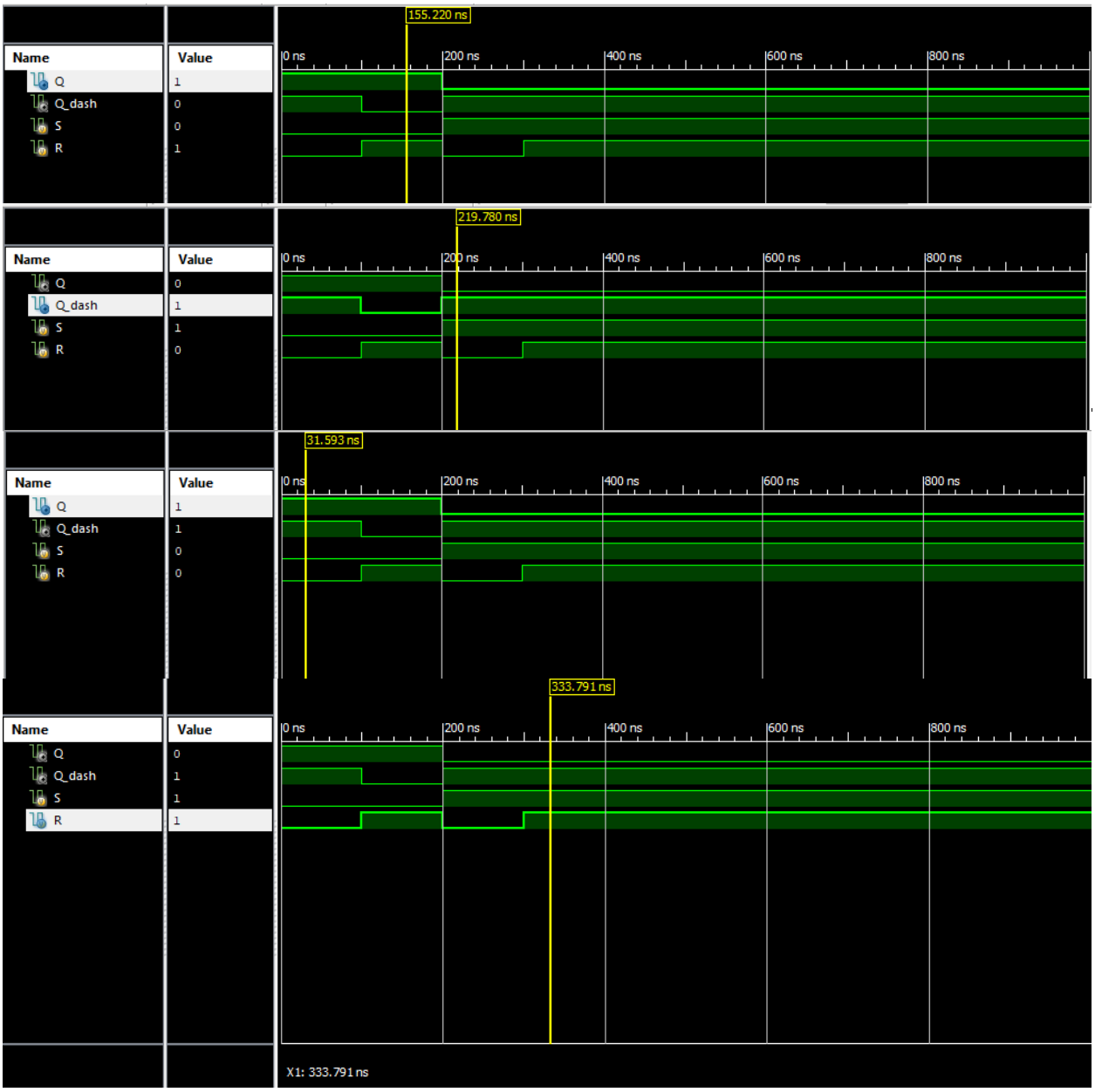



```
module NANDSRLATCH(
Output Q,
Output Q_dash,
input S,
input R
);

nand A1 (Q, S, Q_dash);
nand A2 (Q_dash, R, Q);

endmodule
```

Truth Table

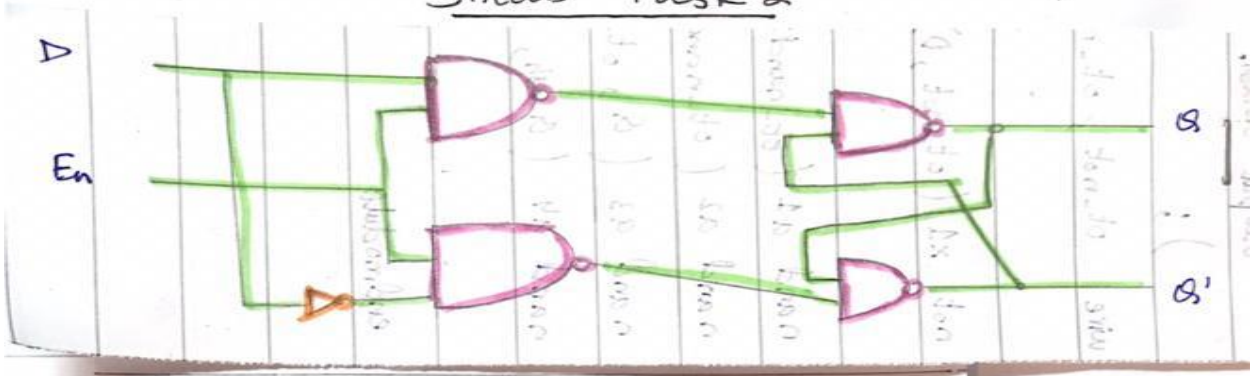
S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

Task1 Output Waveform:



Inlab: Task 2

Inlab Task 2




```
module DLatch (
input D,
input En,
output Q,
output Qdash
);

output ot_not, ot_nand1, ot_nand2;

not x1 (ot_not, D);
nand a1 (ot_nand1, D, En);
nand a2 (ot_nand2, ot_nand1, En);
nand a3 (Q, ot_nand1, Qdash);
nand a4 (Qdash, ot_nand2, Q);

end module
```

En	D	Next state of Q
0	x	No change
1	0	Q = 0
1	1	Q = 1

Task2 Waveform: