# Computer Organization and Architecture

# In-Lab

## Lab 08


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| Class | Computer Organization and Architecture CPE343(**BCE-5B**) |
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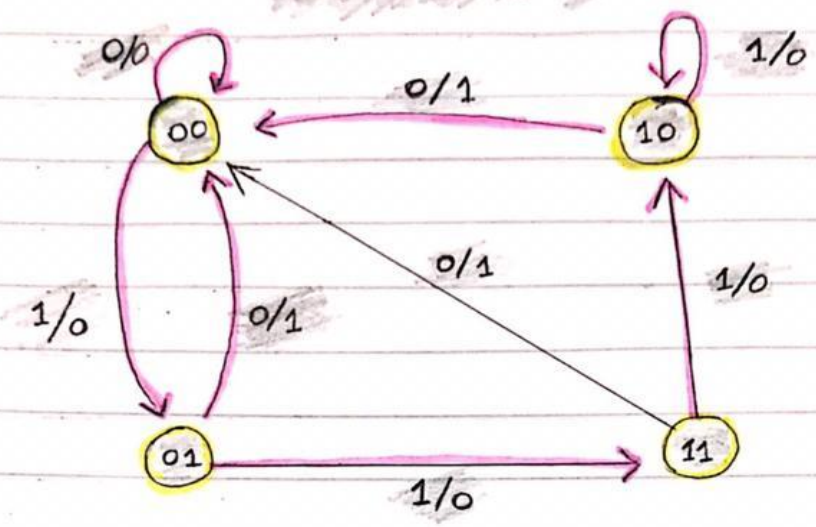
# Inlab: Task 1

## Lab - 08 Inlab




```
module MealyMachine ( output reg y_out,
  input x_in , clock , reset
  );
reg [1 :0] current state , next_state ;
parameter S0 = 2'b00, S1 = 2'b01 , S2 = 2'b10 , S3 = 2'b11 ;
always @ (current state , x_in)
  begin
   next_state = S0;
  case (current state)
 S0 : if (x_in) next_state = S1 ;
 S1 : if (x_in) next_state = S3;
 S2 : if (x_in) next_state = S2;
 S3 : if (x_in) next_state = S2 ;
 endcase
 end
```

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```
always @ ( Posedge clock, negedge reset)
  if (~reset) currentstate <= S0;
  else currentstate <= next_state ;

always @ ( currentstate , x_in)
  case ( currentstate)
  S0: y_out = 0;
  S1, S2, S3 : y_out = ~x_in;
  endcase

endmodule
```

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## Task1 Output Waveform: