

Computer Organization and Architecture

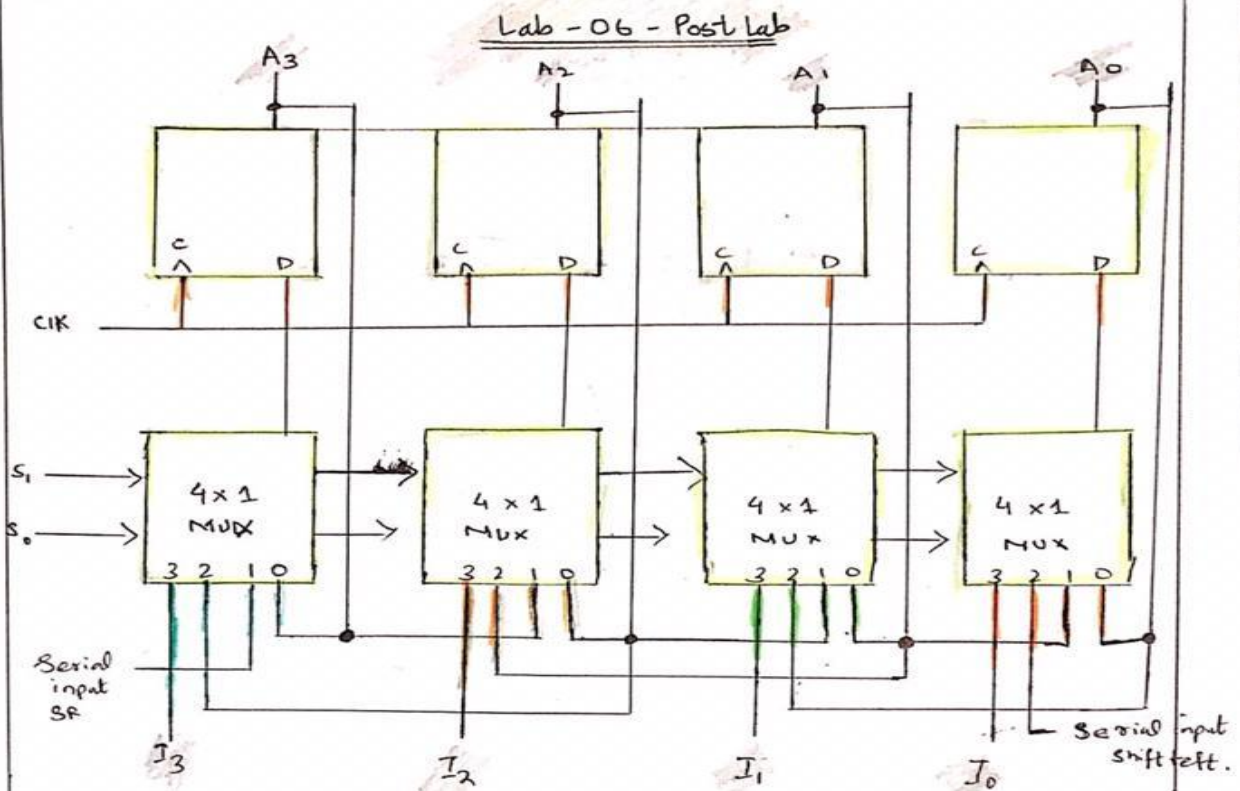
Post-Lab

Lab 06



Group Members Name & Reg #:	<u>Muhammad Haris Irfan</u> (FA18-BCE-090)
Class	Computer Organization and Architecture CPE343(BCE-5B)
Instructor's Name	Dr. Adeel Israr

Postlab



Code:

```

module UniversalSR (I[3:0], select[1:0], A[3:0], clk, se, sl);
    input [3:0] I;
    input clk;
    input [1:0] select;
    input se, sl;
    output [3:0] A;
    wire m1, m2, m3, m4;
    wire q1, q2, q3, q4;

    mux m1 (A[0], A[1], se, I[0], m1, select);
    DFF d1 (m1, clk, A[0], q1);
    mux m2 (A[1], A[2], A[0], I[1], m2, select);
    DFF d2 (m2, clk, A[1], q2);
    mux m3 (A[2], A[3], A[1], I[2], m3, select);
    DFF d3 (m3, clk, A[2], q3);

    mux m4 (A[3], sl, A[2], I[3], m4, select);
    DFF d4 (m4, clk, A[3], q4);

```

end module.

Output Waveform:

