EE 457: Digital Integrated Circuits

Project #1 Report Cover Sheet

Due: 2/28/20

PROJECT TITLE: CMOS 3-input AND Gate

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(print your name)

Your report should follow the following items in sequence. *Do not change the sequence.* Put a table of content after the cover sheet.	GRADE
Section 1: Executive Summary	/5
Section 2: Background and Approach (Include a truth table)	/5
Section 3: Electric Schematic	/15
Section 4: LTSPICE for Electric schematic	/10
Section 5: IRSIM for Electric schematic	/10
Section 6: Electric Layout	/25
Section 7: LTSPICE for Electric layout (compare with schematic)	/15
Section 8: IRSIM for Electric layout	/10
Section 9: Conclusions and References	/5
TOTAL	**/100**

Note: Do not rearrange this table. Submit your report on Blackboard.

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Executive Summary:

In this project, we will be designing a three input AND gate using Electric. In Electric, we will be creating a schematic design and a layout design. To test these designs, we will create waveforms with specific inputs and test if the output is correct using LTSPICE and IRSIM. We can then compare the waveforms of the layout and the schematic design.

To create the three input AND gate, we first made a three input NAND gate and then created an inverter. We then combined the two gates to form the NAND gate. Before combining them, we tested the output of each individual gate so that they were correct and satisfied the requirements. This also helped us avoid creating unexpected waveforms from the combined NAND gate.

For the three input NAND gate, we used three PMOS transistors in parallel and three NMOS transistors in series. To create the three parallel PMOS transistors in the layout, we had to use four P-Active areas and one N-well (which was VDD) area. To create the three series NMOS transistors, we used only two N-Active areas and one P-Well.

After trying to find a Euler path, I found that A -> B -> C works.

Background and Approach:

A three input AND gate is a logic gate that will output a HIGH is all its inputs are also HIGH. It has a Boolean expression of F = ABC.

Table 1: Truth Table of a Three Input AND Gate

Input: A	Input: B	Input: C	Output: A and B and C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

My approach was to make a NAND gate and an inverter separately and then combine them together to create the AND gate. The NAND gate has a Boolean expression of F = $\overline{A}\overline{B}\overline{C}$. So, to turn it into the expression of an AND gate, we need to pass the output of the NAND gate through an inverter to get the Boolean expression of the AND gate, F = ABC. I created the layout of the NAND gate by first drawing a OAI22 stick diagram.

The figures below show the schematic and layout of the two input NOR gate and an inverter that we plan to use for this project.

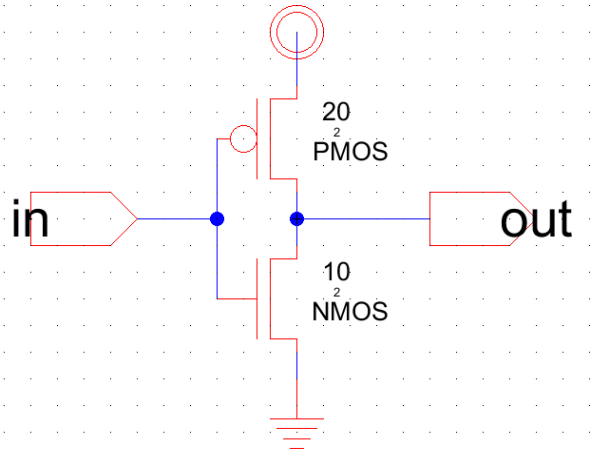

Figure 1: *Schematic Design of an Inverter Gate*

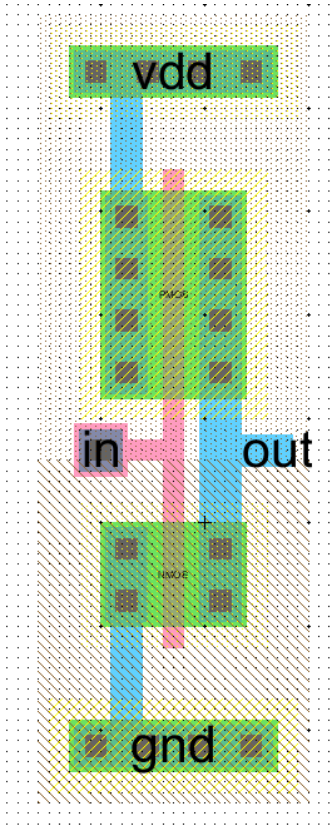

Figure 2: *Layout Design of an Inverter Gate*

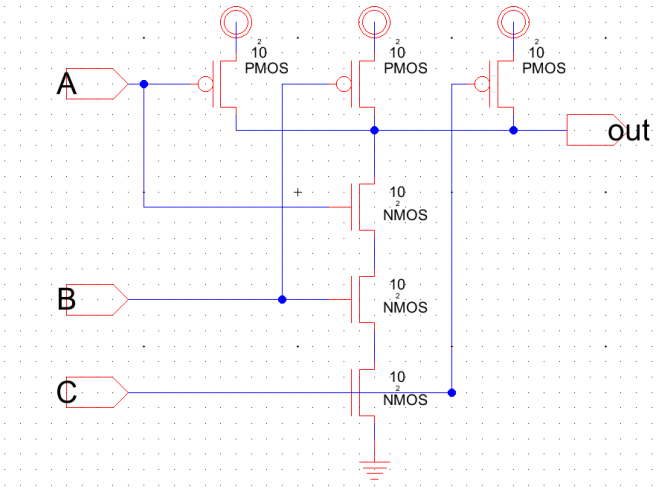

Figure 3: *Schematic Design of a Three Input NAND Gate*

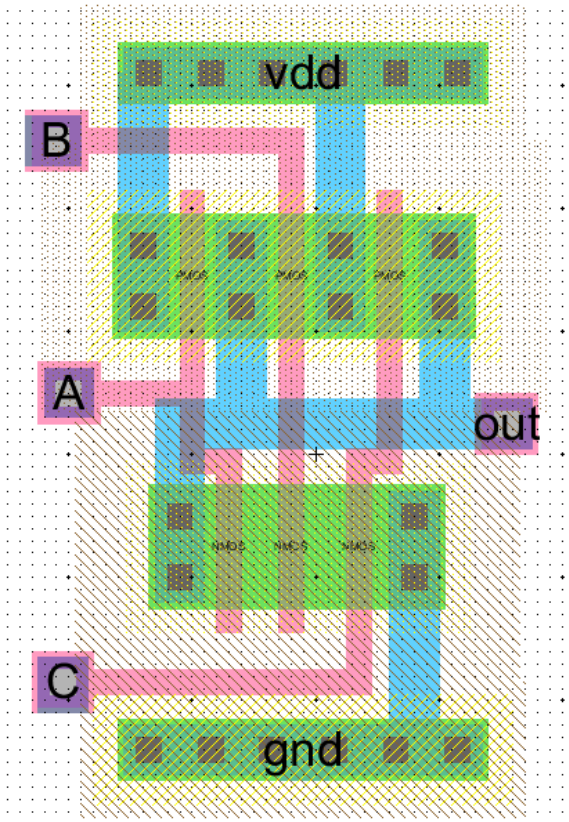

Figure 4: *Layout Design of a Three Input NAND Gate*

Electric Schematic:

I created a schematic of a three input AND gate by combining the three input NAND gate (**Figure 3**) with the inverter (**Figure 1**). I combined it by connecting the output of the three input NAND gate to the input of the inverter. In **Figure 5**, I used Electric to build the three input AND gate. **Figure 6** shows the Design Rule Check (DRC) that was performed on the schematic. This indicates if there is an error or warning in the schematic.

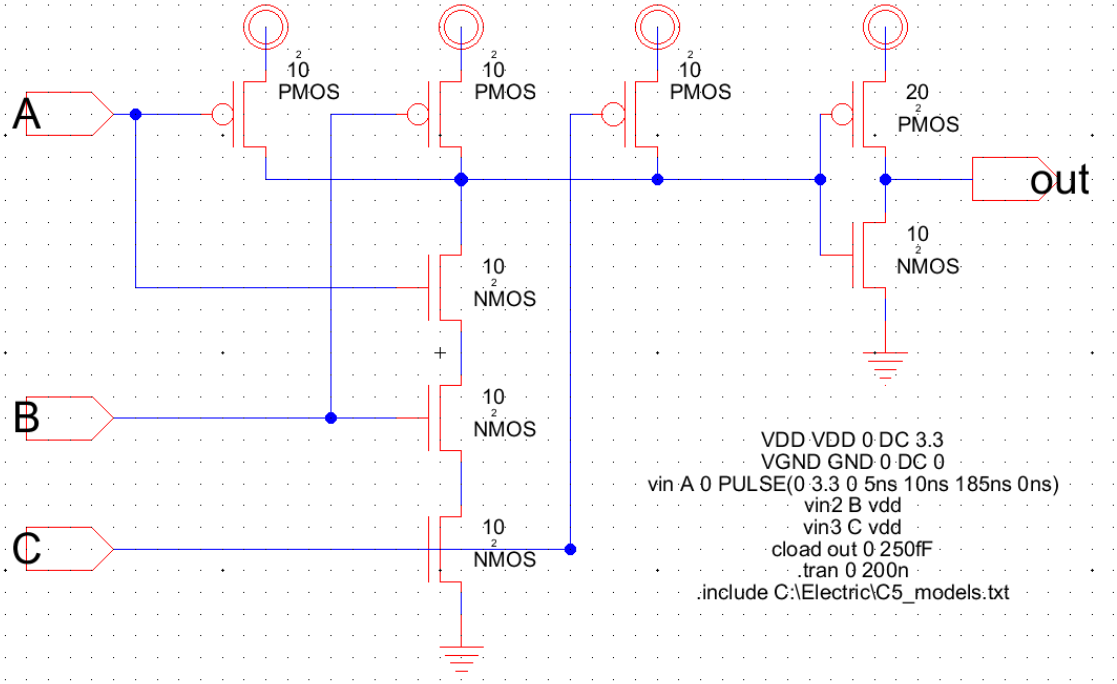

Figure 5: *Schematic Design of Three Input AND Gate*

```
================================94================================
Checking schematic cell 'AND_3{sch}'
   No errors found
0 errors and 0 warnings found (took 0.001 secs)
```

Figure 6: *Design Rule Check (DRC) of Three Input AND Gate Schematic Design*

LTSPICE for Electric Schematic:

After creating the schematics for the three input AND gate, we used LTSPICE to create the input and the output waveforms. We had to generate two different output waveforms with two different input waveforms.

We had to generate the output of an input, A, that is a 5MHz digital pulse that has a raise time of 5 nanoseconds and a fall time of 10 nanoseconds. Since the pulse is 5MHz, the period of the wave is 200 nanoseconds. Therefore, the pulse is HIGH for 185 ns. Inputs B and C were tired to VDD. The input, A, and the output, out, of this wave is shown in **Figure 7**. The spice code for this wave is shown in **Figure 9**.

We then generated the output to all possible inputs to the three input AND gate. I kept the period of input waves to 80 ns. The input and output waves and the spice code can be seen in **Figure 8** and **Figure 9**. There was some delay between the input waves and the output waves. As seen in **Figure 10**, there was about an 8-nanosecond delay between the inputs and the output. The raise time of the output, as seen in **Figure 11**, was about 3.2 nanoseconds. The fall time of the output, as seen in **Figure 12**, was about 4.5 nanoseconds. **Table 2** summarizes these finds.

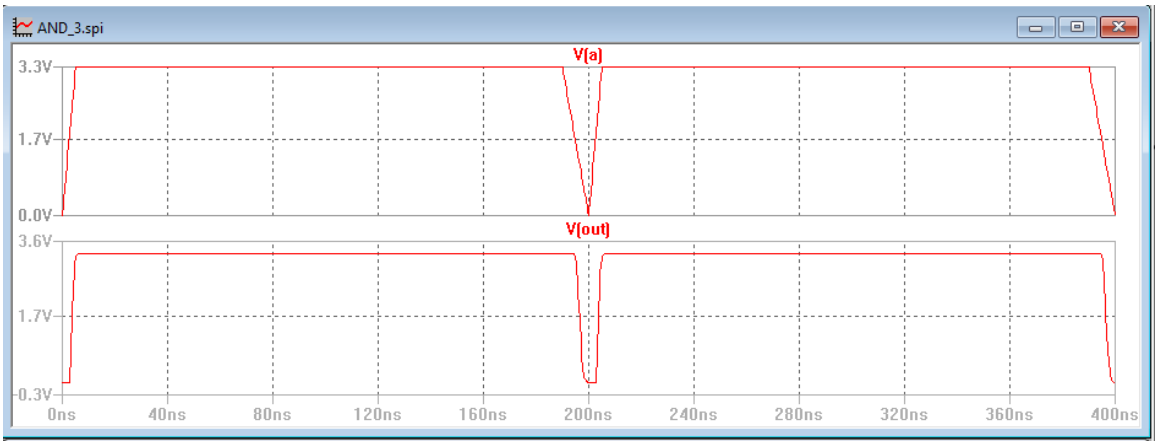

Figure 7: *LTSPICE Waveforms of Three Input AND Gate Schematic Design*

(Input A is a pulse of 200ns period, 5ns raise, 10ns fall, 0ns delay, Inputs B and C are set to HIGH)

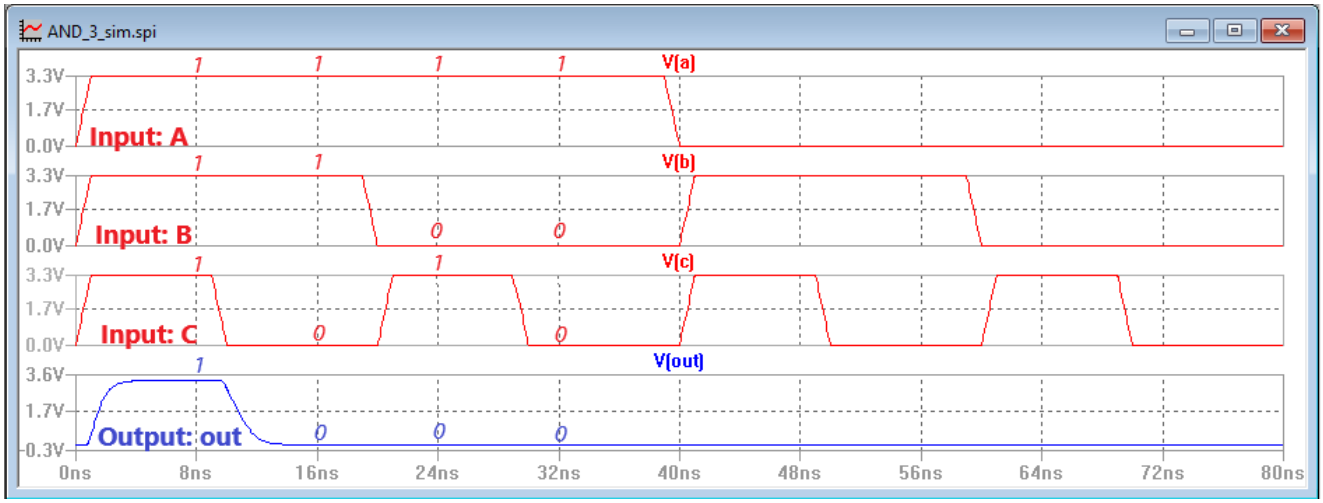

Figure 8: *LTSPICE Waveforms of Three Input AND Gate Schematic Design*

(Testing All Possible Inputs)

```
* Spice Code nodes in cell cell 'AND_3{lay}'
VDD VDD 0 DC 3.3
VGND GND 0 DC 0
vin A 0 PULSE(0 3.3 0 5ns 10ns 185ns 0ns)
vin2 B vdd
vin3 C vdd
cload out 0 250fF
.tran 0 400n
.include C:\Electric\C5_models.txt
.END
```

```
* Spice Code nodes in cell cell 'AND_3_sim{lay}'
VDD VDD 0 DC 3.3
VGND GND 0 DC 0
vin A 0 PULSE(0 3.3 0 1ns 1ns 38ns 80ns)
vin2 B 0 PULSE(0 3.3 0 1ns 1ns 18ns 40ns)
vin3 C 0 PULSE(0 3.3 0 1ns 1ns 8ns 20ns)
cload out 0 250fF
.tran 0 80n
.include C:\Electric\C5_models.txt
.END
```

Figure 9: *(Left) SPICE Code for Figure 7*

(Right) SPICE Code for Figure 8

Table 2: Delay Times of Three Input AND Gate Output (Schematic Design)

	Input Delay	Raise Time	Fall Time
Output	~8 ns	~3.2 ns	~4.5 ns

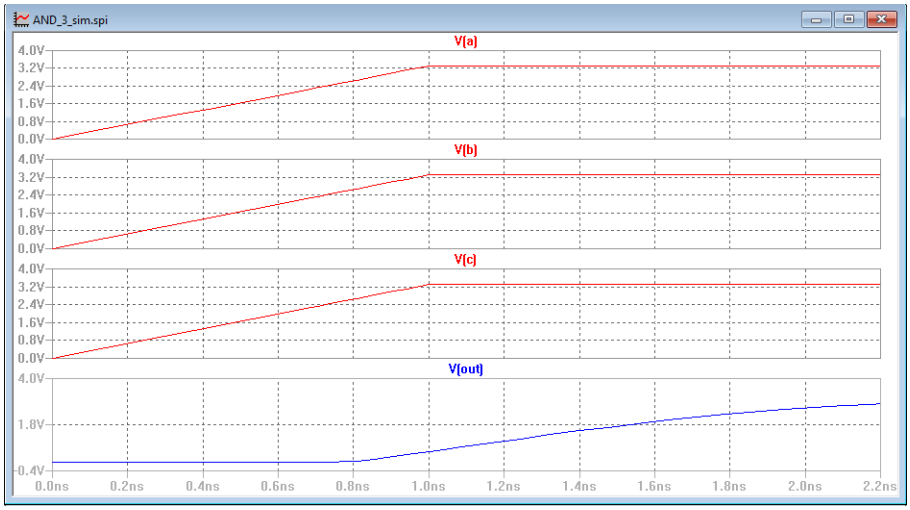

Figure 10: *Output Input Delay of Three Input AND Gate Schematic Design*

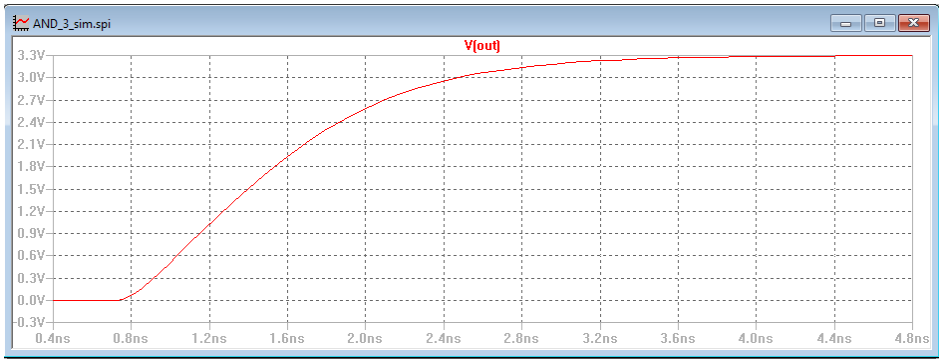

Figure 11: *Output Raise Time of Three Input AND Gate Schematic Design*

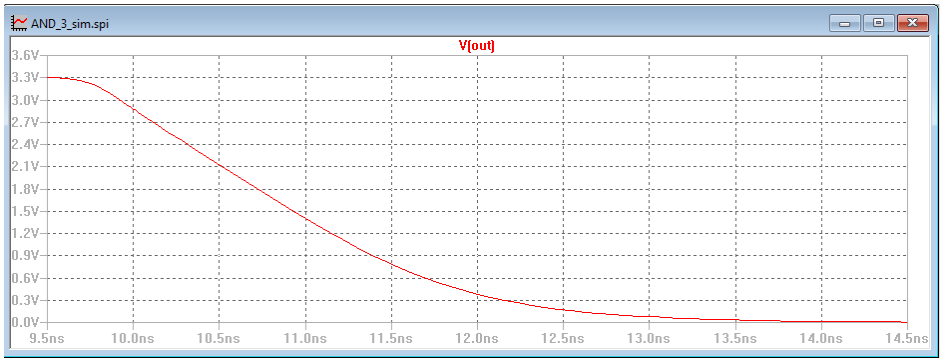

Figure 12: *Output Fall Time of Three Input AND Gate Schematic Design*

IRSIM for Electric Schematic:

After creating the schematics for the three input AND gate, we then used IRSIM to create waveforms to check our outputs. Inputs A, B, and C were configured to cover all possible inputs. We were able to verify that the output waveform generated by LTSPICE was the same as the output waveform generated by IRSIM. **Figure 13** shows the input and output waveforms of IRSIM. The propagation delay is about 0.203 nanoseconds.

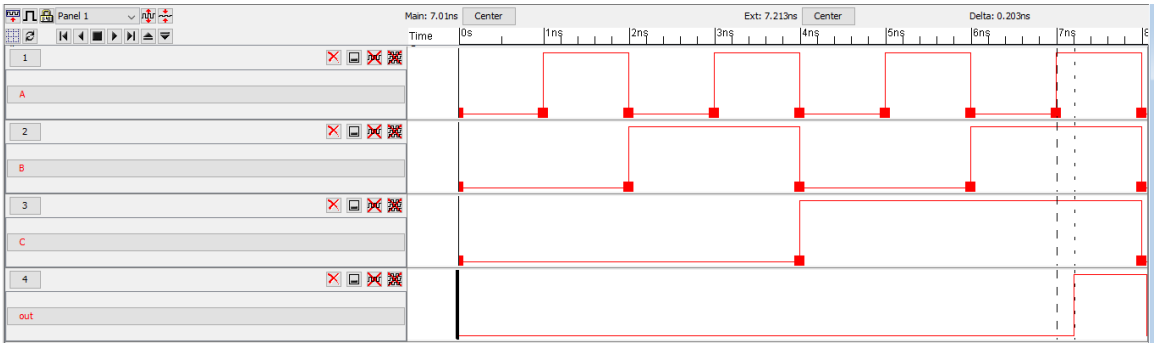

Figure 13: *IRSIM Waveforms of Three Input AND Gate Schematic Design*

Electric Layout:

We created a layout for the three input AND gate by combing a three input NAND gate (**Figure 4**) and an inverter (**Figure 2**). I combined it by connecting the output of the NAND gate to the input of the invertor. I then connected the N-Wells and the P-Wells of the individual NAND and invertor layouts. I think it would have been a better implementation to extend the N-Wells and P-Wells so that both layouts can use the same wells. It could be more cost effective than the layout I have shown here also. The layout with the SPICE code is shown in **Figure 14**. The Design Rule Check, Well Check, and NCC checks are shown in **Figure 15**.

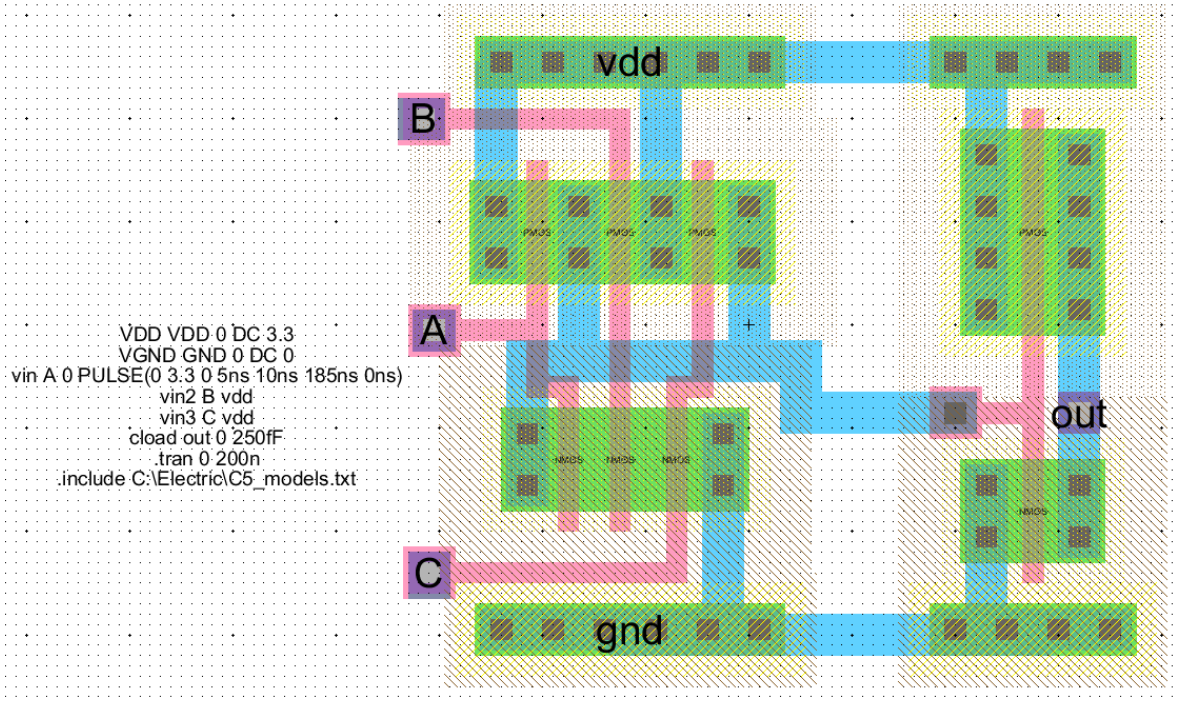

Figure 14: *Layout Design of Three Input AND Gate*

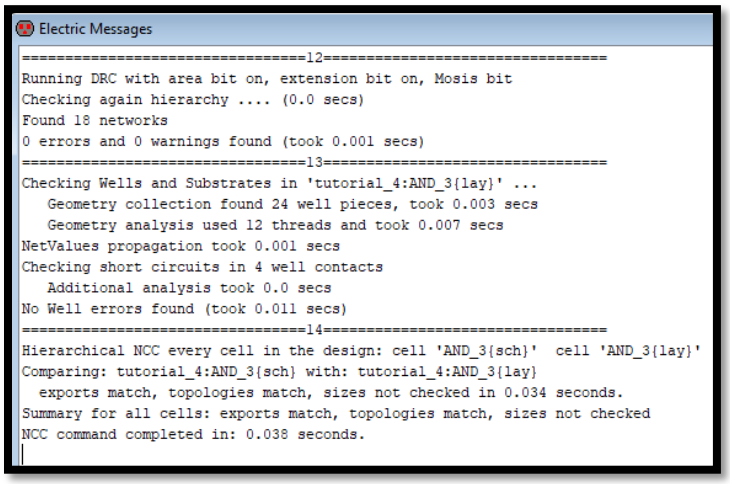

Figure 15: *DRC, Well Check and NCC of Three Input AND Gate Layout Design*

LTSPICE for Electric Layout:

After creating the layout for the three input AND gate, we used LTSPICE to create the input and the output waveforms. Just like we LTSPICE process for the schematic, we had to generate two different output waveforms with two different input waveforms.

Just like the "LTSPICE for Electric Schematic" section, we generated a waveform with one of the inputs, A, having 5 nanoseconds raise time, 10 nanoseconds fall time, and a period of 200 nanoseconds since this is a 5MHz wave. The other inputs, B and C, are tied to VDD. The resulting waveform is shown in **Figure 16**. **Figure 17** shows output waveforms of all possible input waveform. The SPICE code for these are the same ones shown in **Figure 9**.

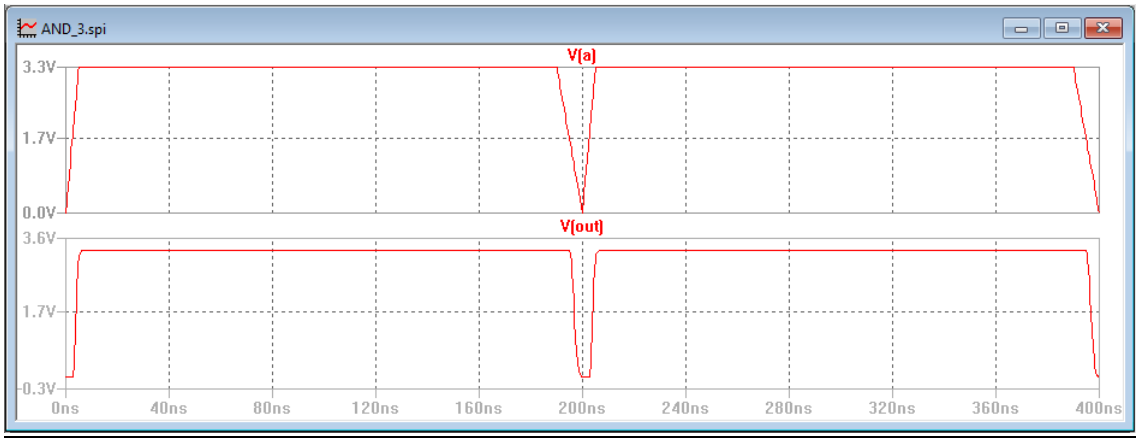

Figure 16: *LTSPICE Waveforms of Three Input AND Gate Layout Design*
(Input A is a pulse of 200ns period, 5ns raise, 10ns fall, 0ns delay, Inputs B and C are set to HIGH)

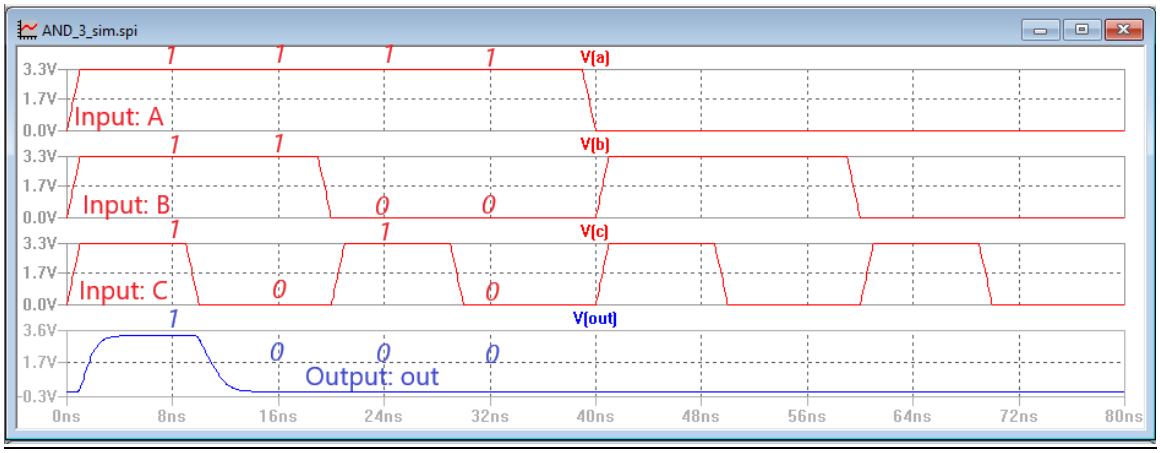

Figure 17: *LTSPICE Waveforms of Three Input AND Gate Layout Design*
(Testing All Possible Inputs)

Table 3: Delay Times of Three Input AND Gate Output (Layout Design)

	Input Delay	Raise Time	Fall Time
Output	~9 ns	~3.3 ns	~4.8 ns

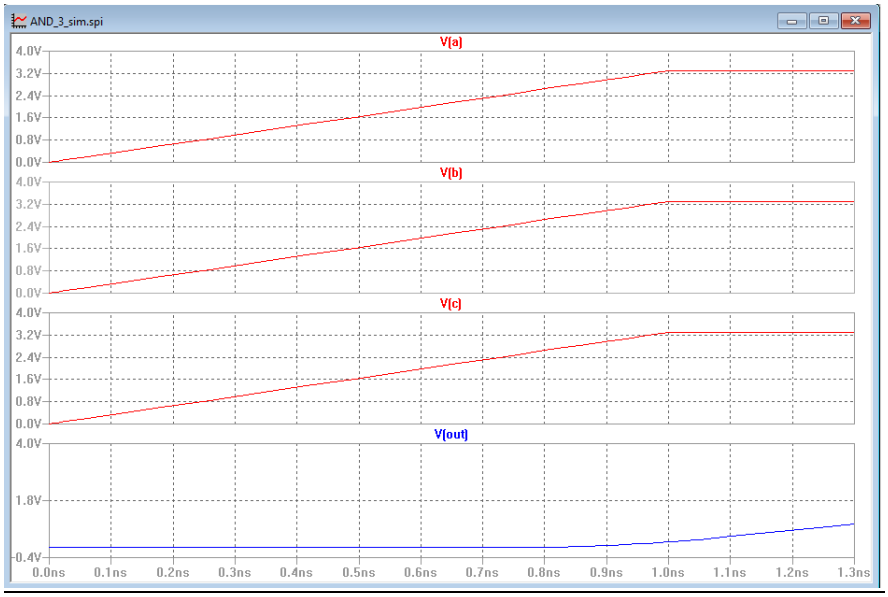

***Figure 18**: Output Input Delay of Three Input AND Gate Layout Design*

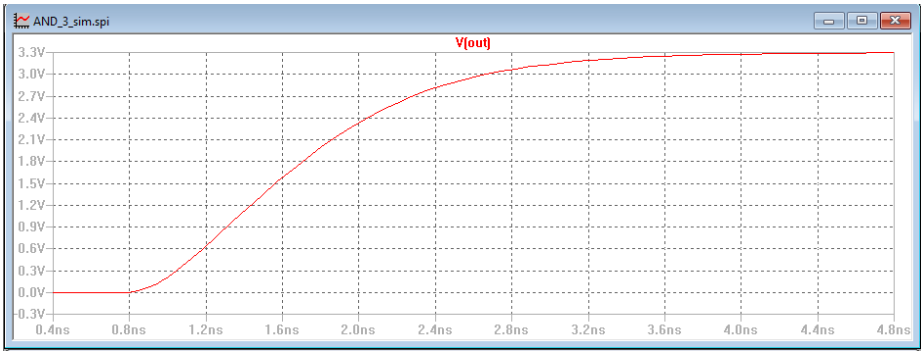

***Figure 19**: Output Raise Time of Three Input AND Gate Layout Design*

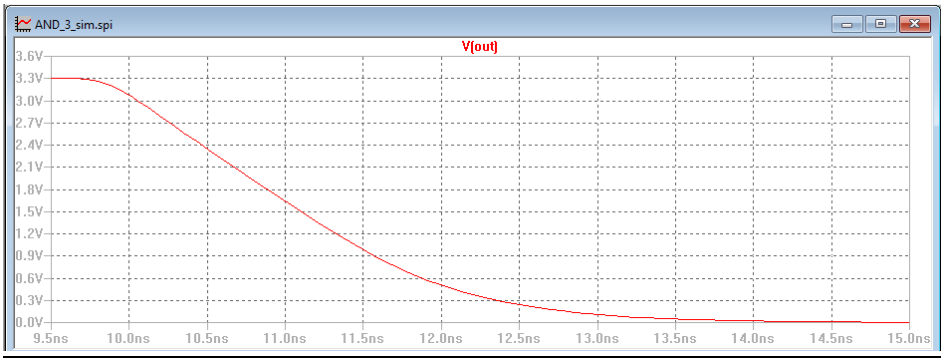

***Figure 20:** Output Fall Time of Three Input AND Gate Layout Design*

Comparison Between LTSPICE (Electric Schematic vs Electric Layout):

As seen from **Table 4**, There is very little different in the input delay, raise time and fall time for the output generated by supplying a 5MHz wave with a raise of 5 ns and a fall of 10ns. When comparing **Figure 8** and **Figure 17**, the waves are near identical. However, the Electric layout has a high delay than the Electric schematic, and thus the Electric Layout is slower.

Table 4: Delay Times of Three Input AND Gate Output

(Electric Schematic vs Electric Layout)

	Input Delay	Raise Time	Fall Time
Output (Schematic)	~8 ns	~3.2 ns	~4.5 ns
Output (Layout)	~9 ns	~3.3 ns	~4.8 ns
Difference	~1 ns	~.1 ns	~.3 ns

IRSIM for Electric Layout:

After creating the layout for the three input AND gate, we then used IRSIM to create waveforms to check our outputs. Inputs A, B, and C were configured to cover all possible inputs. We were able to verify that the output waveform generated by LTSPICE was the same as the output waveform generated by IRSIM. **Figure 21** shows the input and output waveforms of IRSIM. The propagation delay is about 0.262 nanoseconds.

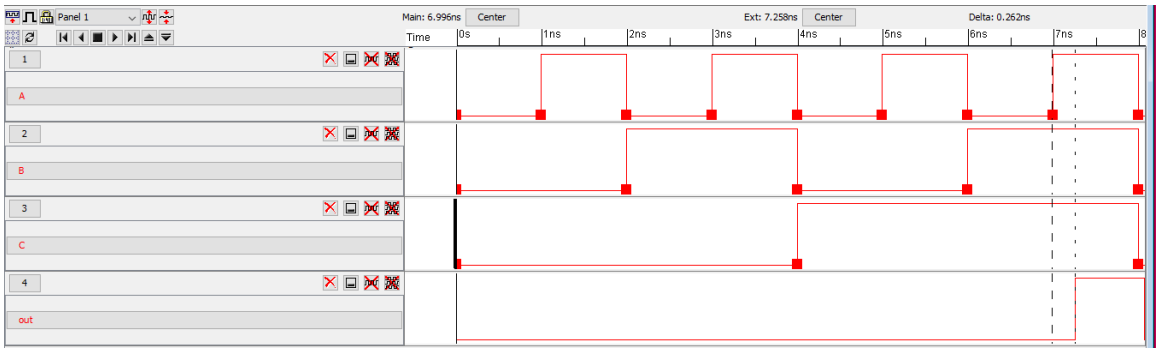

Figure 21: *IRSIM Waveforms of Three Input AND Gate Layout Design*

Comparison Between IRSIM (Electric Schematic vs Electric Layout):

When comparing the IRSIM waveforms of the Electric schematic and the Electric layout, the only difference is the propagation delay. For the Electric schematic, the delay of the output was about 0.203 ns while the delay of the output of the Electric layout was about 0.262 ns. The layout was about 0.059 ns more delayed than the schematic. This result is the same the one found when we compared LTSPICE output behavior of the Electric schematic and Electric Layout. The layout had a larger delay in both comparisons.

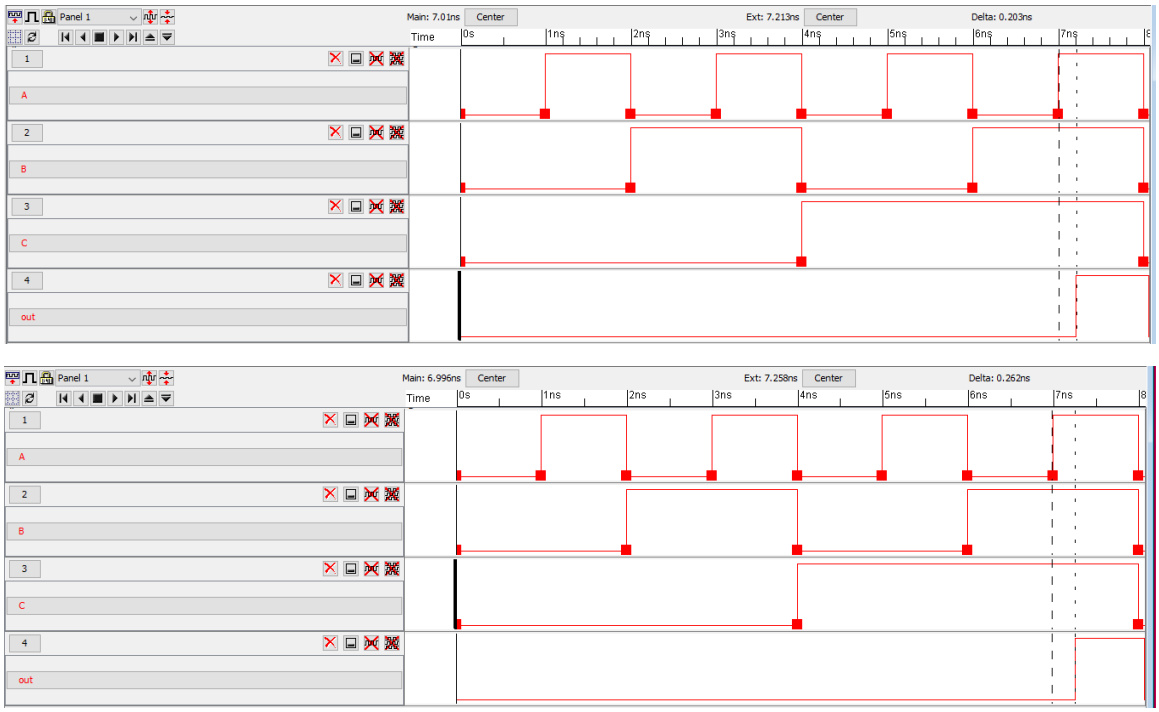

Figure 22: *IRSIM Waveforms of Three Input AND Gate Layout Design*

Electric Schematic (Top) vs Electric Layout (Bottom)

Conclusion:

In this project, we designed a three input CMOS AND gate using a three input NAND gate and an inverter. Using the Electric software, we created a schematic and a layout of the NAND gate and invertor. After testing the outputs, we combined them into an AND gate. We used LTSPICE and IRSIM to check the output waveforms. After that, we compared the differences and similarities of the LTSPICE and IRSIM waveforms of the schematic and layout.

For the Electric layout and schematic, the only differences were the input delay, the raise time, fall time, and the propagation delay. For the LTSPICE comparison, the Electric layout had a 1 ns longer input delay, a 0.1 ns longer raise time, a longer 0.3ns fall time than the Electric schematic waveform. For IRSIM, the layout's propagation delay was 0.059 ns longer. Based on these results, the layout was a little bit slower compared to the schematic.

References:

[1] *Spice3 User's Manual* [Online] Available:

http://www.gianlucafiori.org/appunti/Spice_3f3_Users_Manual.pdf

[2] *CMOS Gate Circuitry* [Online] Available:

https://www.allaboutcircuits.com/textbook/digital/chpt-3/cmos-gate-circuitry/