EE 457: Digital Integrated Circuits

Project #1 Report Cover Sheet

Due: 2/28/20

## **PROJECT TITLE:\_\_CMOS 3-input AND Gate\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

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(print your name)

|  |  |
| --- | --- |
| Your report should follow the following items in sequence.  *Do not change the sequence.*  Put a table of content after the cover sheet. | GRADE |
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| Section 2: Background and Approach (Include a truth table) | /5 |
| Section 3: Electric Schematic | /15 |
| Section 4: LTSPICE for Electric schematic | /10 |
| Section 5: IRSIM for Electric schematic | /10 |
| Section 6: Electric Layout | /25 |
| Section 7: LTSPICE for Electric layout (compare with schematic) | /15 |
| Section 8: IRSIM for Electric layout | /10 |
| Section 9: Conclusions and References | /5 |
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Note: Do not rearrange this table. Submit your report on Blackboard.

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# Executive Summary:

In this project, we will be designing a three input AND gate using Electric. In Electric, we will be creating a schematic design and a layout design. To test these designs, we will create waveforms with specific inputs and test if the output is correct using LTSPICE and IRSIM. We can then compare the waveforms of the layout and the schematic design.

To create the three input AND gate, we first made a three input NAND gate and then created an inverter. We then combined the two gates to form the NAND gate. Before combining them, we tested the output of each individual gate so that they were correct and satisfied the requirements. This also helped us avoid creating unexpected waveforms from the combined NAND gate.

For the three input NAND gate, we used three PMOS transistors in parallel and three NMOS transistors in series. To create the three parallel PMOS transistors in the layout, we had to use four P-Active areas and one N-well (which was Vdd) area. To create the three series NMOS transistors, we used only two N-Active areas and one P-Well.

# Background and Approach:

A three input AND gate is a logic gate that will output a HIGH is all its inputs are also HIGH. It has a Boolean expression of F = ABC.

|  |  |  |  |
| --- | --- | --- | --- |
| Input: A | Input: B | Input: C | Output: A and B and C |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Table 1: Truth Table of a Three Input AND Gate

My approach was to make a NAND gate and an inverter separately and then combine them together to create the AND gate. The NAND gate has a Boolean expression of

F = A̅B̅C̅. So, to turn it into the expression of an AND gate, we need to pass the output of the NAND gate through an inverter to get F = ABC. so all we have to do is put the output through an inverter to get the