Micro-Architecture of ARM AMBA-3 AHB-lite Protocol

ECE-593 Fundamentals of Pre-Silicon Validation Spring -2020

AAYUSH RAVICHANDRAN [9811120898]

KAUSTUBH MHATRE [974819541]

SAURABH WAMAN CHAVAN [911836716]

ARM AMBA-3 AHB-lite Protocol

1 PROTOCOL DESCRIPTION

AMBA AHB-Lite is a bus interface that supports a single bus master and provides high-bandwidth operation. It is used in high-performance synthesizable designs.

AHB-Lite implements the features required for high-performance, high clock frequency systems including:
• burst transfers
• single-clock edge operation
• non-tristate implementation
• wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

The most common AHB-Lite slaves are internal memory devices, external memory interfaces, and high bandwidth peripherals.

The main component types of an AHB-Lite system are:

1. Master
2. Slave
3. Decoder
4. Multiplexor

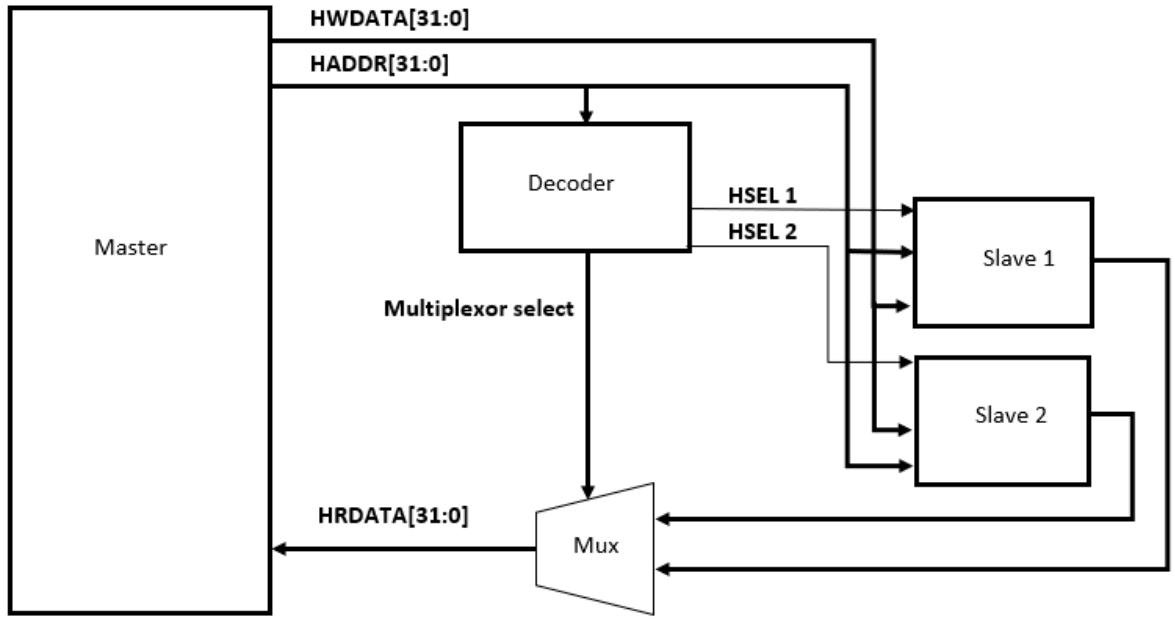

Figure 1: Block diagram of AMBA-3 AHB-Lite protocol

2 SIGNAL DESCRIPTION

2.1 MASTER

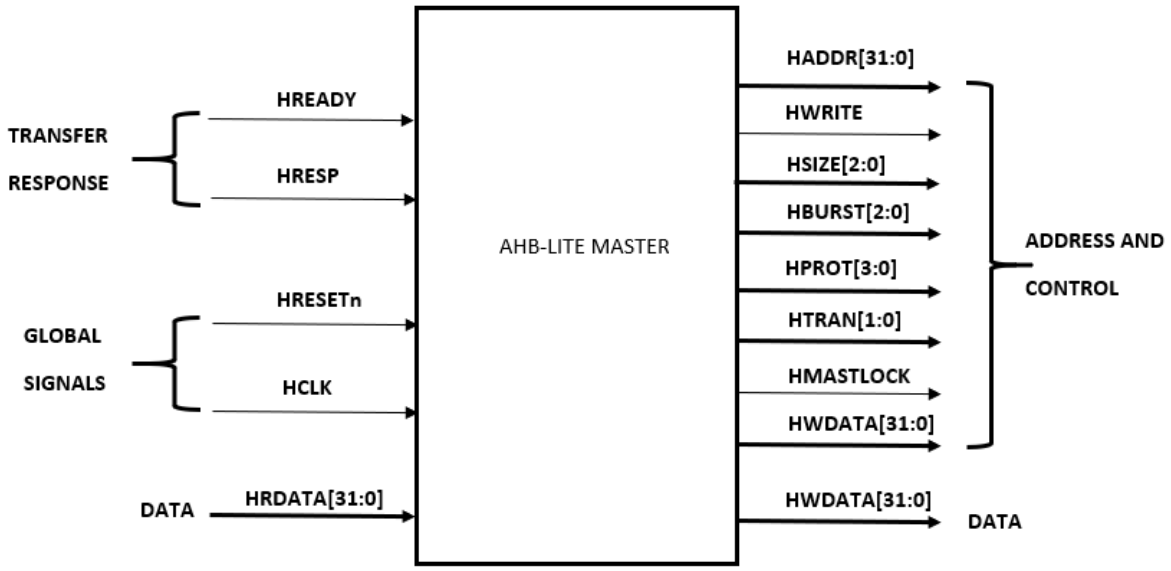

Figure 2: Master Interface

Name	Destination	Description
HADDR[31:0]	Slave and decoder	32 bit system address bus
HBURST[2:0]	Slave	Indicates if the transfer type is a burst of single type or burst of 4, 8 or 16 beats. Burst can be incrementing or wrapping(wrapping burst wrap around a address boundary)
HMASTLOCK	Slave	When asserted HIGH indicates that the transfer sequence is locked and current transfer is indivisible. No other transfer other than the locked sequence can be processed. Note: It is not implemented in the current design and verification
HPROT[3:0]	Slave	Provides additional information about the bus access. Note: It is not implemented in the current design and verification
HSIZE[2:0]	Slave	Indicates the transfer size. Typical sizes are, byte, half word or word. It must be equal or less than the size of the bus. It is used in conjunction with the HBURST and has the timing which is same as address bus.
HTRANS[1:0]	Slave	Indicates the transfer type is: 1. IDEAL 2. BUSY 3. NONSEQUENTIAL 4. SEQUENTIAL
HWDATA[31:0][a]	Slave	Indicates write data of minimum 32 bits from Master to Slave
HWRITE	Slave	Indicates direction of transfer. When HIGH the direction is from Master to Slave and when LOW it indicates read operation from slave to master.

2.2 SLAVE

A Slave selected using the HSELx signal using the Decoder controls the transfer progress. Slave response signalling consists of the following three types:

1. It can immediately complete the transfer
2. Insert WAIT states for the transfers to continue
3. Provide error signalling to indicate the transfer has failed

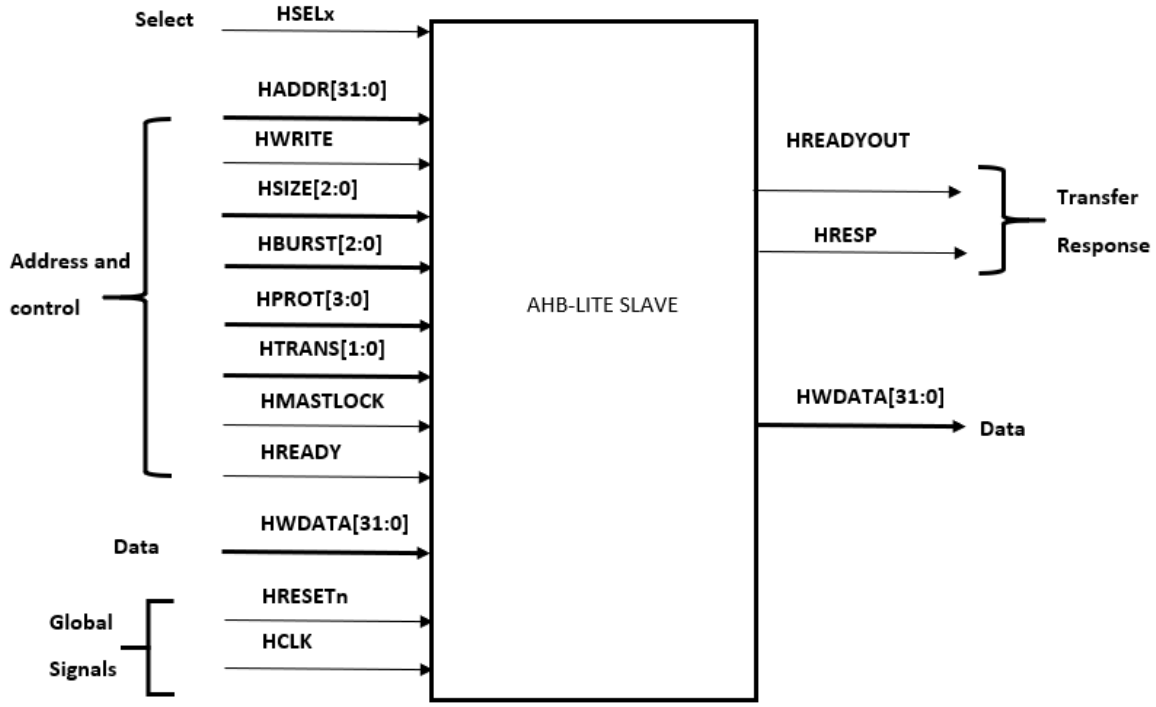

Figure 3: Slave Interface

Name	Destination	Description
HRDATA[31:0][a]	Multiplexor	During read operation, the data is transferred from slave to multiplexor and then from multiplexor to the master.
HREADYOUT	Multiplexor	When HIGH it indicates that the transfer has finished on the bus. When LOW the current transfer is extended.
HRESP	Multiplexor	Additional information can be provided on the transfer status. LOW indicates that the transfer status is OKAY HIGH indicates that the transfer status is ERROR

2.3 GLOBAL SIGNALS

Name	Destination	Description
HCLK	Clock source	It is a single clock signal. All signals are sampled at the rising edge of the clock. Output signal changes must occur after the rising edge of HCLK
HRESETn	Reset Controller	It is the only active LOW signal. It resets the bus and the system. The reset can be asserted asynchronously, it is deasserted synchronously after the rising edge of HCLK

2.4 DECODER

The central decoder provides HSELx slave select signal for each slave of interest for transfer.

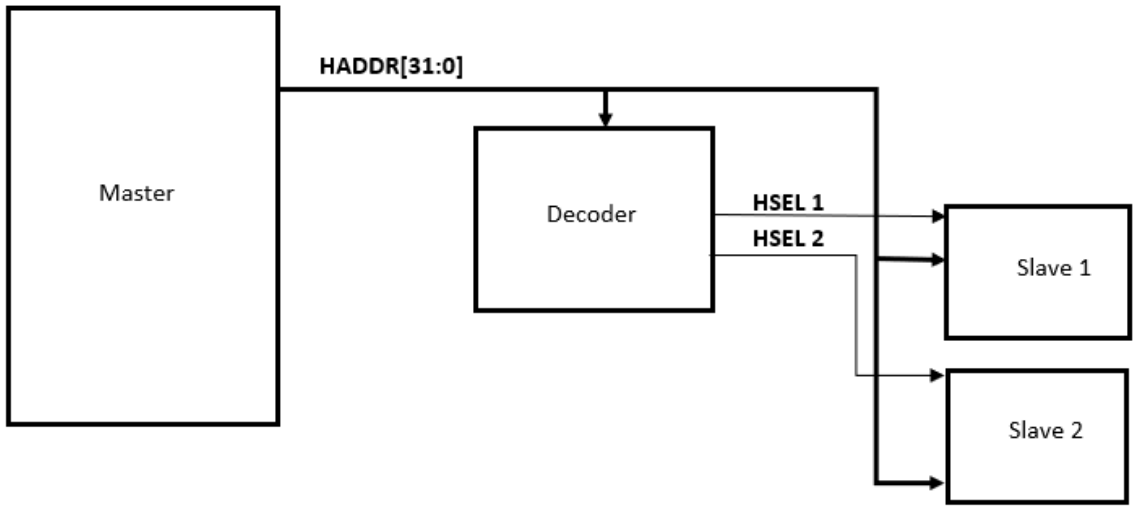

Figure 4: Decoder Interface

Name	Destination	Description
HSELx[a]	Slave	Each slave has this signal which indicates its selection. HREADY signal is monitored when a slave is selected initially to ensure the previous transfer completion

The decoder also provides the signal HSELx to the Multiplexor so that the Multiplexor routes the signals from the selected Slave to the Master.

2.5 MULTIPLEXOR

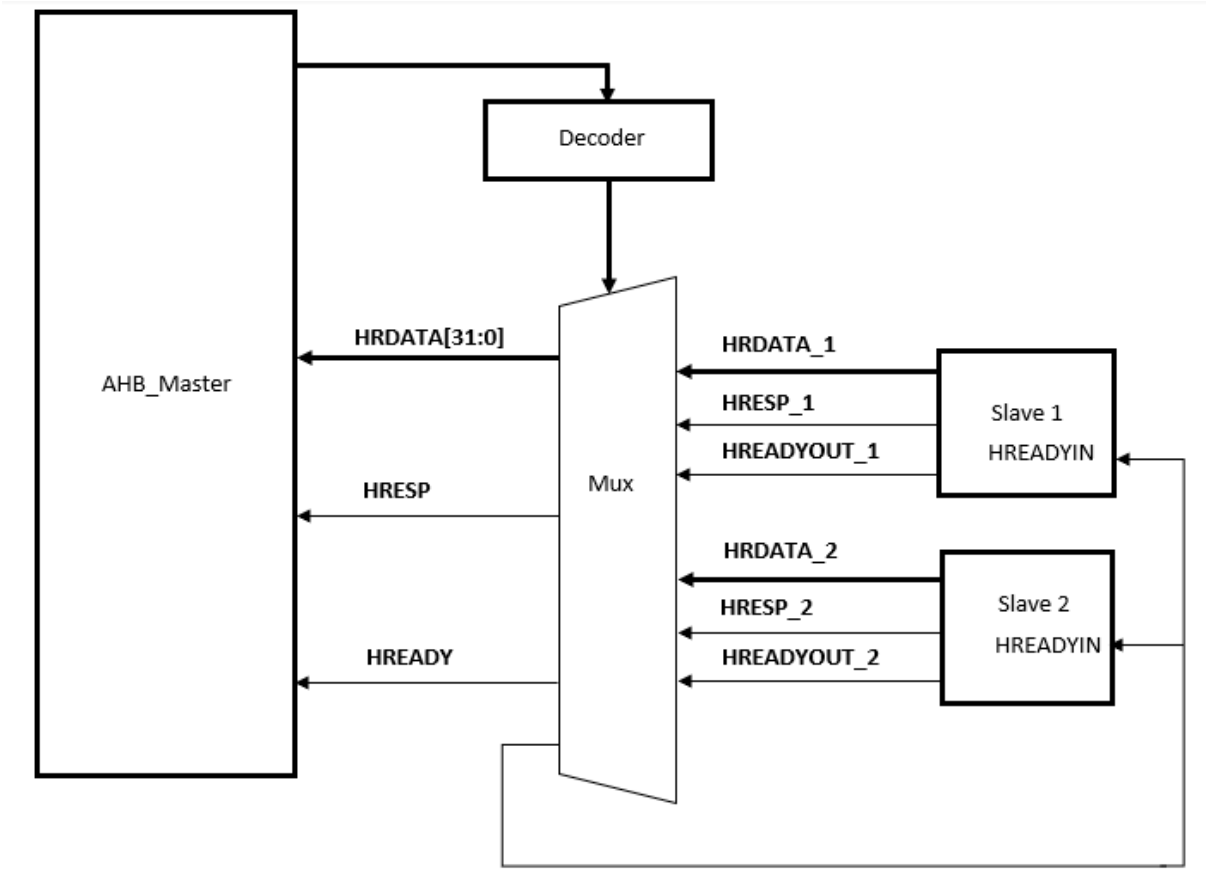

Figure 5: Multiplexor Interface

Name	Destination	Description
HRDATA[31:0]	Master	Read data bus as selected by the decoder
HREADY	Master and Slave	HREADY when asserted HIGH indicates that the previous transfer is complete
HRESP	Master	Response signal of the transfer selected by the decoder

3 OPERATION

The Master drives the control and address signals when it starts a transfer. The transfer consists of two phases:

1. Address phase: One address and control cycle
2. Data Phase: one or more cycles for the data

The transfers can be:

1. Single
2. Incremental burst
3. Wrapping burst which wrap at address boundaries

4 BURST

The protocol defines the BURSTS of 4, 8, and 16-beats, undefined burts, and single transfers. Support for incrementing and wrapping burst is provided

HBURST[2:0]	Type	Description
b000	SINGLE	Single burst
b001	INCR	Incrementing burst of undefined length
b010	WRAP4	4-beat wrapping burst
b011	INCR4	4-beat incrementing burst
b100	WRAP8	8-beat wrapping burst
b101	INCR8	8-beat incrementing burst
b110	WRAP16	16-beat wrapping burst
b111	INCR16	16-beat incrementing burst

Single Burst example:

- The simplest transfer with no WAIT state for the SINGLE burst is shown below.
- It consists of one address phase cycle and data phase cycle both happening in single clock.

SINGLE BURST READ TRANSFER

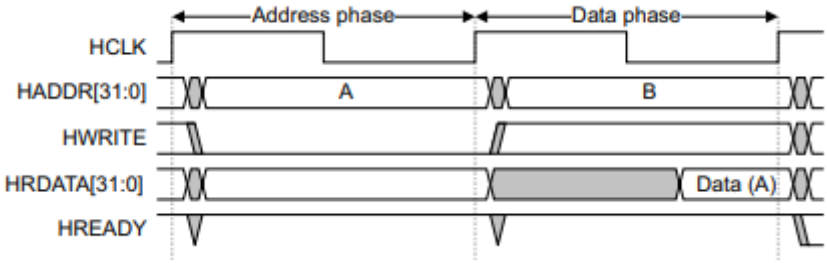

Figure 6: SINGLE burst READ transfer

SINGLE BURST WRITE TRANSFER

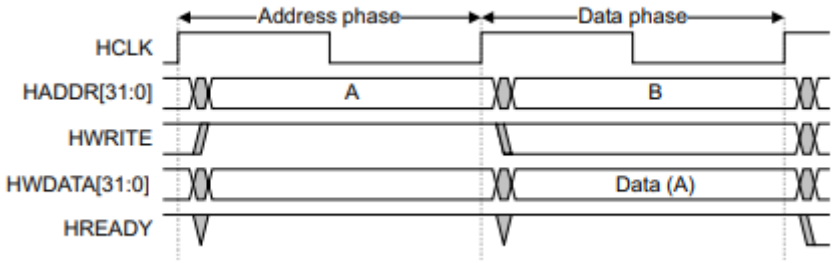

Figure 7: SINGLE burst WRITE transfer

5 TRANSFER TYPES

The transfer types supported in the protocol are as follows:

TYPE	DESCRIPTION
IDLE	It indicates that no data transfer is required. Master uses and IDLE transfer when it does not want to perform a data transfer.Slaves must always provide a zero wait state OKAY response to IDLE transfers and the transfer must be ignored by the slave
BUSY	The BUSY transfer enables masters to insert idle cycles in the middle of a burst. The next transfer cannot take place immediately. When a master uses the BUSY transfer type the address and control signals must reflect the next transfer in the burst. Slaves must always provide a zero wait state OKAY response to BUSY transfers and the transfer must be ignored by the slave.
NONSEQ	Indicates a single transfer or the first transfer of a burst. The address and control signals are unrelated to the previous transfer. Single transfers on the bus are treated as bursts of length one and therefore the transfer type is NONSEQUENTIAL.
SEQ	The remaining transfers in a burst are SEQUENTIAL and the address is related to the previous transfer. The control information is identical to the previous transfer. The address is equal to the address of the previous transfer plus the transfer size, in bytes, with the transfer size being signaled by the HSIZE[2:0] signals. In the case of a wrapping burst the address of the transfer wraps at the address boundary.

Wrapping burst example with No IDLE or BUSY state transfer type:

1. The first cycle is of transfer type NONSEQ.
2. Following cycles are of transfer type SEQ.
3. The burst is an eight-beat burst of word transfers, the address wraps at 32-byte boundaries, and the transfer to address 0x3C is followed by a transfer to address 0x20.

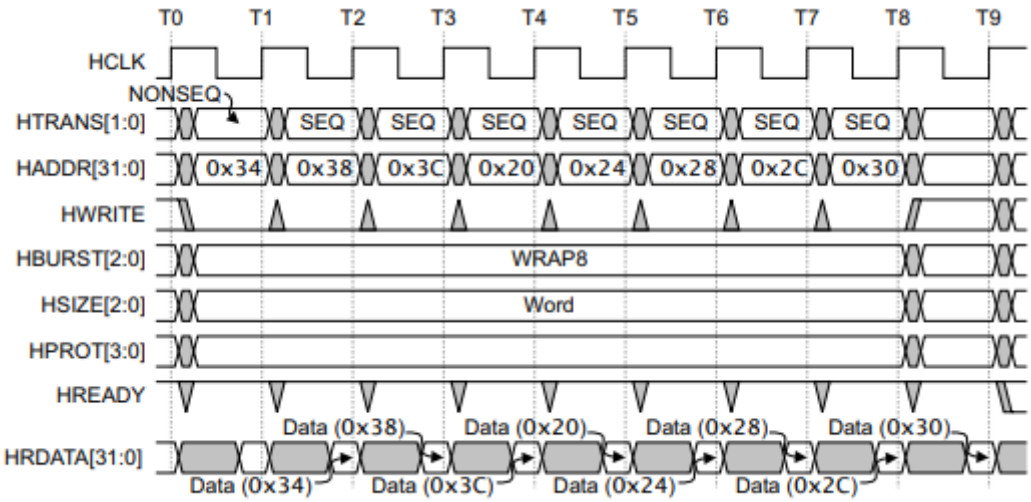

Figure 8: EIGHT beat WRAPPING burst