Problem

Create 8 D flip-flops with active high synchronous reset. All DFFs should be triggered by the positive edge of clk.

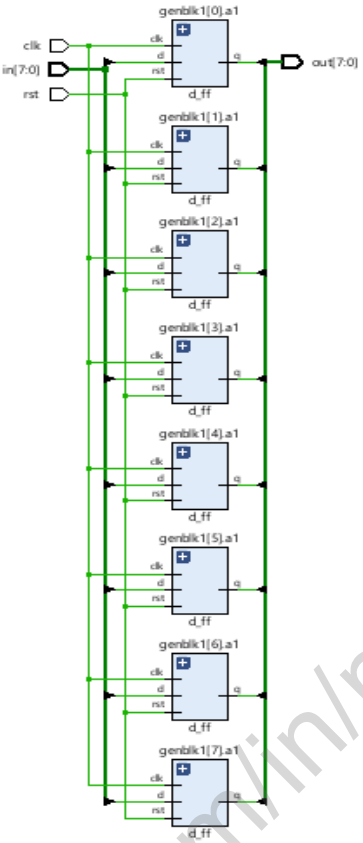
Design

```
module d_ff( input clk,d,rst,
             output reg q
    );
    always@(posedge clk)begin
    if(rst) q<=0;
    else
    q<=d;
    end
endmodule

module pipo #(parameter Bitwidth=8)(input [Bitwidth-1:0] in,
                                    input clk,rst,output [Bitwidth-1:0]
out);
 generate
genvar i;
for (i = 0; i < Bitwidth; i = i + 1) begin
d_ff a1(clk,in[i],rst,out[i]);
end
endgenerate

endmodule
```

Circuit



Testbench

```
module tb( );
reg rst,clk;reg [7:0] in;
wire[7:0] out;

pipo a1(in,clk,rst,out);

always #5 clk=~clk;

initial begin
clk=0;rst=1;
repeat(2)begin
#3
in=$random;
#7;
end
rst=0;
repeat(5)begin
#3
in=$random;
```

```
#7;
end
rst=1;
repeat(2)begin
#3
in=$random;
#7;
end
endmodule
```

Waveform