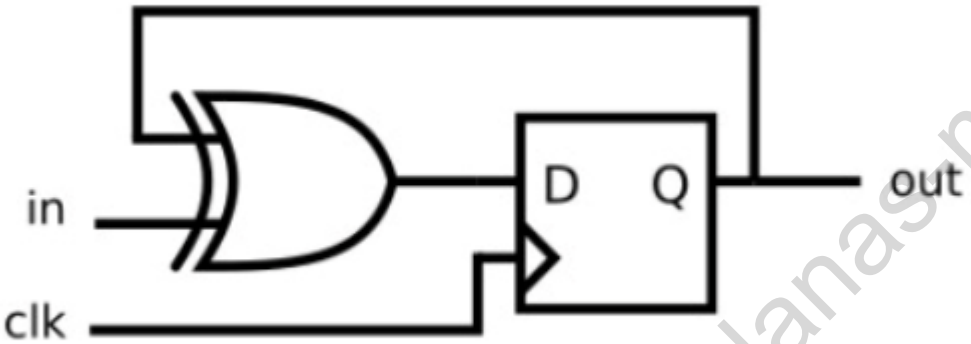
Problem

Implement the given circuit



Design

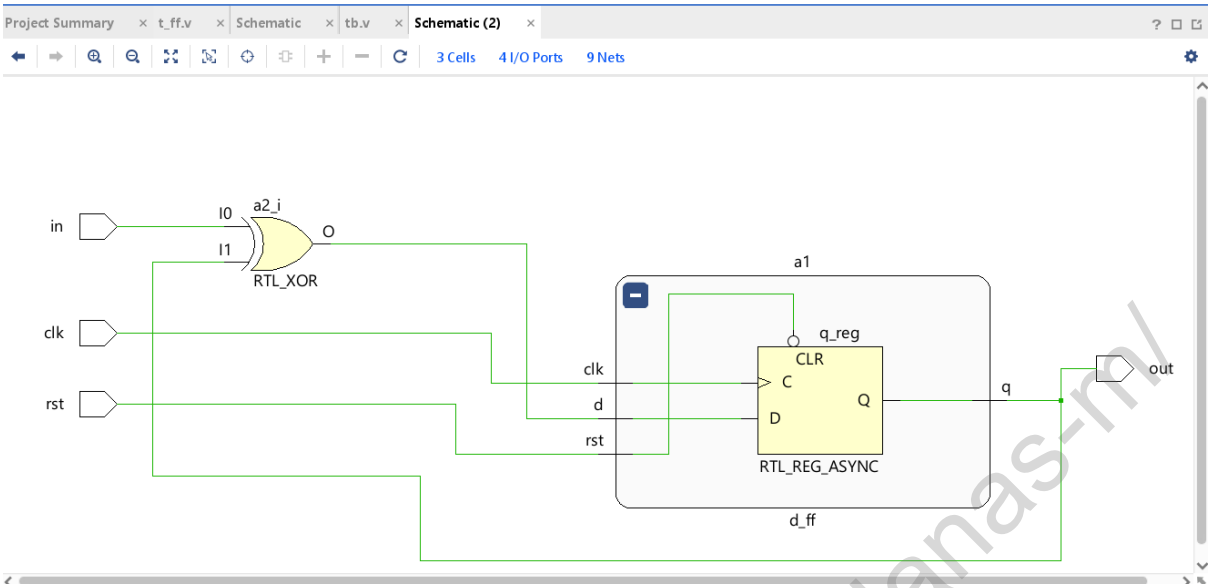
```
module d_ff(input d,clk,rst,output reg q);
always @(posedge clk or negedge rst)
if(~rst)
q<=0;
else
q<=d;
endmodule

module t_ff( input in,clk,rst,
             output out  );
    wire t1,t2;
    d_ff a1(t1,clk,rst, t2);
    xor a2(t1,in,t2);

    assign out=t2;

endmodule
```

Circuit



Testbench

```
module tb();

reg clk,in,rst;
wire out;

t_ff a1(in,clk,rst,out);

 always #5 clk=~clk;

 initial begin
 clk=0;in=0;rst=0;
 #3;
 rst=1;
  repeat(10) begin
  in={$random}%2;
  #5;
  end
  $finish;
  end

endmodule
```

Waveform