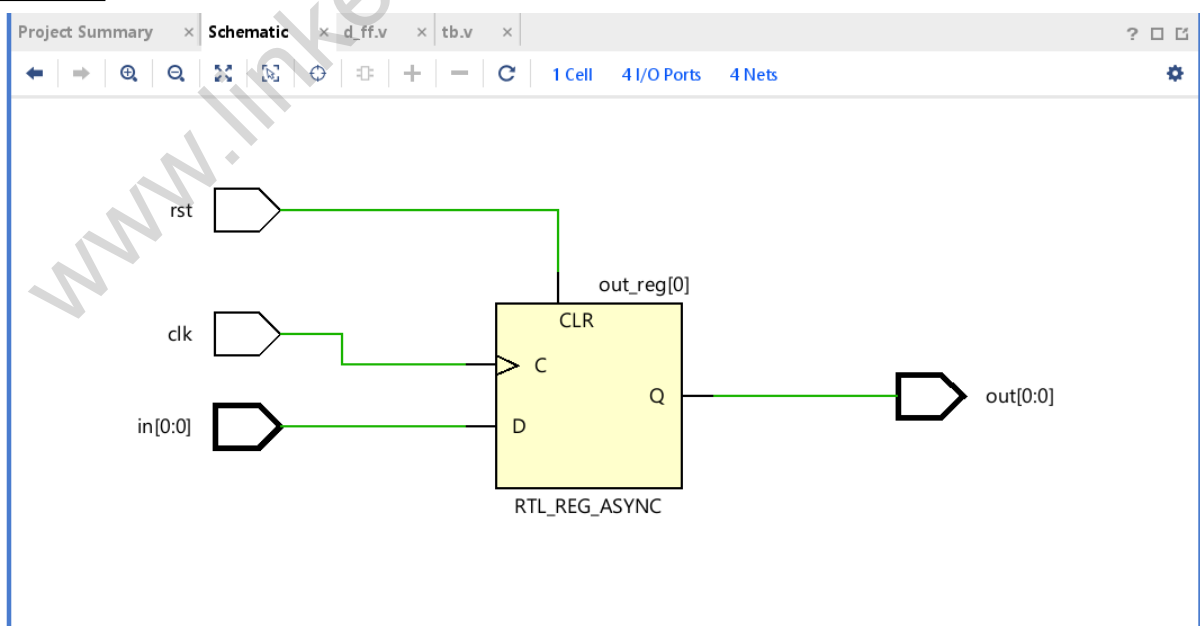## Problem

Implement a D Flip Flop with asynchronous reset

Design

```verilog
module d_ff #(parameter Bitwidth=1)(input [Bitwidth-1:0] in,
                                    input clk,rst,output reg
[Bitwidth-1:0] out);
    always@(posedge clk or posedge rst)begin
    if(rst) out<=8'h00;
    else
    out<=in;
    end

endmodule
```

Circuit

Testbench

```verilog
module tb( );
reg rst,clk;reg [0:0] in;
wire[0:0] out;

d_ff a1(in,clk,rst,out);

always #5 clk=~clk;

initial begin
clk=0;rst=1;
repeat(2)begin
#3
in={$random}%2;
#7;
end
rst=0;
repeat(5)begin
#3
in={$random}%2;
#7;
end
rst=1;
repeat(2)begin
#3
in={$random}%2;
#7;
end

end
endmodule
```

Waveform