Problem

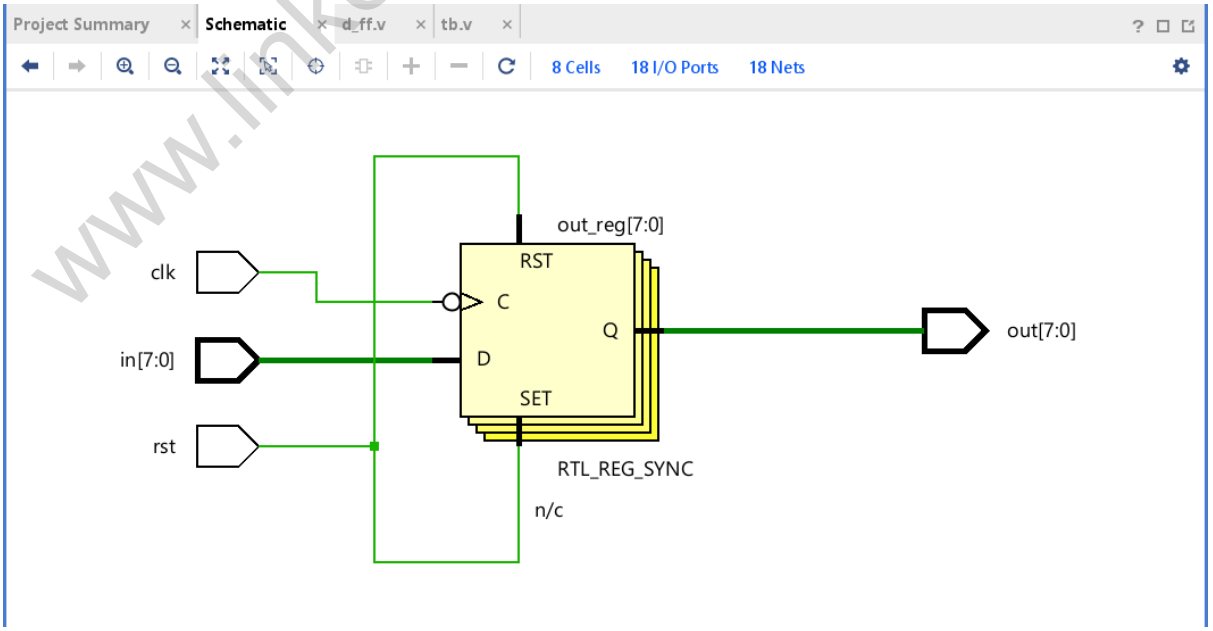
Create 8 D flip-flops with active high synchronous reset. The flip-flops must be reset to Ox34 rather than zero. All DFFs should be triggered by the negative edge of clk.

Design

```
module d_ff #(parameter Bitwidth=8)(input [Bitwidth-1:0] in,
                                    input clk,rst,output reg
[Bitwidth-1:0] out);
    always@(negedge clk)begin
    if(rst) out<=8'h34;
    else
    out<=in;
    end

endmodule
```

Circuit



Testbench

```
module tb( );
reg rst,clk;reg [7:0] in;
wire[7:0] out;

d_ff a1(in,clk,rst,out);

always #5 clk=~clk;

initial begin
clk=0;rst=1;
repeat(2)begin
#3
in=$random;
#7;
end
rst=0;
repeat(5)begin
#3
in=$random;
#7;
end
rst=1;
repeat(2)begin
#3
in=$random;
#7;
end
endmodule
```


Waveform