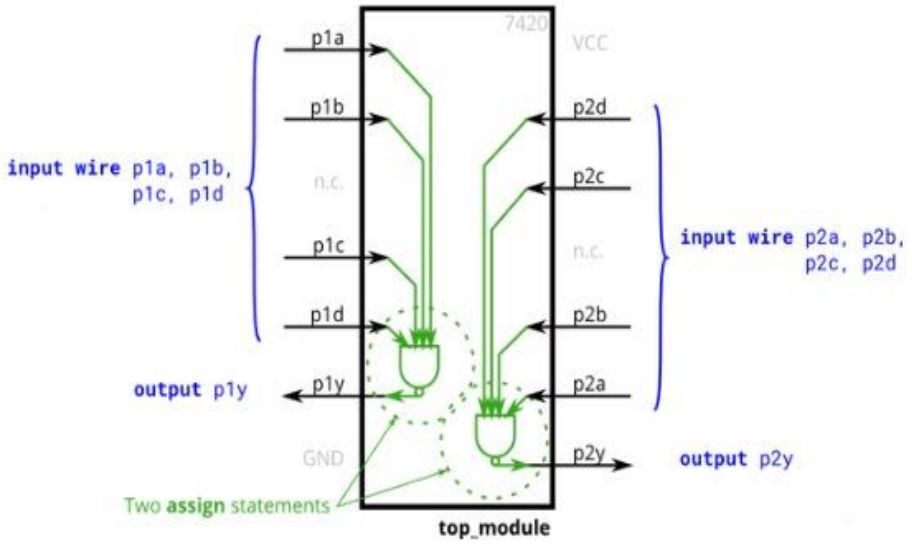
IEEE CAS STUDENT CHAPTER
SAHRDAYA COLLEGE OF
ENGINEERING AND TECHNOLOGY

#100rtldays Challenge

EXPERIENCE THE JOY OF LEARNING

#Day2: Implement the chip shown below



Design

```
module day2( input p1a,p1b,p1c,p1d,p2a,p2b,p2c,p2d, output p1y,p2y);
  assign p1y=~(p1a^p1b^p1c^p1d);
  assign p2y=~(p2a^p2b^p2c^p2d);

endmodule
```

Testbench

```
module tb;
  reg p1a,p1b,p1c,p1d,p2a,p2b,p2c,p2d;
  wire p1y,p2y;
  integer c1=0,c2=0;
  integer err_count=0;
  day2 a1(p1a,p1b,p1c,p1d,p2a,p2b,p2c,p2d,p1y,p2y);

  initial begin
    $dumpfile("test.vcd");
    $dumpvars;
  end

  initial begin
    repeat (5)begin
      #5 p1a={$random} % 2;p1b={$random} % 2;p1c={$random} % 2;
      p1d={$random} % 2;p2a={$random} % 2;p2b={$random} % 2;
      p2c={$random} % 2;p2d={$random} % 2;
    end
    $display("\nerror count=%0d time=%0t\n",err_count,$time);
 $finish;
  end

  always @(p1a,p1b,p1c,p1d) begin
    c1=p1a+p1b+p1c+p1d;
    c1=c1%2;
    if(p1y==!c1)
      $display("\nsucces1 time=%0t\n",$time);
    else begin
      $display("\nfail1 time=%0t\n",$time);
      err_count++;
    end
  end

    always @(p2a,p2b,p2c,p2d) begin
    c2=p2a+p2b+p2c+p2d;
    c2=c2%2;
    if(p1y==!c1)
      $display("\nsucces2 time=%0t\n",$time);
    else begin
      $display("\nfail2 time=%0t\n",$time);
      err_count++;
    end
  end

endmodule
```

Console report

```
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4671 kB (elbread=427 elab2=4109 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL:
# KERNEL: succes1 time=5
# KERNEL:
# KERNEL:
# KERNEL: succes2 time=5
# KERNEL:
# KERNEL:
# KERNEL: succes1 time=10
# KERNEL:
# KERNEL:
# KERNEL: succes2 time=10
# KERNEL:
# KERNEL:
# KERNEL: succes1 time=15
# KERNEL:
# KERNEL:
# KERNEL: succes2 time=15
# KERNEL:
# KERNEL:
# KERNEL: succes1 time=20
# KERNEL:
# KERNEL:
# KERNEL: succes2 time=20
# KERNEL:
# KERNEL:
# KERNEL: error count=0 time=25
# KERNEL:
# RUNTIME: Info: RUNTIME_0068 testbench.sv (22): $finish called.
# KERNEL: Time: 25 ns,  Iteration: 0,  Instance: /tb,  Process: @INITIAL#15_1@.
# KERNEL: stopped at time: 25 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
```

Waveform