Problem

Create a 1-bit wide, 256-to-1 multiplexer. The 256 inputs are all packed into a single 256-bit input vector. sel=0 should select in[0], sel=1 selects bits in[1], sel=2 selects bits in[2], etc.

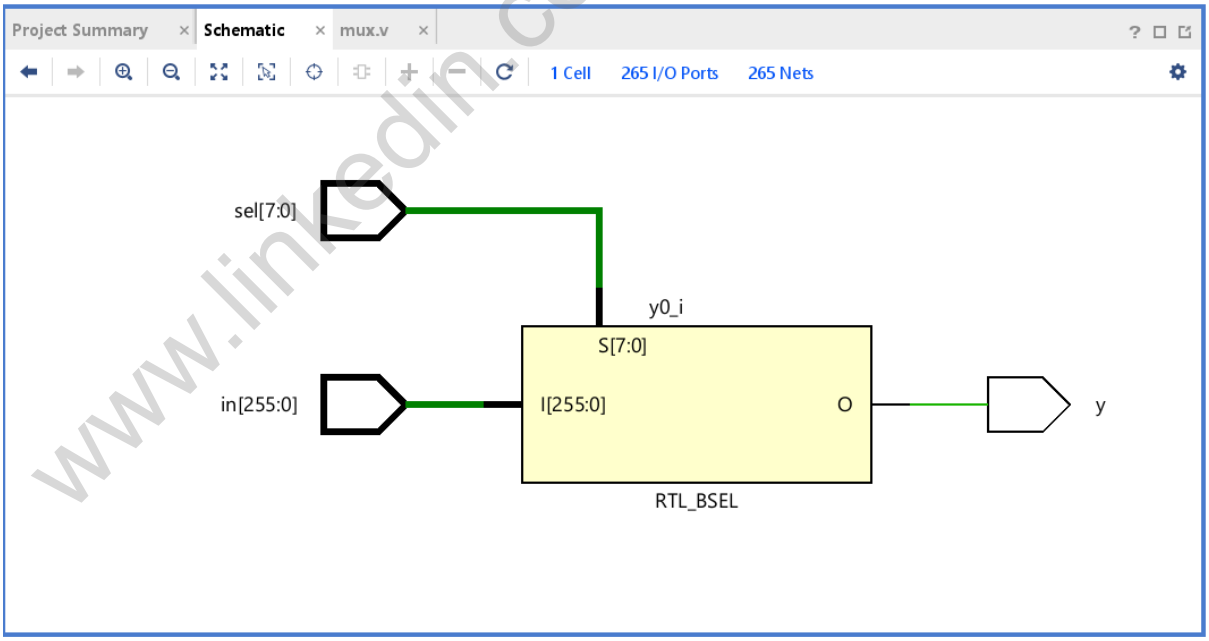
Design

```
module mux( input [255:0] in,
            input [7:0] sel,
            output reg y
    );

    always @(*)
    y=in[sel];

endmodule
```

Circuit



Testbench

```
module tb();
   reg [255:0] in;reg [7:0]sel;
   wire out;
   integer i=0;
    mux a1(in,sel,out);
initial begin
repeat(10) begin
in=i+1;
sel=i;
#50;
sel=i+1;
i=i+1;
end
end
endmodule
```

Waveform