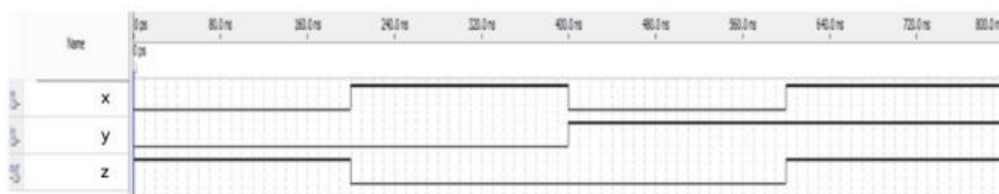


#100rtdays Challenge

EXPERIENCE THE JOY OF LEARNING

#Day5: Circuit B can be described by the following simulation waveform:



Implement this circuit

Design

```
module B( input x,y, output z);
  xnor a1(z,x,y);

endmodule
```

Testbench

```
`timescale 1ns/1ns
module tb;
  reg x,y;
  wire z;

  B a2(x,y,z);

  initial begin
    $dumpfile("test.vcd");
    $dumpvars;
  end

  initial begin
    x=0;y=0;
    #200 x=1;
    #200 x=0;y=1;
    #200 x=1;
    #200
    $finish;
  end

endmodule
```

Waveform

