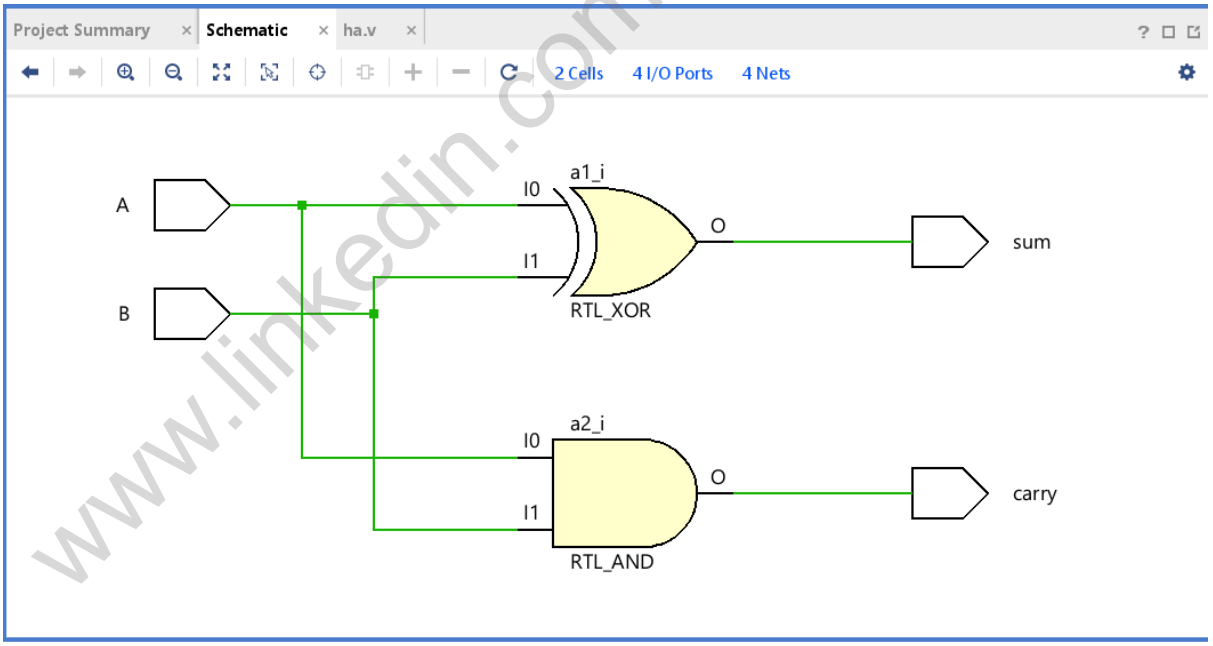
Problem

Create a half adder. A half adder adds two bits(with no carry-in) and produces a sum and carry-out.

Design

```
module ha(
input A,B,output sum,carry
    );
    xor a1(sum,A,B);
    and a2(carry,A,B);
endmodule
```

Circuit



Testbench

```
module tb();

reg a,b;
wire sum,carry;

ha a3(a,b,sum,carry);

initial begin
repeat(10) begin
{a,b}={$random}%4;
#50;
end
end
endmodule
```

Waveform