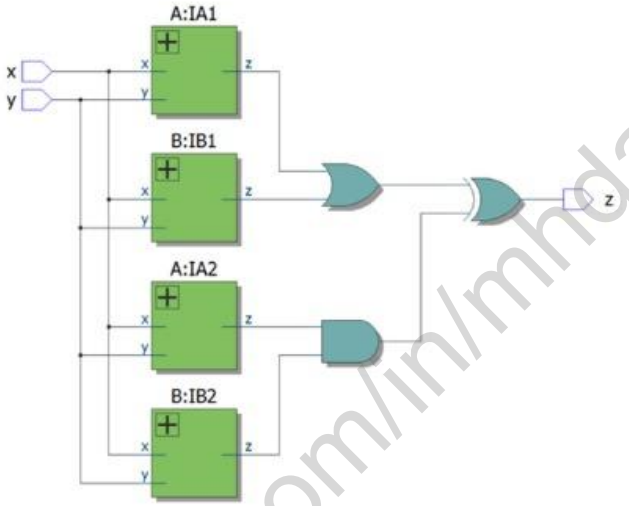
ELECSTA IEEE CAS STUDENT CHAPTER SAHRDAYA COLLEGE OF ENGINEERING AND TECHNOLOGY IEEE CAS

#100rtldays Challenge

EXPERIENCE THE JOY OF LEARNING

#Day6: Implement the circuit. A is the module used #Day4 challenge and B is the module used #Day5 challenge .



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Design

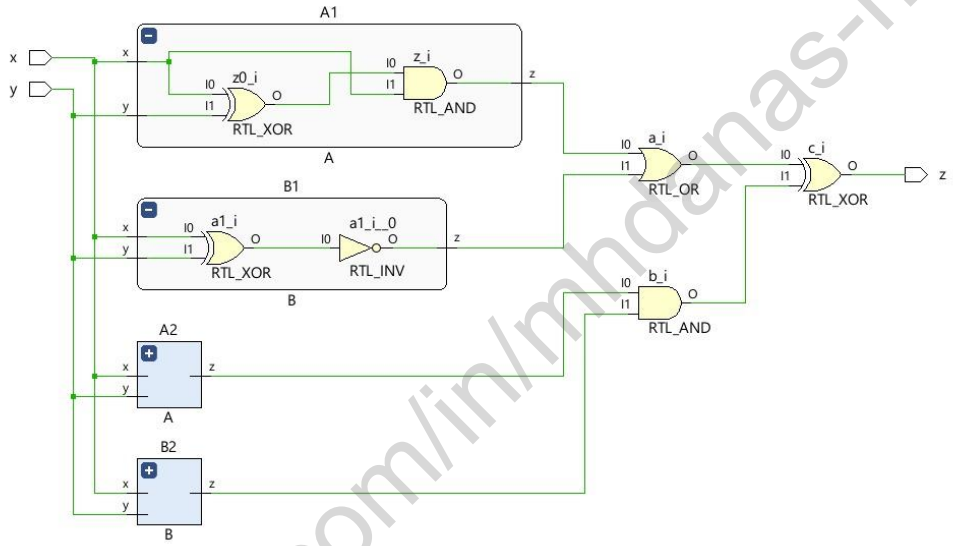
```
module A( input x,y, output z);
  assign z=(x^y)&x;
endmodule

module B( input x,y, output z);
  xnor a1(z,x,y);
endmodule

module C(input x,
         input y,
         output z
    );
    wire z1,z2,z3,z4,z5,z6;
    A A1(x,y,z1);
    B B1(x,y,z2);
```

```
    A A2(x,y,z3);
    B B2(x,y,z4);
    or a(z5,z1,z2);
    and b(z6,z3,z4);
    xor c(z,z5,z6);
endmodule
```

Circuit



Testbench

```
`timescale 1ns/1ns
module tb;
  reg x,y;
  wire z;

  C a2(x,y,z);

  initial begin
    $dumpfile("test.vcd");
    $dumpvars;
  end

  initial begin
    x=0;y=0;
```

```
    #200 x=1;
    #200 x=0;y=1;
    #200 x=1;
    #200
    $finish;
  end

endmodule
```

Waveform