#100rtldays Challenge
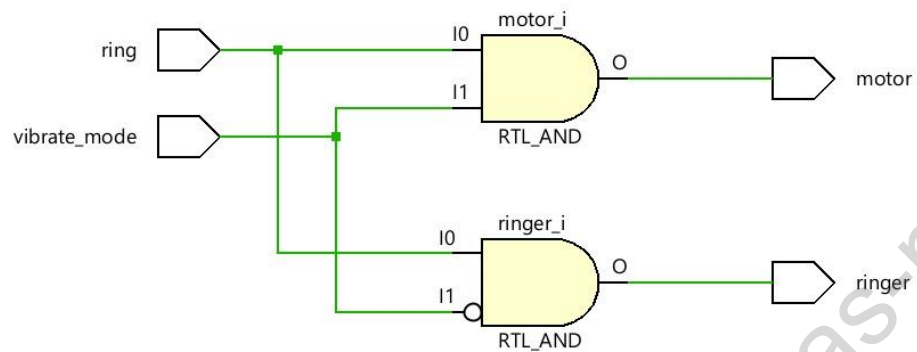## EXPERIENCE THE JOY OF LEARNING

#Day7: Suppose you are designing a circuit to control a cellphone's ringer and vibration motor. Whenever the phone needs to ring from an incoming call (input ring), your circuit must either turn on the ringer (output ringer = 1) or the motor (output motor = 1), but not both. If the phone is in vibrate mode (input vibrate_mode = 1), turn on the motor. Otherwise, turn on the ringer. Design this circuit.

Design

```verilog
module ring_ctrl(input ring,vibrate_mode,
                output ringer , motor
  );
  assign motor=ring&vibrate_mode;
  assign ringer=ring&(~vibrate_mode);

endmodule
```

Circuit

Testbench

```verilog
module tb;
  reg ring,vibrate_mode;
  wire ringer,motor;

  ring_ctrl a2(ring,vibrate_mode,ringer,motor);

  initial begin
    $dumpfile("test.vcd");
    $dumpvars;
  end

  initial begin
    ring=0;vibrate_mode=0;
    #200 ring=1;
    #200 ring=0;vibrate_mode=1;
    #200 ring=1;
    #200
    $finish;
  end

endmodule
```

Waveform