VLSI Design
ECE314
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M1: VLSI Technology
Lecture 1
CMOS Fabrication & Layout

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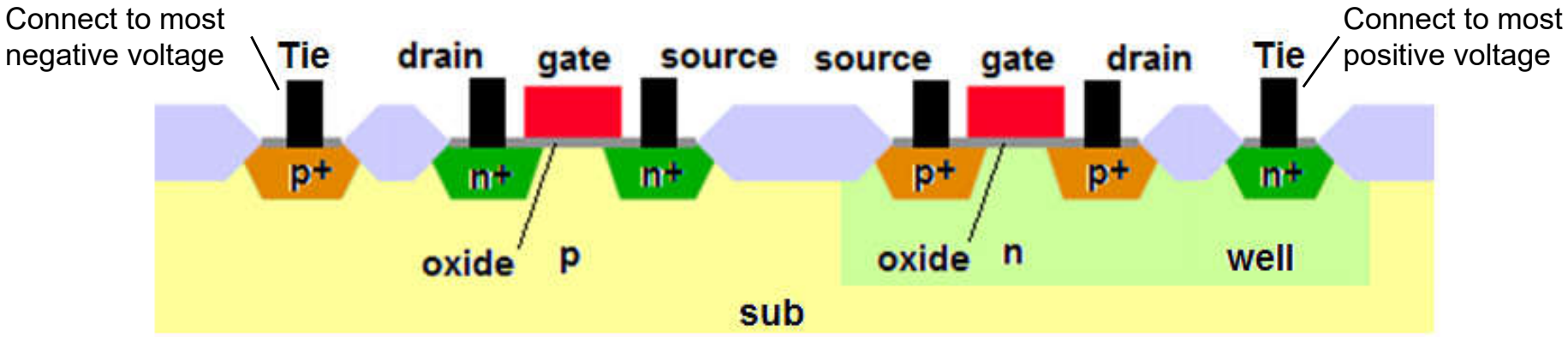
Outline

- **Introduction**
  - **What is CMOS**
  - **Why CMOS**
  - **Advanced CMOS**
  - **What's inside a Chip**
- CMOS Fabrication & Layout
- Layout & Geometric Design Rules

CMOS

- CMOS uses both NMOS and PMOS devices to realize circuits
- Wells must be used to accommodate both NMOS and PMOS on the same area (p-sub & n-well or n-sub & p-well or twin well)
- Source/drain, substrate, and well junctions must always be reverse-biased under all operating conditions
- Bulk ties are needed to bias the bulk properly (remember MOS is a 4-terminal device: source, drain, gate, and bulk)



Single Well CMOS Cross-Section

Why CMOS

- Most popular technology for realizing microcircuits
- Lower fabrication cost
- Relatively easy to reduce dimensions
- For digital circuits:
  - Consumes less power than BJT
  - Requires fewer devices than BJT
- For analog circuits:
  - Slower and noisier than the BJT

    (speed is getting more comparable in recent technologies)

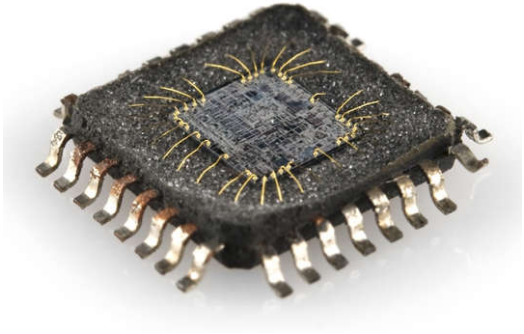
Advanced CMOS

Further improvements are continuously added to CMOS

- Triple-well CMOS
- Strained-Silicon CMOS
- Silicon-on-Insulator CMOS
- Tri-gate CMOS
- Fin-FET CMOS

What's Inside a Chip

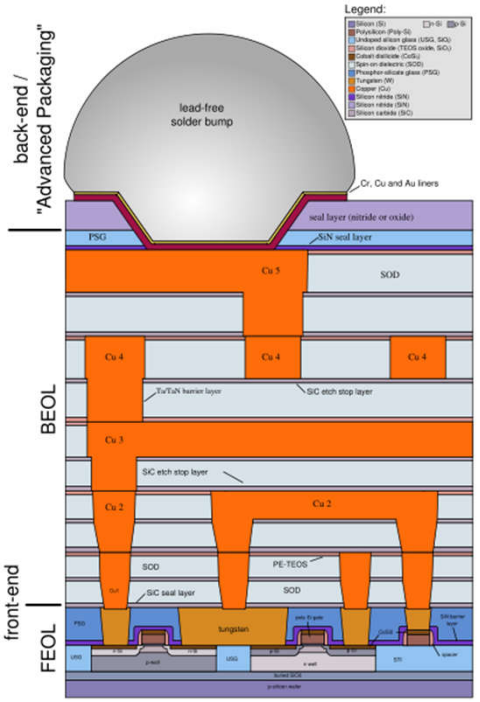
- Transistors
  - Different types of NMOS and PMOS
  - Fabricated on the silicon surface



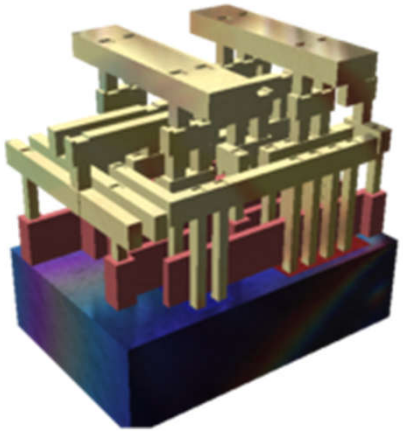
- Wires
  - Aluminum or copper wires
  - Fabricated using several patterned metal and contact layers
  - Insulator fills the remaining volume in each layer
- Passive devices (optional)
  - Integrated resistors, capacitors, inductors
  - Mainly used in analog and RF circuits

* http://en.wikipedia.org/wiki/Integrated_circuit

Cross-section showing silicon and metal layers including solder balls*



3D visualization of silicon and few metal layers (transparent insulator)*



Outline

- Introduction
- **CMOS Fabrication & Layout**
  - **Wafer Fabrication**
  - **Making Chips**
  - **Basic Processing Steps**
  - **Simplified CMOS Process Flow**
- Layout & Geometric Design Rules

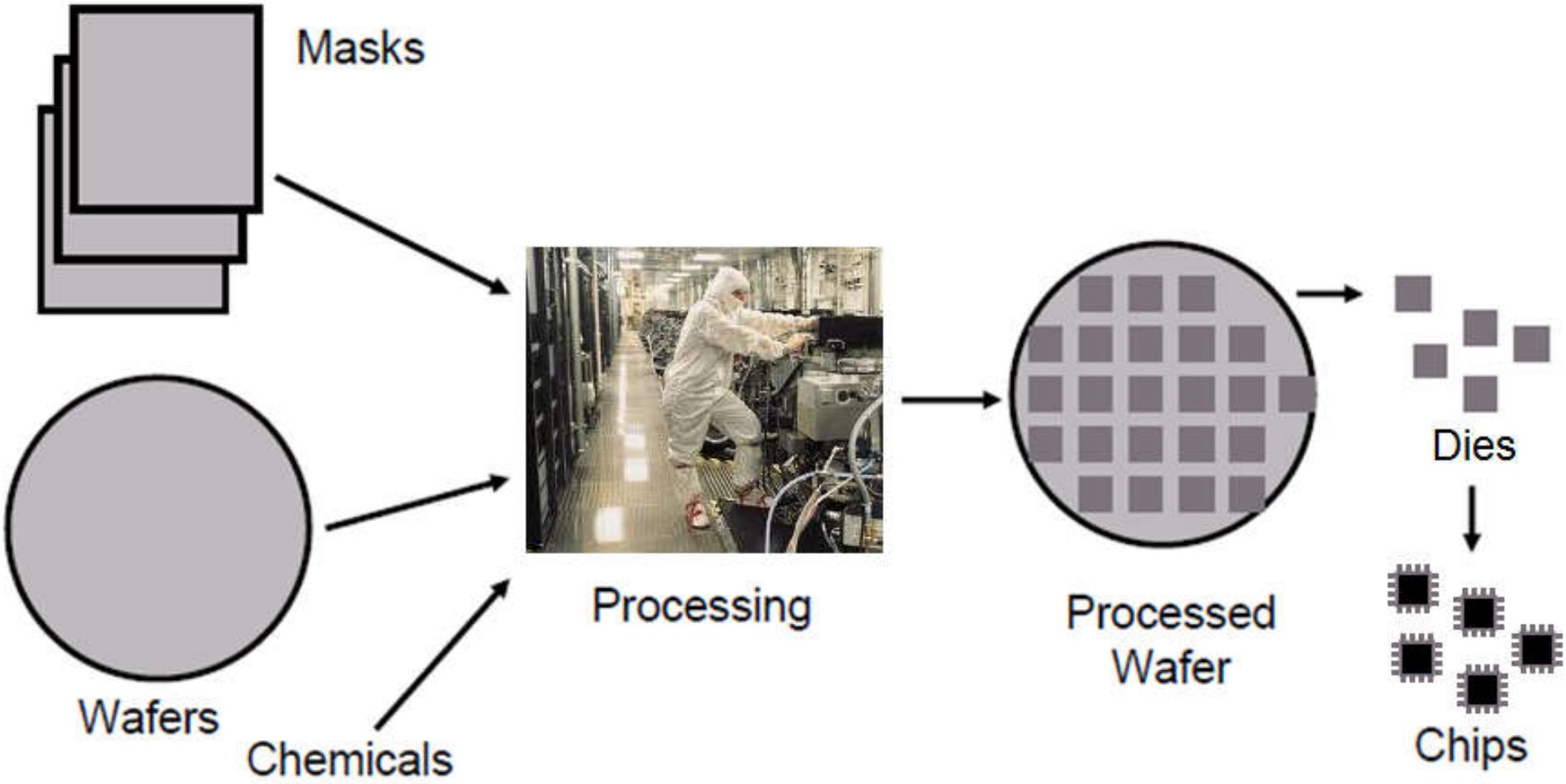
Wafer Fabrication

- Separate facility to fabricate wafers
- Si ingots are fabricated from Si seeds
- Si ingots are sliced to thin wafers
- Wafer properties:
  - resistivity 0.05 – 0.1 Ω.cm
  - diameter 10 – 30 cm
  - thickness 500 – 1000 μm

wafers

large single-crystal « ingot »

Making Chips



Making Chips

Basic Idea:

- Integrated circuits are built over wafers in a layer-by-layer fashion
- An image of the desired layer mask is transferred to the wafer (photolithography)
- That image is used as a guide to the desired fabrication step (oxidation, diffusion, ion implantation, etch, …)
- There are other blanket fabrication steps that apply to the whole wafer (deposition, metallization, polishing, annealing, …)
- Once wafers are fully processed, they are diced into dies
- Each die is packaged to become a chip
- Finally, chips are soldered on PCBs

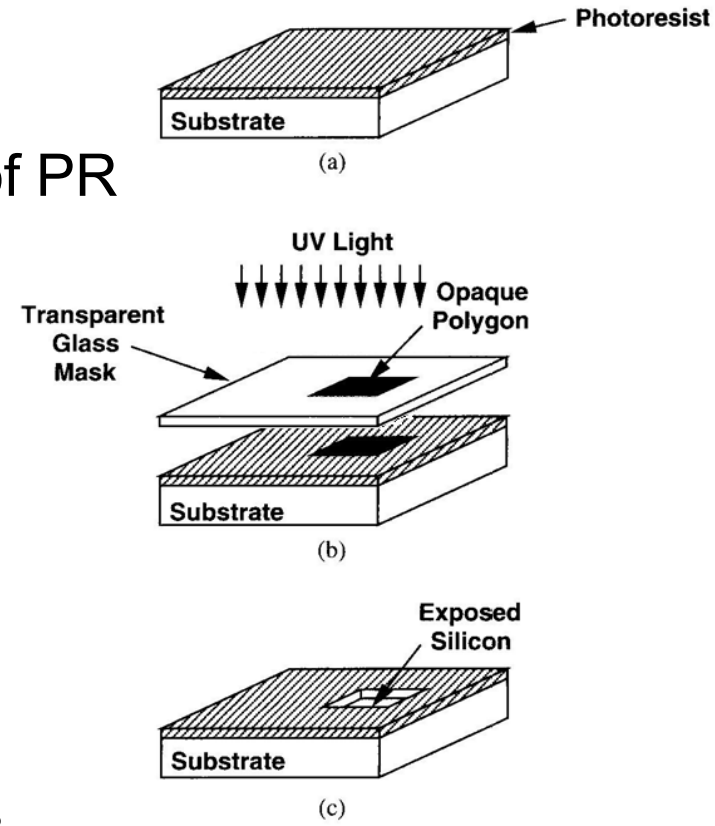
Will briefly cover some processing steps in the next few slides

Optional course is dedicated to fabrication technology

Basic Processing Steps

Photolithography

- Wafer covered with soft photoresist (PR)
- Mask exposure to harden selected areas of PR
- Soft PR dissolving to uncover surface for next processing
- Note: The hardened PR is removed after needed processing is done



- Two types of PR:
  - Negative PR: hardens in exposed areas
  - Positive PR: hardens in non-exposed areas

- Cost is proportional to the number of masks

Basic Processing Steps

Oxidation

- Exposed silicon areas oxidized in controlled temperature furnace

Diffusion

- Dopants cover the exposed silicon areas
- Dopants diffuse into silicon proportional to time
- Dopants washed off the surface

Ion Implantaion

- Dopants projected at silicon surface with selected angle/energy/dose
- Dopants penetrates silicon surface to desired depth
- Annealing step is necessary after implantation

Basic Processing Steps

Etch

- The material under exposed surface areas are etched (removed)
- Selective etch removes certain material and leave others
- Reactive ion etch removes material in the vertical direction much faster than in the planer direction

Deposition

- Material layer deposited to cover the surface of the wafer
- Selective deposition only covers surface of selected material
- It is typically patterned by a subsequent etch step

Metallization

- Metal layer sputtered to cover the surface of the wafer

Basic Processing Steps

Polishing

- The surface of the wafer is polished to make it even (planer)
- Chemical mechanical polishing is often used

Annealing

- Wafers placed in in controlled temperature furnace with inert ambient or vacuum for some time
- Typically used after ion implantation to heal damage and diffuse dopants

Simple Flow - Making Transistors

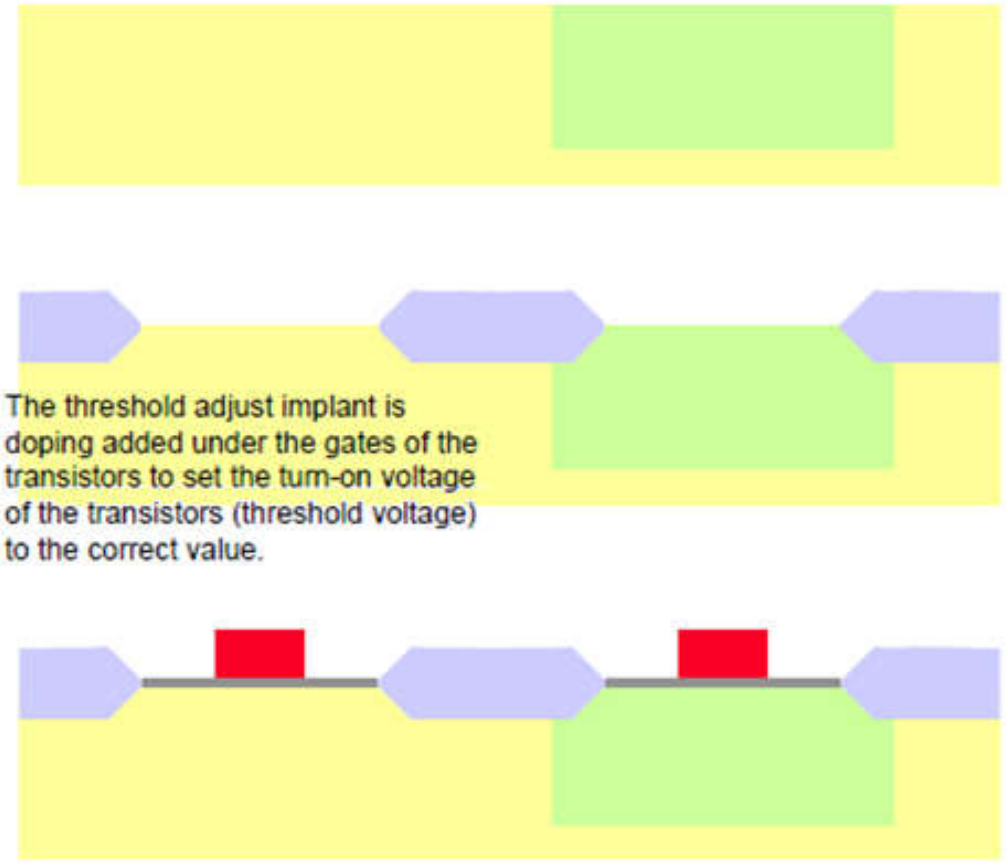
Steps Description

1. N-well creation
N-well mask litho,
N-well implant

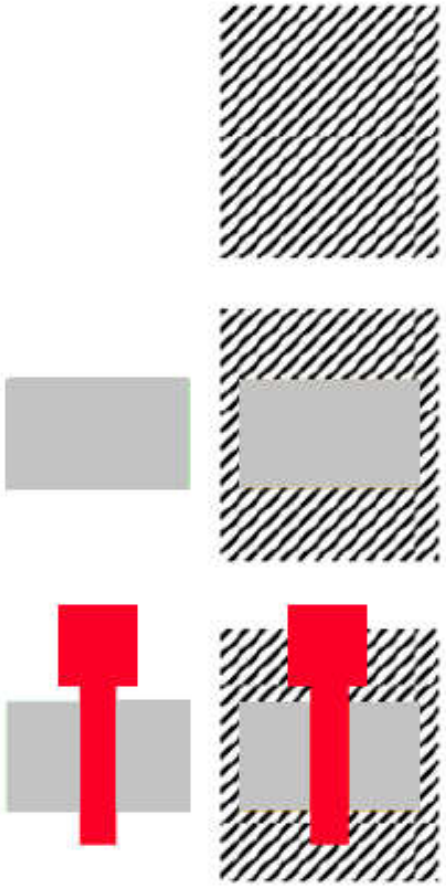
2. FOX creation
Si_3N_4 deposit,
Active mask litho,
Si_3N_4 etch, Grow field oxide, Si_3N_4 etch, Threshold adjust implants

3. Gate creation
Grow gate oxide,
Poly deposit,
Poly mask litho,
Poly etch

Cross-Section (After Steps)



Masks (Cumulative)



Simple Flow - Making Transistors

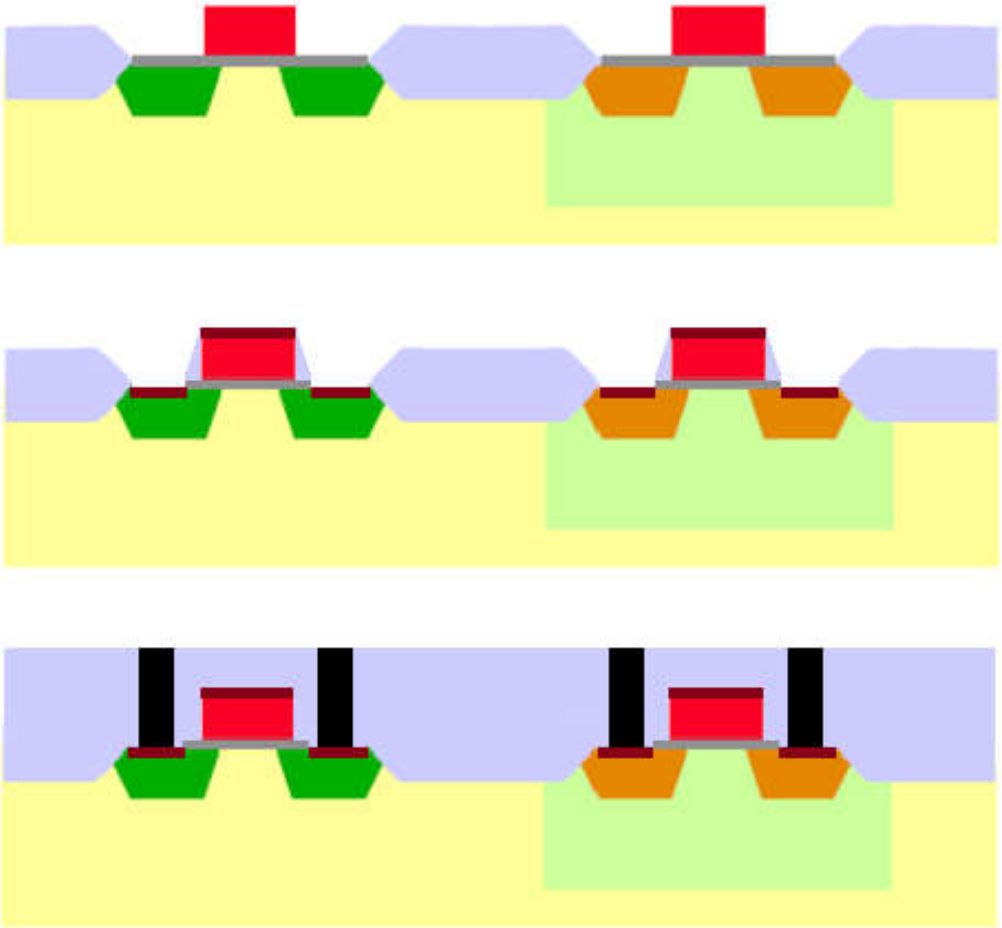
Steps Description

4. Source/drain creation
N-select mask litho, N+ source/drain implant (self-aligned), P-select mask litho, P+ source/drain implant (self-aligned)

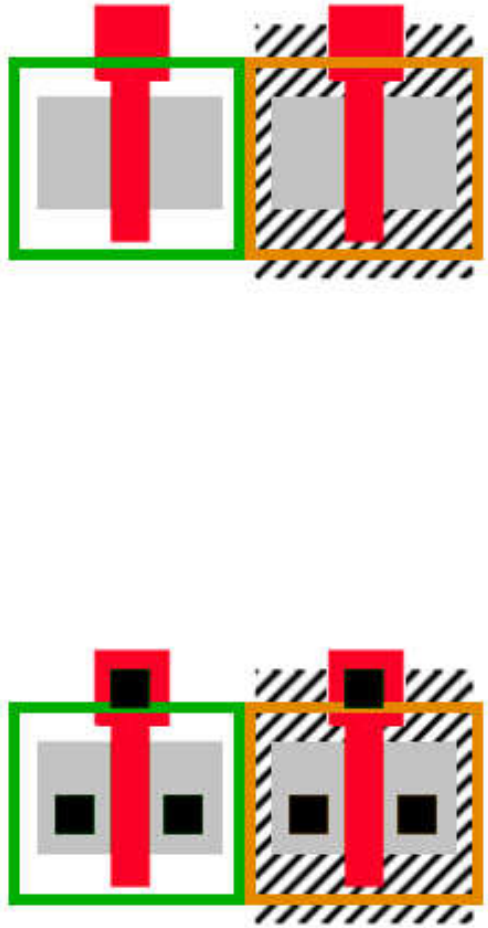
5. Salicidation
Oxide deposit, Oxide etch (gate spacer created), Ti deposit, Anneal to form $TiSi_2$, Ti etch (self-aligned salicidation)

6. Contact creation
Fill oxide deposit, Polish, Contact mask litho, Contact etch, W plug despoit, Polish

Cross-Section (After Steps)



Masks (Cumulative)



Simple Flow - Making Wires

Steps Description

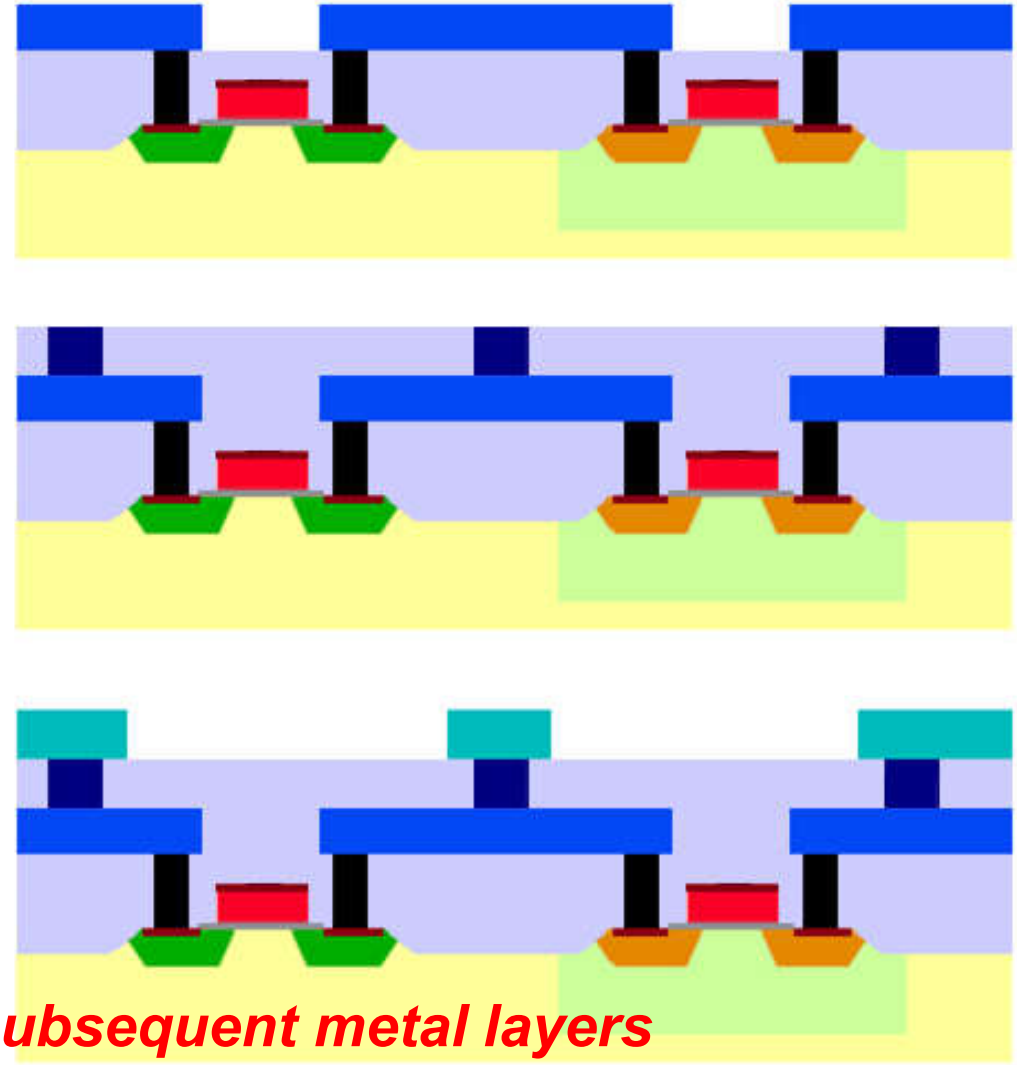
7. M1 creation
M1 Metallization,
M1 mask litho,
M1 etch

8. V1 creation
Fill oxide deposit,
Polish, Via1 mask
litho, Via1 etch,
Via1 despoit, Polish
Similar to 6

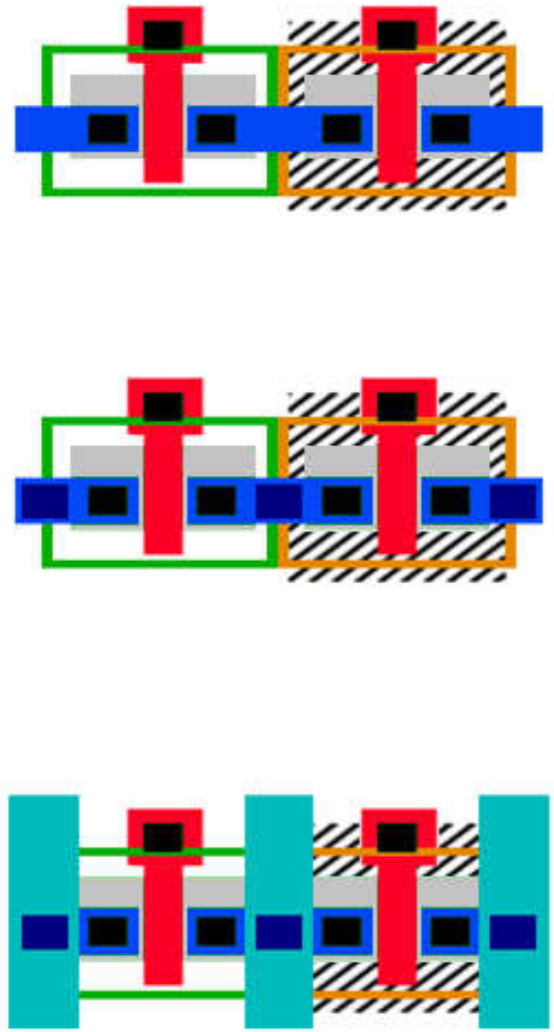
9. M2 creation
M2 Metallization,
M2 mask litho,
M2 etch
Similar to 7

Repeat 8 & 9 for subsequent metal layers

Cross-Section (After Steps)

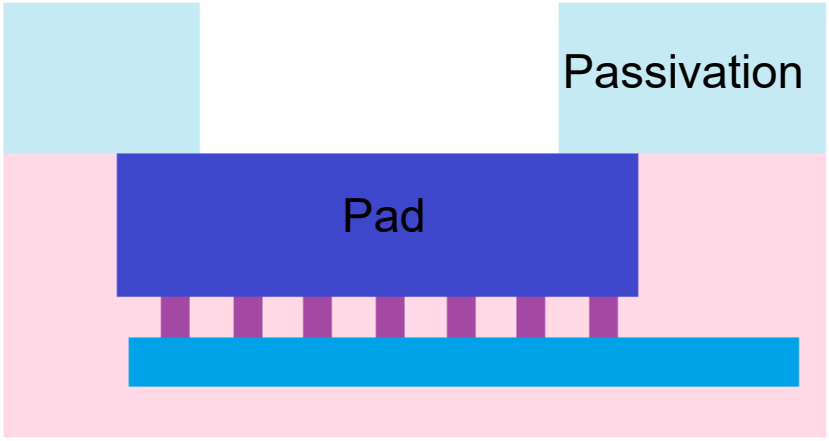


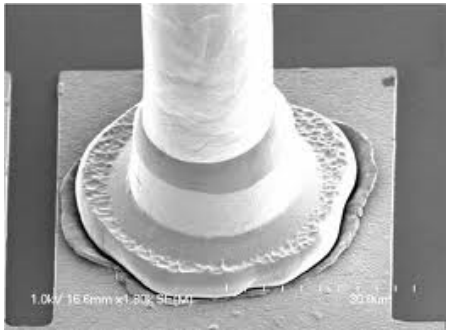
Masks (Cumulative)



Simple Flow - Passivation

- Top metal layer is dedicated to form bond pads
- Bond pads are used to electrically connect the integrated circuit supplies and I/Os to the outside world through the package pins
- Final step is to cover the wafer with a passivation layer
- Passivation seals underlying layers from moisture and contamination and protects against damage caused by subsequent dicing and handling
- Passivation mask is needed to uncover the surface over bond pads to allow external connection





Outline

- Introduction
- CMOS Fabrication & Layout
- **Layout & Geometric Design Rules**

Layout

- Process controls vertical dimensions and sets constraints on planer dimensions (mask dimensions) that are set by the design
- Layout defines colored planer geometries on different layers corresponding collectively to different masks used in fabrication (Each layer has a unique color)
- Layout editor CAD tool is used by designers to draw the layout and finally generate layers to send to fabrication in GDSII format (a process called tapeout)
- IC design is concerned with both schematic and layout "views" of the design
- Most companies have dedicated layout teams

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (diffusion)	Green	
Select diffusion (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Layout Geometric Design Rules

- Fabrication process places many constraints on the layout
- A set of geometric design rules guarantees proper fabrication
- In general, two main categories of constraints:
  1. Resolution constraints

     Smallest width and spacing to margin for variations
  2. Overlap constraints

     Smallest extension and spacing to margin for alignment mismatch
- Two ways to define geometric design rules:
  1. Scalable rules:

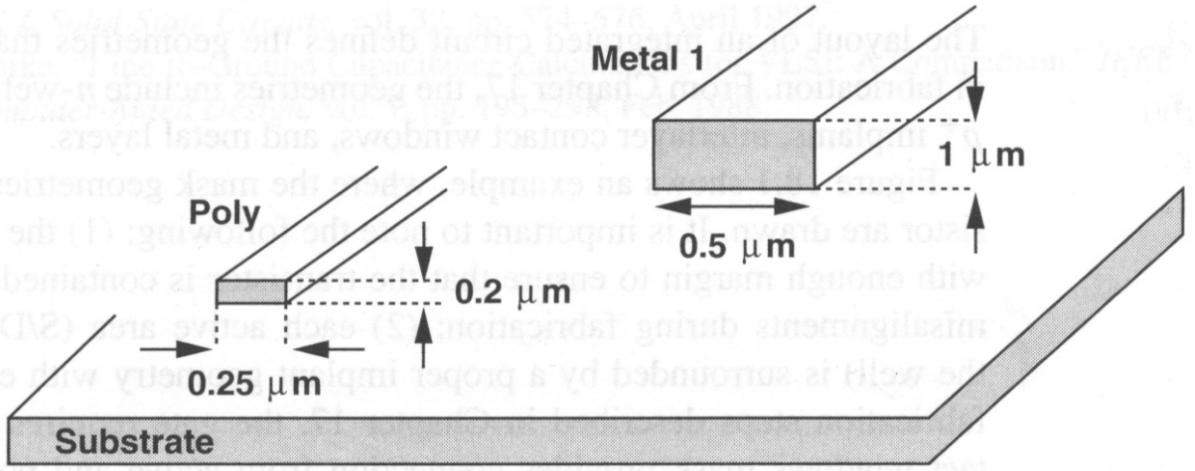
     All dimensions in multiples of λ (min gate poly line width = 2λ)

     As technology scales, changing λ would change all rules
  2. Absolute rules:

     All dimensions in metric system

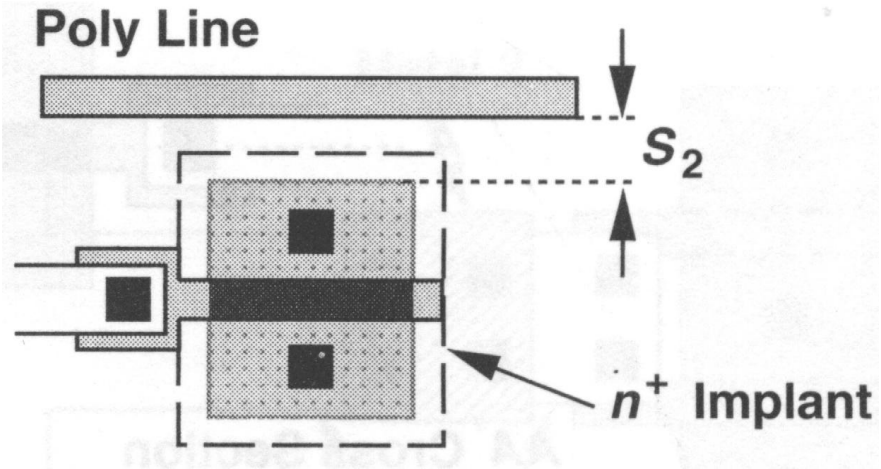
Minimum Width Rules

- Dimensions must be equal or greater than minimum values
- Minimum values are imposed by the processing capabilities of the target technology



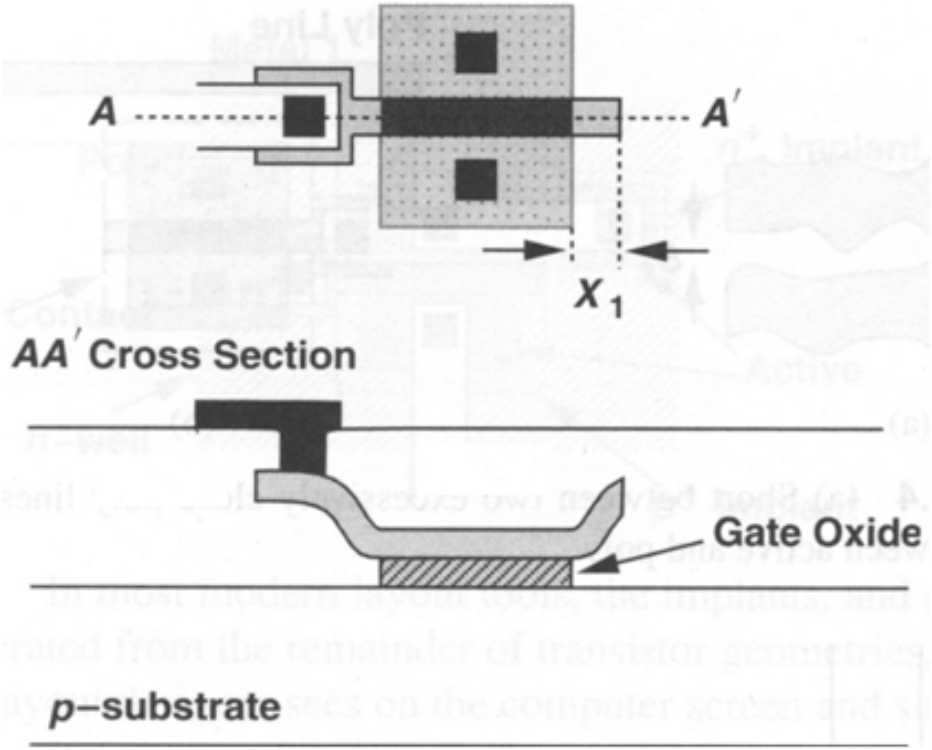
Minimum Spacing Rules

- The same argument applies for spacing
- Dimensions must be equal or greater than minimum values
- On the same layer: Minimum values are imposed by the processing capabilities of the target technology
- On different layers: Minimum values are imposed to avoid parasitic devices or undesired connection



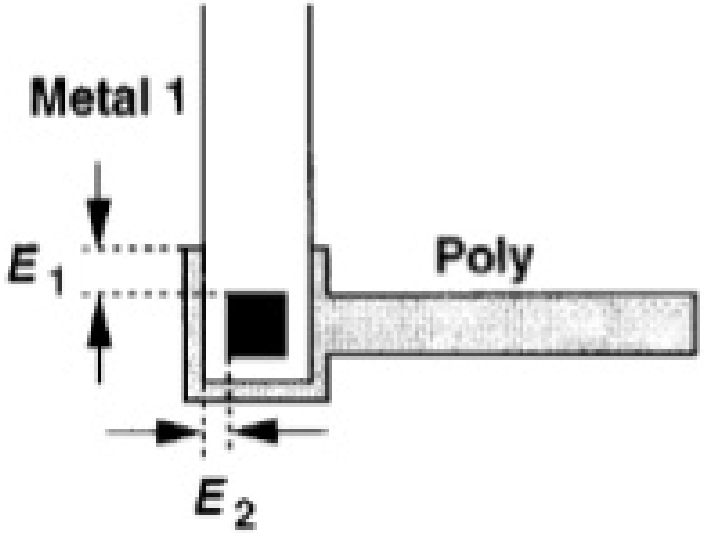
Minimum Extension Rules

- Some geometries must extend beyond the edge of others by a minimum value to margin for misalignment
- EG: Gate poly must extend beyond active-area by a minimum value to ensure proper gate control at the edge



Minimum Enclosure Rules

- Geometry enclosure means that an inner geometry is completely inside another outer geometry
- Enclosure rules set a minimum distance between the inner geometry and the outer geometry to margin for misalignment
- EG: Active-area edge distance to well edge, active-area edge distance to n/p select edge, and contact/via edge distance to metal edge



Links

- Foundries (Fabs):
  - TSMC: http://www.tsmc.com/
  - Global Foundries: http://www.globalfoundries.com/
- Interface to Foundries:
  - CMP: http://cmp.imag.fr/
  - MOSIS: http://www.mosis.com/
- CAD Companies:
  - Synopsys: http://www.synopsys.com/
  - Cadence: http://www.cadence.com/
  - Mentor Graphics: http://www.mentor.com/

References

- Rabaey, chapter 2