Mohammad Haris Minai

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Summary:

- Thrives on learning and exploring new technologies and ideas.
- Self-starter, quick learner & works well independently and as a team member.
- More than 13 years of experience in the VLSI Semiconductor industry.
- Excellent analytical, problem solving and communication skills.
- Exposure in a team leadership role.
- Willing to travel moderately.

Education:

- **BTech in Electronics Engineering, 1998**, Zakir Hussain College of Engineering and Technology, Aligarh Muslim University, Aligarh, Uttar Pradesh, India
- **Fellow Programme in Management, 2016 (expected)**, Indian Institute of Management, Lucknow, Uttar Pradesh, India

Work Experience

Organization	Designation	Duration
Freescale Semiconductors (FSL) Noida, India	*Applications Engineering Manager*	2010 – 2012
Freescale Semiconductors (FSL) Noida, India	*Applications Engineer*	2009 – 2010
Freescale Semiconductor (FSL) Noida, India	*Design Manager*	2006 – 2009
Freescale Semiconductor (FSL) Noida, India	*IC Design Engineer II*	2005 – 2006
Texas Instruments (TI) Bangalore, India	*Lead Engineer*	2004 – 2005
Interra Systems India Pvt. Ltd, Noida, India	*Senior Design Engineer*	2003 – 2004
Cogency Semiconductor Inc., Toronto, Canada	*ASIC Design Engineer*	2001 – 2003
Tundra Semiconductors, Ottawa, Canada	*Emulation Engineer*	2001 – 2001
STMicroelectronics (STM) Noida, India	*Team Leader*	1999 – 2001
STMicroelectronics (STM) Noida, India	*Design Engineer*	1998 – 1999

Technical summary:

Hardware Design: HDL based design and verification, targeting both ASICs and FPGAa.

- Excellent Digital Design Skills.
- Proficient in Verilog, Synthesis Tools, ASIC Design and Debug and FPGA Implementation Tools.

HDL Exposure: Verilog, VHDL, SystemVerilog, Bluespec SystemVerilog

Embedded Systems Design: Have developed and debugged hardware and software

- PowerPC based systems for NAS, Networking and Consumer Electronics
- Nios II microprocessor based Systems on a Programmable Chip (SOPC) using Cyclone III FPGAs
- 8051 microcontroller based systems

Prototyping: Experience in prototyping complex designs using FPGAs.

Emulation: Emulation of complex digital designs on Quickturn's Mercury™ emulation platform.

Scripting languages: perl, gawk, bash, tcsh and tcl/tk

Selected Accomplishments:

Design Related:

- Was Applications Engineering manager for Networking Products Division in India Design Centre of Freescale. Responsible for all customer collateral and support for all SoCs released out of the division in India. Have a team of six engineers working with me on this. (FSL)
- Applications Engineer for Freescale's latest dual PowerPC core (QorIQ) based SoCs. The primary end markets of this SoC are printing, digital signage and NAS applications. Was personally responsible for the Hardware Specifications, Design Guidelines and Customer support for all (Hardware and Software) issues of a highly integrated printing SoC. (FSL)
- Led a team of eight in the design and development of a low power, small footprint, 3-axis digital accelerometer SoC (the first product of the Xtrinsic family) which has a ColdFire Processor, Flash, ROM and RAM memories with associated controllers, multiple timers, I2C/SPI slave interface and other peripherals. I owned and was responsible for all aspects of the digital design and verification, integration with analog as well as applications suite development. (FSL)
- Led a team of seven engineers to perform the micro-architecture, design and development of a Mobile Industry Processor Interface (MIPI) SLIMbus standard interface IP. Was personally responsible for the Timing Control Unit and the Clock and Reset Unit. (FSL)
- Participated in architecting and designing a DigRF3G standard interface IP for use with Freescale's mobile handset baseband SoCs. Was personally responsible for designing the Framer, Memory interface and PISO (Parallel In Serial Out) controller. Also had joint responsibility of the synthesis effort. (FSL)
- Led the frontend effort for two derivatives of TI's DSP memory subsystem based on the award winning C55x DSP IP. Personally responsible for designing the cache subsystem. (TI)
- Independently designed, coded and verified an OFDM (Orthogonal Frequency Division Multiplexing) tone modulator, for HomePlug2.0 candidate VIPER ASIC. (Cogency)
- Independently designed, coded and verified the USB interface of HomePlug1.0 compatible PHANTOM ASIC. USB core was integrated as an IP. PHANTOM SoC silicon was proven on reference design. (Cogency)
- Led a team and participated in the architecture definition and coding of a USB/PCI based ADSL modem. Architected the USB controller and the USB/ADSL interface. (STM)
- Designed, developed and verified a (2,1/2) viterbi decoder. Implemented on Xilinx Virtex, Altera Flex10K and ASIC libraries to provide benchmarking. (STM)

Methodologies related:

- Modeled, implemented and verified a cache coherence protocol using BlueSpec SystemVerilog. Did comparative studies with respect to hand written RTL for lines of code, performance and area on ASIC library. (Interra)

- Performed FPGA validation of SLIMbus IP on Altera using Nios II processor. The processor was implemented on FPGAs and interfaced with the SLIMbus IP then validated to work on a reference board. (FSL)
- Led a team of twelve engineers in the partitioning, mapping and verification of the Instruction Unit, Bus Interface Unit and Floating Point unit of a pentium class microprocessor on Lucent's ORCA 3 series FPGAs. (STM)
- Was an active member of IPDesign Core Team, which was a global, multi-site grouping of people mandated with improving the quality and reusability of IP developed by Freescale's design centers located across the world. Had primary ownership of the "memory policy" and the "RTL Compiler policy". (FSL)
- Guided and mentored an effort to develop a serial protocol analyzer using the graphical and scripting capabilities for Tcl/Tk. Attempted to make the protocol analyzer as generic as possible but the effort was specifically targeted towards the SLIMbus protocol. (FSL)
- Was responsible for consultative development and deployment of various power reduction techniques during frontend design. Techniques included isolation with multiple power domains, multi-VT and aggressive clock gating. (TI)
- Made the testbench for DFT for the PHANTOM ASIC. ARM DFT vectors were ported for which scripts were written in perl and gawk. (Cogency)
- Developed methodology for measurement of BlueSpec SystemVerilog RTL generation capabilities, specifically as regards synthesis by Design Compiler. (Interra)
- Developed and generated bitstreams for designs to be used with a handcrafted semi-custom softmodel of a new FPGA architecture, developed under my guidance. This enabled swift decision making on architectural features to be incorporated in the FPGA. (STM)
- Led and participated in the evaluation of FPGA Toolset and Architecture under development by Software Group. Gave competitive information on Toolsets of competitors (Xilinx and Altera) and provided suggestions for improvement. Benchmarked performance and area requirements against competitor devices. Arranged for the benchmark designs and developed comparison methodology. (STM)

Published Work

1. M. Ajmal, A. Samad, and M.H. Minai, ***"Basics of FPGA design in context with AES algorithm,"*** proceedings of national conference on Emerging Technologies NCET-08 Lucknow, pp. 313-318, March 29th – 30th, 2008.

2. Kafeel M.A and Minai H., ***"FPGA based AES Hardware implementation for secure management of systems"***, proceedings of the All India seminar on communication convergence, institution of engineers, Lucknow, India, September 8th - 9th, 2007.

Mentoring Activities

- Guest lecture on "Hardware accelerators for Network Security" at University Women's Polytechnic, Aligarh Muslim University on the occasion of a workshop on "Network Security and Applications" held in collaboration with Institute of Engineers.
- Training on Verilog Hardware Description Language to 2007 and 2008 batch of fresh recruits. (FSL)
- Drove and participated in PowerPC processor training to Applications Engineers. (FSL)
- Guided interns for final year projects
  - Establishment of a verification flow for Clock Domain Crossing checks using formal tools
  - Development of algorithms for use of a 3 axis accelerometer in mobile handsets