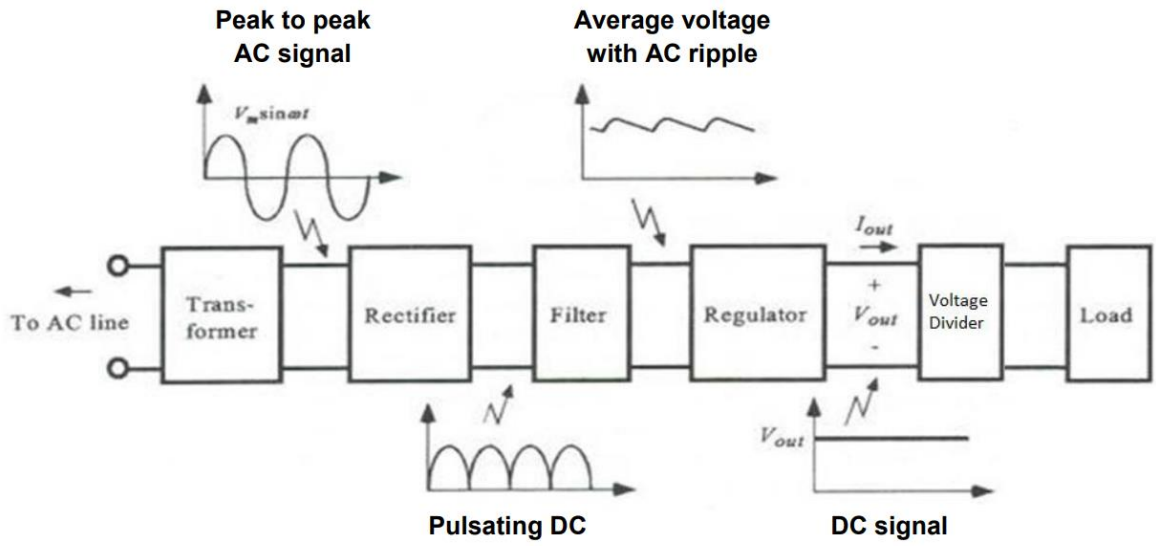
ELECTRONIC CIRCUIT

- Block Diagram DC Power Supply



- Ideal Power Equation
- Turns Ratio:

$$Turns\ ratio = \frac{N_P}{N_S} = \frac{V_P}{V_S}$$

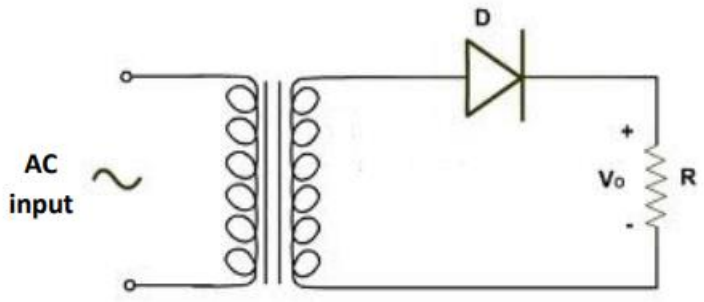
Vp = Primary Voltage
Np = Number of turns on primary coil
Vs = Secondary Voltage
Ns = Number of turns on secondary coil

- Outgoing Power:

$$P_{in} = P_{out}, \qquad I_p V_p = I_s V_s, \qquad \frac{V_P}{V_S} = \frac{I_S}{I_P}$$

Ip = Primary Current
Is = Secondary Current

- Rectifier
- Half wave Rectifier



i. Output Voltage:

$$V_{out} = \frac{V_{pp(\text{sec})}}{2} - 0.7V$$

ii. Average Voltage

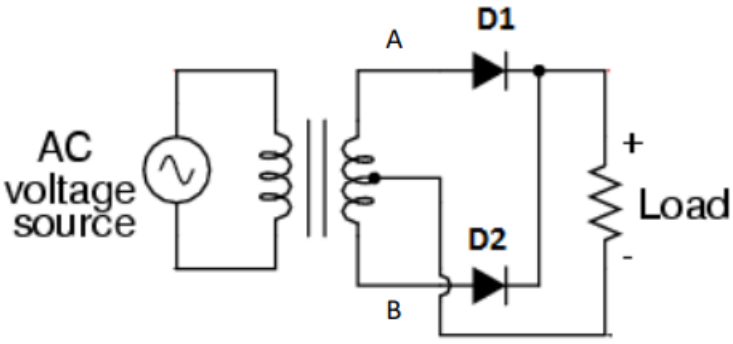
$$V_{avg} = 0.318\, V_{out}$$

iii. Frequency

$$f_{out} = f_{in}$$

- Full wave Rectifier

a) Center-tapped full wave rectifier:



i. Output Voltage

$$V_{out} = \frac{V_{p(\text{sec})}}{2} - 0.7V;\ \ where\ V_{p(\text{sec})} = \frac{V_{pp(\text{sec})}}{2}$$

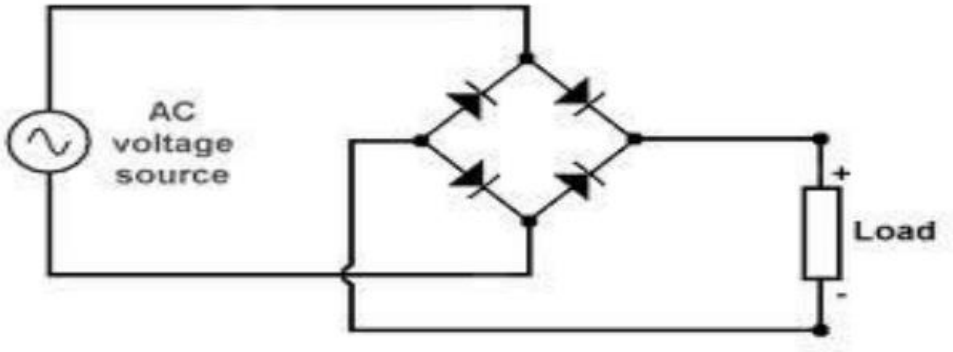
ii. Average Voltage

$$V_{avg} = 0.637\ V_{out}$$

iii. Frequency

$$f_{out} = 2f_{in}$$

b) Bridge Rectifier



i. Output Voltage

$$V_{out} = \frac{V_{pp(\text{sec})}}{2} - 1.4V$$

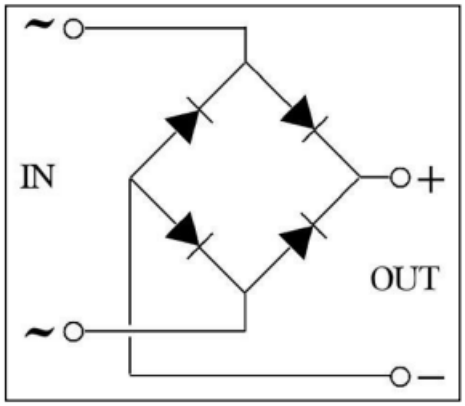
ii. Average Voltage

$$V_{avg} = 0.637\ V_{out}$$

iii. Frequency

$$f_{out} = 2f_{in}$$

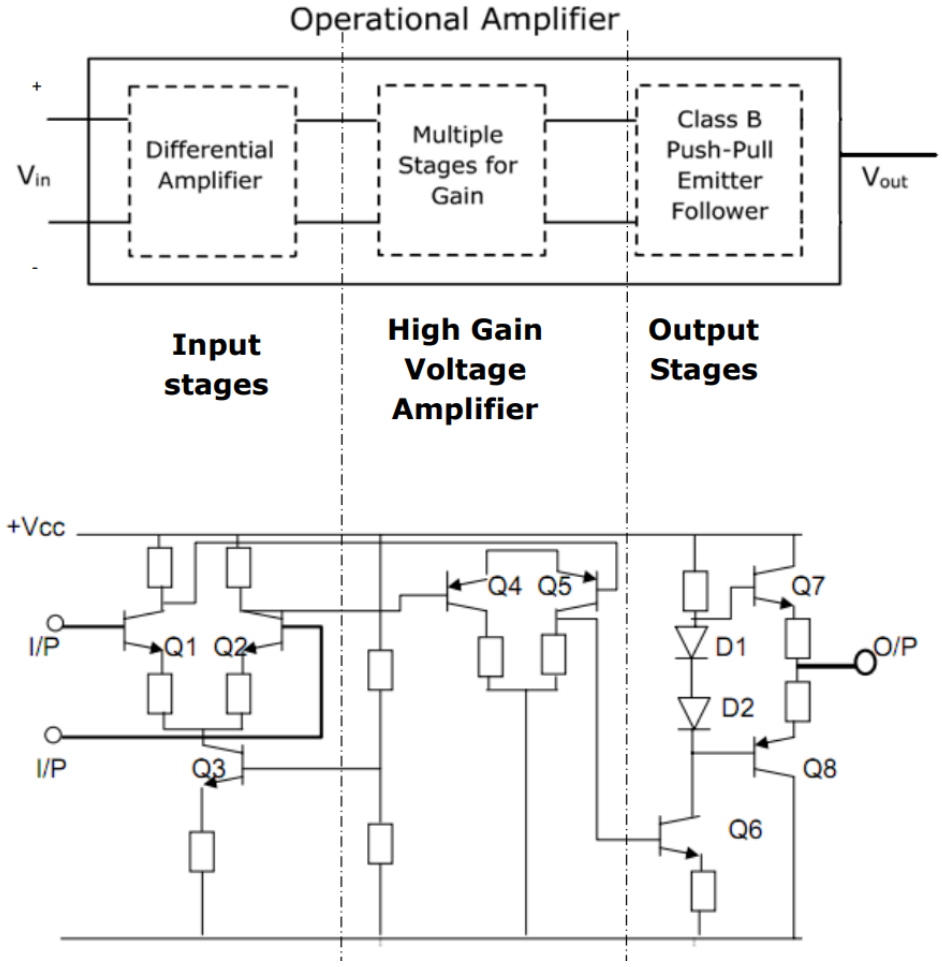
c) Bridge Rectifier IC



- Voltage Gain

$$Voltage\ Gain, A = \frac{V_{out}}{V_{in}}$$

- Block Diagram Of Op Amp



- Open Loop Gain

$$A_{OL} = \frac{V_{out}}{0}$$

- Impedance

$$Z = \frac{V}{I}$$

(Unit: Ohm)

- Input Bias Current

$$I_B = \frac{(I_{B1} - I_{B2})}{2}$$

- Input Offset Current

$$I_{OS} = |I_{B1} - I_{B2}|$$

- Common-Mode Rejection Ratio (CMRR)

$$CMRR = \frac{Differential\ Gain, A_d}{Common - mode\ Gain, A_c}$$

$$CMRR\ (dB) = 20\ \log_{10} \frac{A_d}{A_c}$$

- Inverting Amplifier

  Gain:

$$A = -\frac{R_F}{R_1}$$

  Output Voltage:

$$V_{out} = -\frac{R_F}{R_1}(V_{in})$$

- Non-Inverting Amplifier

  Gain:

$$A = \frac{R_G + R_F}{R_G}$$

  Output Voltage:

$$V_{out} = \left(1 + \frac{R_F}{R_G}\right) V_{in}$$

- Summing Amplifier

  Output Voltage:

$$V_{out} = -\left[\frac{R_f}{R_1}(V_1) + \frac{R_f}{R_1}(V_2) + \cdots \frac{R_f}{R_n}(V_n)\right]$$

- Subtractor/Difference Amplifier

  Output Voltage:

$$V_{out} = -V_1\left[\frac{R_F}{R_A}\right] + V_2\left[\frac{R_{IN}}{R_B - R_{IN}}\right]\left[\frac{R_A + R_F}{R_A}\right]$$

When $R_A = R_B$ and $R_F = R_{IN}$;

$$V_{out} = \frac{R_F}{R_A}(V_2 - V_1)$$

If unity gain; $R_A = R_F$;

$$V_{out} = V_2 - V_1$$

- Differentiator Amplifier

  Output Voltage:

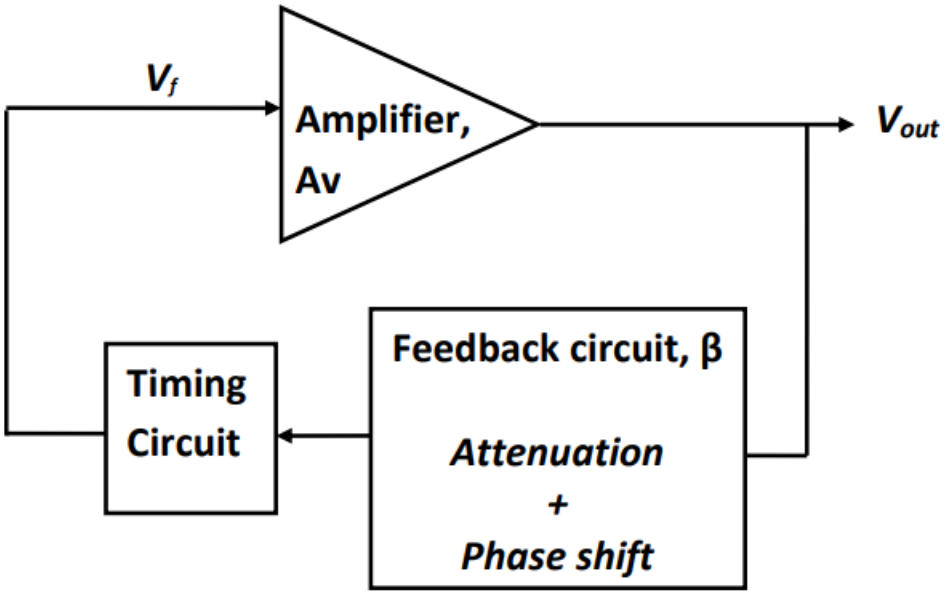
$$Vo(t) = -RC\frac{dVi}{dt}$$

- Integrator Amplifier

  Output Voltage:

$$Vo(t) = -\frac{1}{RC}\int Vi\ dt$$

- Oscillator Block Diagram



- Closed Feedback Loop Gain

$$Acl = A_v \times \beta$$

- Phase Shift Oscillator

  Oscillation Frequency:

$$f_r = \frac{1}{2\pi RC\sqrt{2N}}$$

  The Attenuation:

$$\beta = \frac{R}{R_f}$$

  The Voltage Gain:

$$A = \frac{R_f}{R}$$

- Colpitts Oscillator

  Operating Frequency:

$$f = \frac{1}{2\pi\sqrt{LC_T}}$$

  Total Capacitance:

$$Xc_T = Xc_1 + Xc_2$$

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

  The Attenuation:

$$\beta = \frac{V_f}{V_{out}} = \frac{Xc_1}{Xc_2}$$

- Hartley Oscillator

  Oscillation Frequency:

$$f = \frac{1}{2\pi\sqrt{L_T C}}$$

  Total Inductance:

$$L_T = L_1 + L_2$$

  The Attenuation:

$$\beta = \frac{V_f}{V_{out}} = \frac{X_{L1}}{X_{L2}}$$

- Armstrong Oscillator

  Operating Frequency:

$$f = \frac{1}{2\pi\sqrt{L_{pri} C_1}}$$

- Series Resonance Mode

  Series Resonant Frequency:

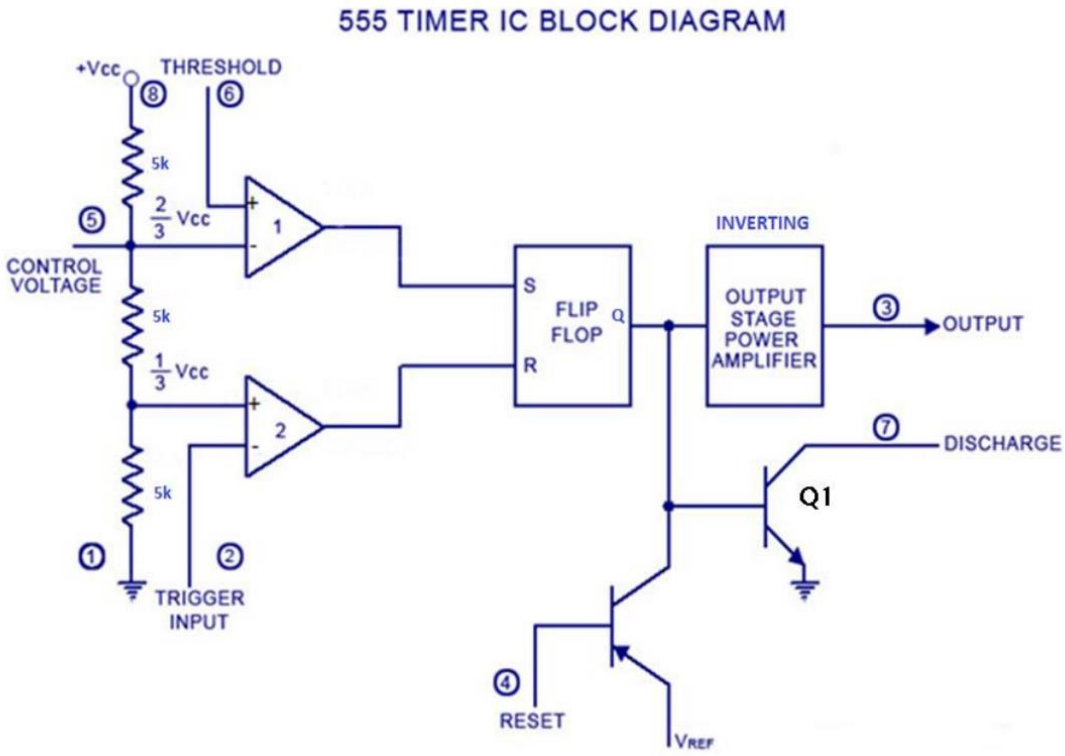
$$f_s = \frac{1}{2\pi\sqrt{LC_s}}$$

- Parallel Resonant Mode

  Oscillation Frequency:

$$f_a = \frac{1}{2\pi\sqrt{L\frac{C_s C_p}{C_s + C_p}}}$$

- 555 Timer IC Block Diagram



- Monostable Mode

$$T_W \approx 1.1\, R_A C$$

- Astable Mode

  Time High:

$$T_H = 0.693(R_A + R_B)C$$

  Time Low:

$$T_L = 0.693(R_B)C$$

  Duty Cycle:

$$D = \frac{T_H}{T_H + T_L}$$

  Total Period:

$$T = T_H + T_L$$

Astable Frequency:

$$F = \frac{1}{T}$$

Mark to Space Ratio

$$Mark\ to\ Space\ Ratio = \frac{T_H}{T_L}$$

- Cut-Off Frequency

$$20\ \log\left(\frac{V_o}{V_i}\right)$$

$$20\ \log 0.707 = -3dB$$

a) For RC circuit:

$$f_c = \frac{1}{2\pi RC}$$

b) For RL circuit:

$$f_c = \frac{R}{2\pi L}$$

- Bandwidth Frequency

$$BW = f_{OH} - f_{OL}$$

- Cut-Off Frequency for Bandpass Filter

$$f_{c1} = \frac{1}{2\pi R_1 C_1}$$

$$f_{c2} = \frac{1}{2\pi R_2 C_2}$$

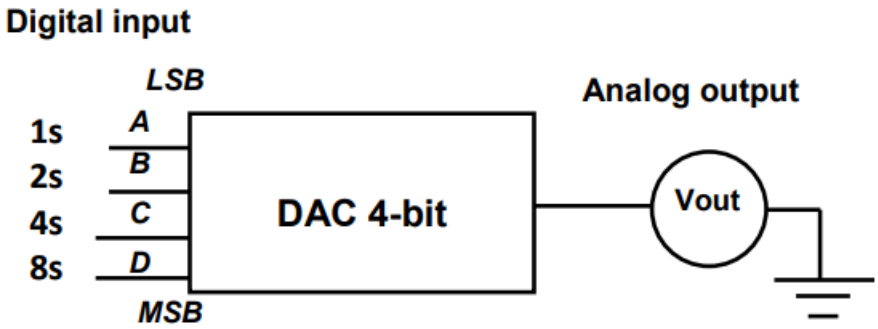
- Second Order Passive Low Pass Filter

$$f_{OH} = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

- Second Order Passive High Pass Filter

$$f_{OL} = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

- Block Diagram Of DAC



- Resistor Network

a) The binary-weighted DAC

If the input is applied to inverting terminal:

$$V_{out} = -\left[\frac{R_F}{R}(V_1) + \frac{R_F}{2R}(V_2) + \frac{R_F}{4R}(V_3) + \cdots \frac{R_F}{2^{(N-1)}}(V_N)\right]$$

If the input is applied to non-inverting terminal:

$$V_{out} = +\left[\frac{R_F}{R}(V_1) + \frac{R_F}{2R}(V_2) + \frac{R_F}{4R}(V_3) + \cdots \frac{R_F}{2^{(N-1)}}(V_N)\right]$$

b) R/2R Ladder DAC

If the input is applied to inverting terminal:

$$V_{out} = -\frac{V_{ref}}{2^n} \times B_{in} \times \frac{R_f}{R}$$

If the input is applied to non-inverting terminal:

$$V_{out} = \frac{V_{ref}}{2^n} \times B_{in} \times \frac{R_f}{R}$$

- DAC Specification

Analog Output:

$$Vout = K \times digital\ input$$

Where K is step size.

Step size = analog output for lowest digital word

Full Scale:

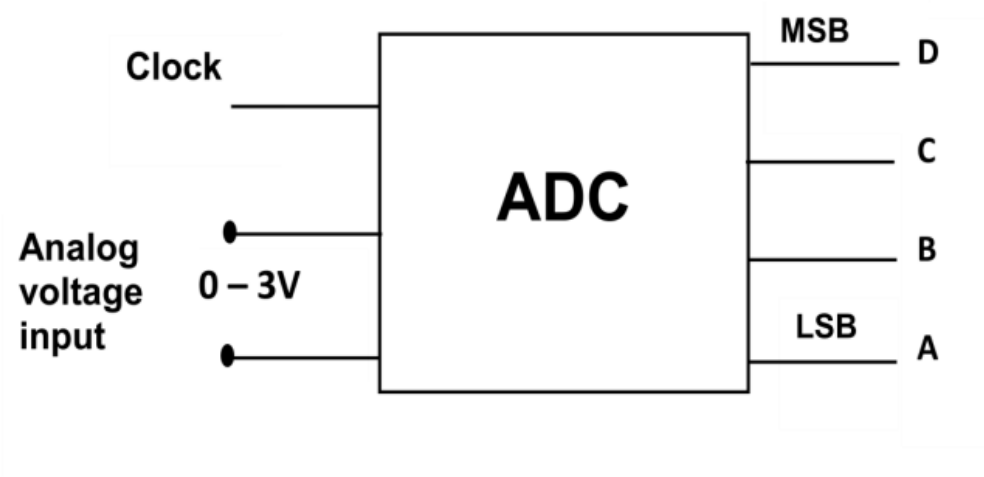
$$Full\ scale = Number\ of\ steps \times step\ size$$

$$= (2^n - 1) \times step\ size$$

% Resolution

$$\%\ resolution = \frac{Step\ size}{Full\ scale} \times 100\%$$

- Block Diagram Of ADC



- Conversion Time for DRC

$$Conversion\ Time = Number\ of\ steps \times T$$

$$Maximum\ conversion\ time = Maximum\ number \times T$$
$$= (2^n - 1) \times T$$

- Conversion Time for SAC

$$n\ bit\ conversion\ time = n \times T$$