# Structural Hazard

Stall the pipeline:

If the memory stage uses the address bus, the fetch stage will issue control signals of “NOP” instruction without incrementing the PC.

# Data Hazard

## EX hazard (EX to EX forwarding)

If(EX/MEM.RW AND (EX/MEM.Rd == ID/EX.Rs))

Forward EX/MEM.Rd data

## MEM hazard (MEM to EX forwarding)

### Case1 (Forward from ith instruction to (i+1)th instruction):

If(MEM/WP.RW AND (MEM/WP.Rd == ID/EX.Rs))

Forward MEM/WP.Rd data

### Case2 (Forward from ith instruction to (i+2)th instruction):

If(MEM/WP.RW AND NOT(EX/MEM.RW) AND (EX/MEM.Rd != ID/EX.Rs))

Forward MEM/WP.Rd data