# Structural Hazard

Stall the pipeline:

If the memory stage uses the address bus, the fetch stage will issue control signals of “NOP” instruction without incrementing the PC.

# Data Hazard

## EX hazard (EX to EX forwarding)

If(EX/MEM.RegWrite AND (EX/MEM.Rd == ID/EX.(Rs/Rd)))

Forward EX/MEM.Rd data

## MEM hazard (MEM to EX forwarding)

### Case1 (Forward from ith instruction to (i+1)th instruction):

If(MEM/WP.RegWrite AND (MEM/WP.Rd == ID/EX.(Rs/Rd)))

Forward MEM/WP.Rd data to

### Case2 (Forward from ith instruction to (i+2)th instruction):

If(MEM/WP.RegWrite AND NOT(EX/MEM.RegWrite) AND (EX/MEM.Rd != ID/EX.(Rs/Rd)))

Forward MEM/WP.Rd data

### Case3 (Load-case)

If(ID/EX.MemRead AND (ID/EX.Rs = IF/ID.(Rs/Rd)))

Stall the pipeline

## Control Hazard

Approach: Not Taken static prediction.

Evaluation in Decode stage.