# Computer Architecture II project phase 1

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| --- | --- | --- |
| Name | BN | Sec |
| محمد حسانين محمد | 16 | 2 |
| بلال الحسينى احمد عبدالفتاح | 19 | 1 |
| احمد عطيه عبدالراضى عبدالعال | 4 | 1 |
| محمد سيد حسين عبدالرازق | 19 | 2 |

# Pipeline hazards and solutions

## Structural Hazard

Stall the pipeline:

If the memory stage uses the address bus, the fetch stage will issue control signals of “NOP” instruction without incrementing the PC.

## Data Hazard

### EX hazard (EX to EX forwarding)

If(EX/MEM.RegWrite AND (EX/MEM.Rd == ID/EX.(Rs/Rd))

Forward EX/MEM.Rd data

### MEM hazard (MEM to EX forwarding)

#### Case1 (Forward from ith instruction to (i+1)th instruction):

If(MEM/WP.RegWrite AND (MEM/WP.Rd == ID/EX.(Rs/Rd)))

Forward MEM/WP.Rd data to

#### Case2 (Forward from ith instruction to (i+2)th instruction):

If(MEM/WP.RegWrite AND (MEM/WB.Rd = ID/EX.Rs) AND NOT(EX/MEM.RegWrite) AND (EX/MEM.Rd != ID/EX.(Rs/Rd)))

Forward MEM/WP.Rd data

#### Case3 (Load-case)

If(ID/EX.MemRead AND (ID/EX.Rs = IF/ID.(Rs/Rd)))

Stall the pipeline

Note: In case of MemWrite signal asserted the check should be on the X.Rd (destination register) otherwise X.Rs.

## Control Hazard

Approach: Not Taken static prediction.

Evaluation in Decode stage.

## Instruction bits details

## Registers

10

4 bits

R0 (0000) to R7 (0111), PC (1000), SP (1001)

## Types

### R-type

|  |  |  |
| --- | --- | --- |
| Op-code (8) | Rdst(4) | Rsrc(4) |

All instructions except:

IADD, SHL, SHR, LDM

### I-type

|  |  |  |  |
| --- | --- | --- | --- |
| Op-code (8) | Rdst(4) | Rsrc(4) | IMM(16) |

Instructions:

IADD, SHL, SHR, LDM

PUSH and POP would consist of 4 words and take 2 cycles to complete. It will have the two instructions

PUSH:

IADD SP, -2

STD Rdst, 0(SP)

POP:

LDD Rdst, 0(SP)

IADD SP, 2

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NOP |  |  |  | 0 | 0 | 0 | 0 | 0 |
| ADD |  |  |  | 0 | 0 | 0 | 0 | 1 |
| SUB |  |  |  | 0 | 0 | 0 | 1 | 0 |
| AND |  |  |  | 0 | 0 | 0 | 1 | 1 |
| OR |  |  |  | 0 | 0 | 1 | 0 | 0 |
| IADD |  |  |  | 0 | 0 | 1 | 0 | 1 |
| SHL |  |  |  | 0 | 0 | 1 | 1 | 0 |
| SHR |  |  |  | 0 | 0 | 1 | 1 | 1 |
| RLC |  |  |  | 0 | 1 | 0 | 0 | 0 |
| RRC |  |  |  | 0 | 1 | 0 | 0 | 1 |
| MOV |  |  |  | 0 | 1 | 0 | 1 | 0 |
| SETC |  |  |  | 0 | 1 | 0 | 1 | 1 |
| CLRC |  |  |  | 0 | 1 | 1 | 0 | 0 |
| CLR |  |  |  | 0 | 1 | 1 | 0 | 1 |
| NOT |  |  |  | 0 | 1 | 1 | 1 | 0 |
| INC |  |  |  | 0 | 1 | 1 | 1 | 1 |
| DEC |  |  |  | 1 | 0 | 0 | 0 | 0 |
| NEG |  |  |  | 1 | 0 | 0 | 0 | 1 |
| OUT |  |  |  | 1 | 0 | 0 | 1 | 0 |
| IN |  |  |  | 1 | 0 | 0 | 1 | 1 |
| LDM |  |  |  | 1 | 0 | 1 | 0 | 0 |
| LDD |  |  |  | 1 | 0 | 1 | 0 | 1 |
| STD |  |  |  | 1 | 0 | 1 | 1 | 0 |
| JZ |  |  |  | 1 | 0 | 1 | 1 | 1 |
| JN |  |  |  | 1 | 1 | 0 | 0 | 0 |
| JC |  |  |  | 1 | 1 | 0 | 0 | 1 |
| JMP |  |  |  | 1 | 1 | 0 | 1 | 0 |

## Opcode of each instruction

# Control Unit Detailed Design

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inst | | MemWrite | MemRead | ALU | IMM | IO | WBO | RegWrite |
| MOV | | 0 | 0 | 00000 | 0 | 0 | 0 | 1 |
| ADD | | 0 | 0 | 00001 | 0 | 0 | 0 | 1 |
| SUB | | 0 | 0 | 00010 | 0 | 0 | 0 | 1 |
| AND | | 0 | 0 | 00011 | 0 | 0 | 0 | 1 |
| OR | | 0 | 0 | 00100 | 0 | 0 | 0 | 1 |
| IADD | | 0 | 0 | 00001 | 1 | 0 | 0 | 1 |
| SHL | | 0 | 0 | 00101 | 1 | 0 | 0 | 1 |
| SHR | | 0 | 0 | 00110 | 1 | 0 | 0 | 1 |
| RLC | | 0 | 0 | 00111 | 0 | 0 | 0 | 1 |
| RRC | | 0 | 0 | 01000 | 0 | 0 | 0 | 1 |
|  |  | | | | | | | |
| NOP | | 0 | 0 | 00000 | 0 | 0 | 0 | 0 |
| SETC | | 0 | 0 | 01001 | 0 | 0 | 0 | 0 |
| CLRC | | 0 | 0 | 01010 | 0 | 0 | 0 | 0 |
| CLR | | 0 | 0 | 01111 | 0 | 0 | 0 | 1 |
| NOT | | 0 | 0 | 01011 | 0 | 0 | 0 | 1 |
| INC | | 0 | 0 | 01100 | 0 | 0 | 0 | 1 |
| DEC | | 0 | 0 | 01101 | 0 | 0 | 0 | 1 |
| NEG | | 0 | 0 | 01110 | 0 | 0 | 0 | 1 |
| OUT | | 0 | 0 | 00000 | 0 | 1 | 0 | 0 |
| IN | | 0 | 1 | 00000 | 0 | 1 | 1 | 1 |
|  |  | | | | | | | |
| LDM | | 0 | 0 | 00000 | 1 | 0 | 0 | 1 |
| LDD | | 0 | 1 | 00001 | 0 | 0 | 1 | 1 |
| STD | | 1 | 0 | 00001 | 1 | 0 | 0 | 0 |

## ALU Operations

|  |  |
| --- | --- |
| ALU\_Operations | ALU |
| Op1 | 00000 |
| ADD | 00001 |
| SUB | 00010 |
| AND | 00011 |
| OR | 00100 |
| SHL | 00101 |
| SHR | 00110 |
| RLC | 00111 |
| RRC | 01000 |
| SETC | 01001 |
| CLRC | 01010 |
| NOT | 01011 |
| INC | 01100 |
| DEC | 01101 |
| NEG | 01110 |
| CLR | 01111 |
| Op2 | 10000 |

# Pipeline registers design

## IF/ID

* Instruction

## ID/EX

* Control Signals:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| MemWrite | MemRead | ALU | IMM | IO | WBO | RegWrite |

* IMM Value (32 bit)
* Src register (32 bits)
* Dst register (32 bits)
* Rdst (4 bits)

## EX/MEM

* Control signals

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| MemWrite | MemRead | IO | WBO | RegWrite |

* ALU\_OUTPUT (32 bits)
* Dst register (32 bits)
* Rdst (4 bits)

## MEM/WB

* Control signals

|  |  |
| --- | --- |
| WBO | RegWrite |

* MEM/IO\_OUTPUT (32 bits)
* ALU\_OUTPUT (32 bits)
* Rdst (4 bits)

No operand

Opcode + 11111111

Single operand

|  |  |  |
| --- | --- | --- |
| Op code | R | 1111 |

|  |  |  |  |
| --- | --- | --- | --- |
| LDD | Rdst | Rsrc | Offset |
| LDM | Rdst | Rsrc | IMM |
| STD | Rdst | Rsrc | IMM |
| MOV | Rdst | Rsrc | - |
| ADD/SUB/OR/AND | Rdst | Rsrc | - |
| IADD/SHL/SHR | Rdst | Rdst | IMM |
| RLC/RRC | Rdst | Rdst | - |