EDF Scheduler Report:

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1. Tasks Data

Execution time measured using Keil logic analyzer:

- Execution Time Button_1_Monitor = 0.0012 ms
- Execution Time Button_2_Monitor = 0.0012 ms
- Execution Time Periodic_Transmitter = 0.0013 ms
- Execution Time Uart_Receiver = 0.0014 ms
- Execution Time Load_1_Simulation = 5 ms
- Execution Time Load_2_Simulation = 12 ms

- Periodicity Button_1_Monitor = 50 ms
- Periodicity Button_2_Monitor = 50 ms
- Periodicity Periodic_Transmitter = 100 ms
- Periodicity Uart_Receiver = 20 ms
- Periodicity Load_1_Simulation = 10 ms
- Periodicity Load_2_Simulation = 100 ms

- Dead Line Button_1_Monitor = 50 ms
- Dead Line Button_2_Monitor = 50 ms
- Dead Line Periodic_Transmitter = 100 ms
- Dead Line Uart_Receiver = 20 ms
- Dead Line Load_1_Simulation = 10 ms
- Dead Line Load_2_Simulation = 100 ms

2. Hyper Period

- **Hyperperiod** =
  Least common multiplier (50 , 50 , 100 , 20 , 10 , 100) = **100**

3. CPU Load

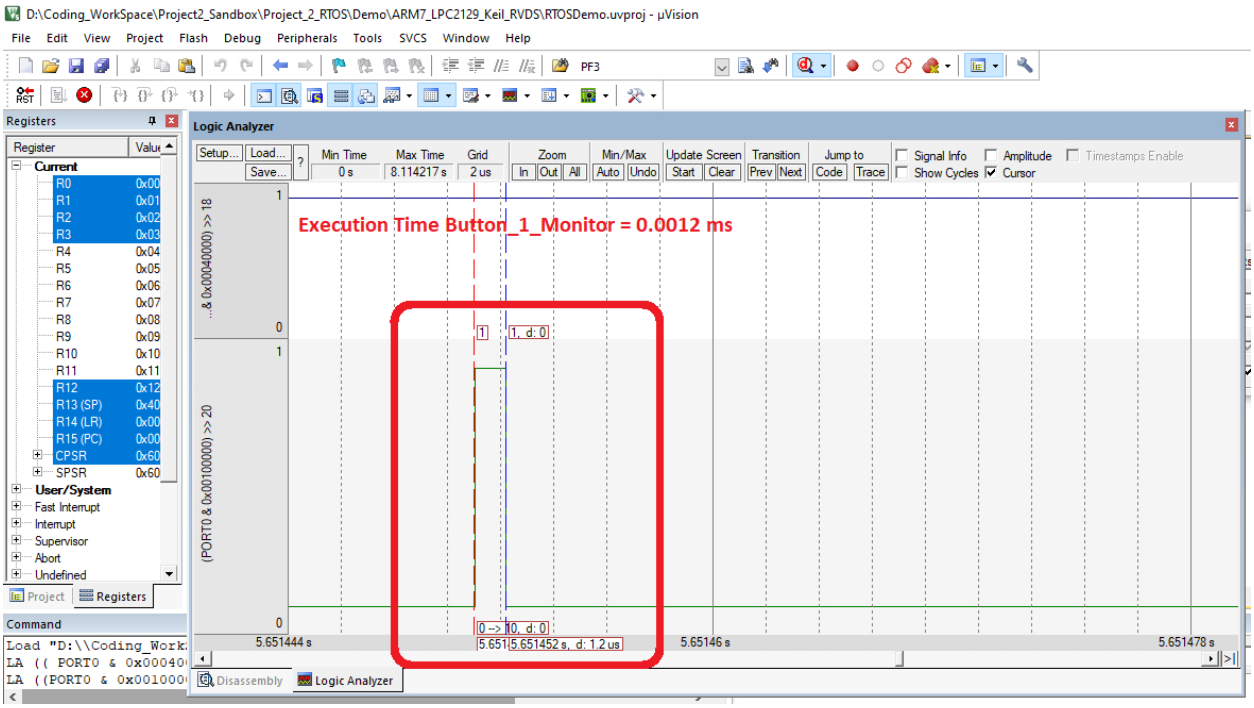
- WCET (worst case execution time) analysis:
  utilization factor of one frame = execution time * frequency =
  execution time / Period

- CPU Load = summation of utilization factor for all tasks

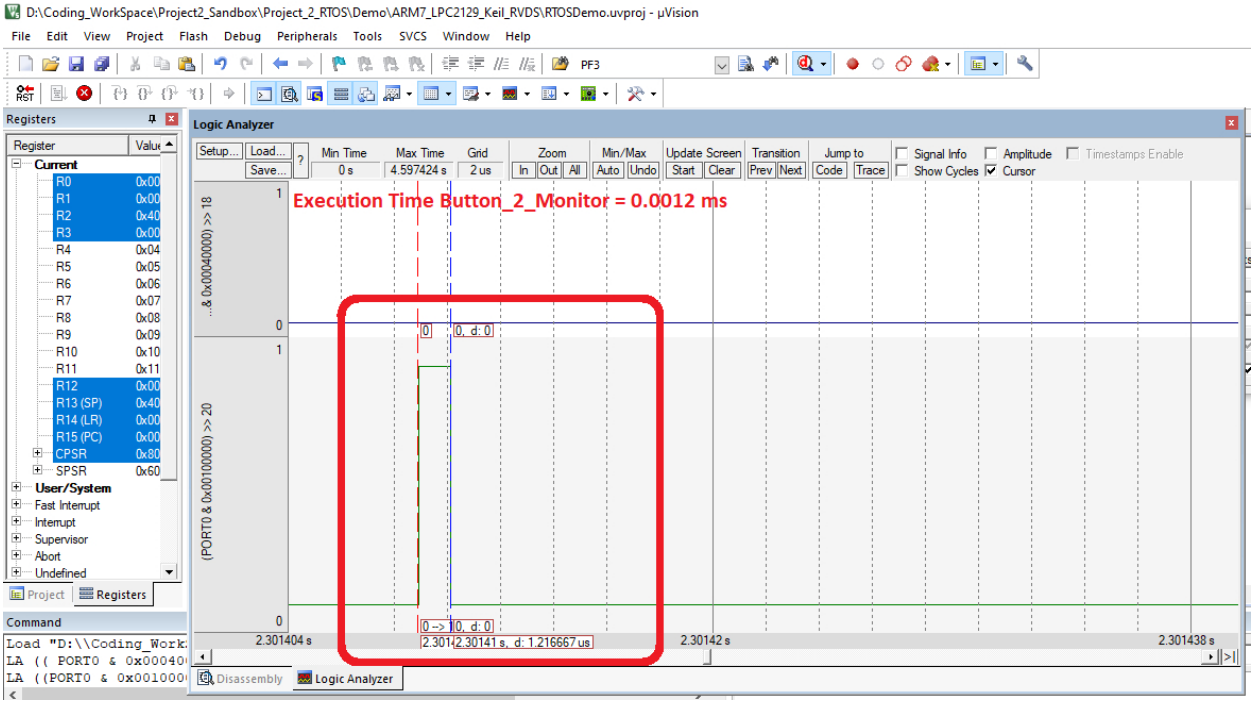
  CPU Load =
  (0.0012 / 50) +
  (0.0012 / 50) +
  (0.00138 / 100) +
  (0.0014 / 20) +
  (5 / 10) +
  (12 / 100) = **0.6201** = **62.01 %**

4. Measurement of Execution Time

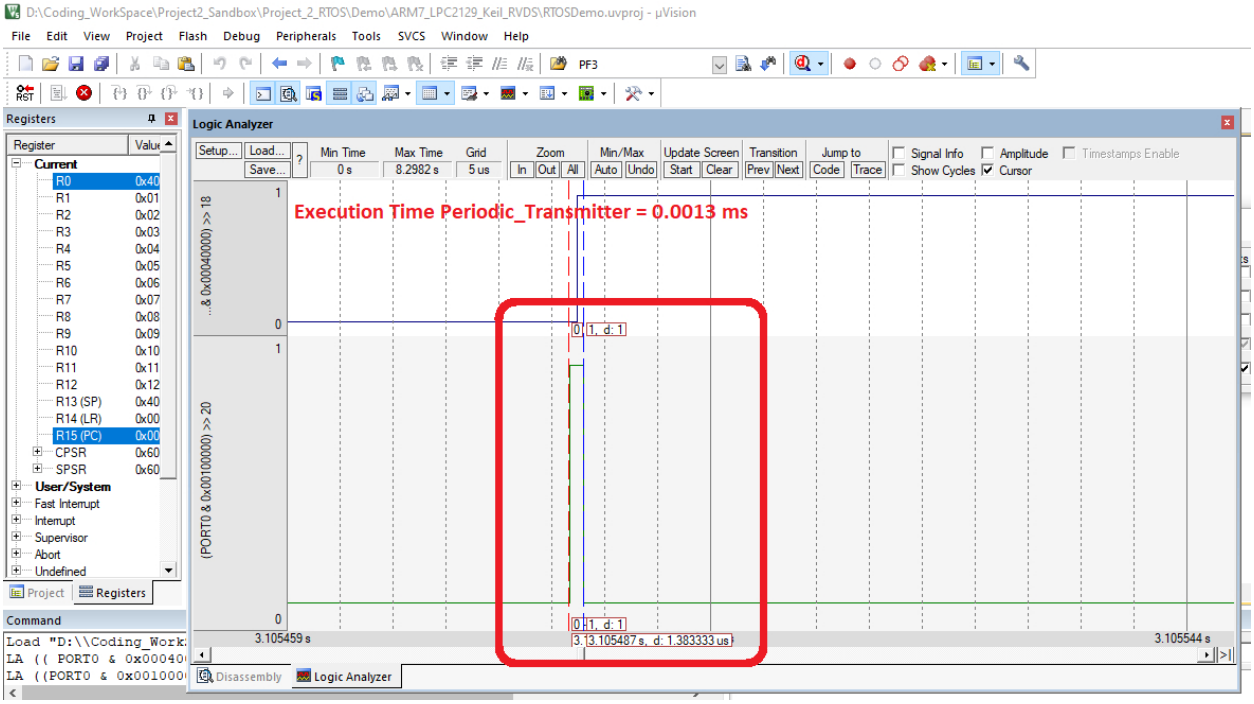
Task 1:



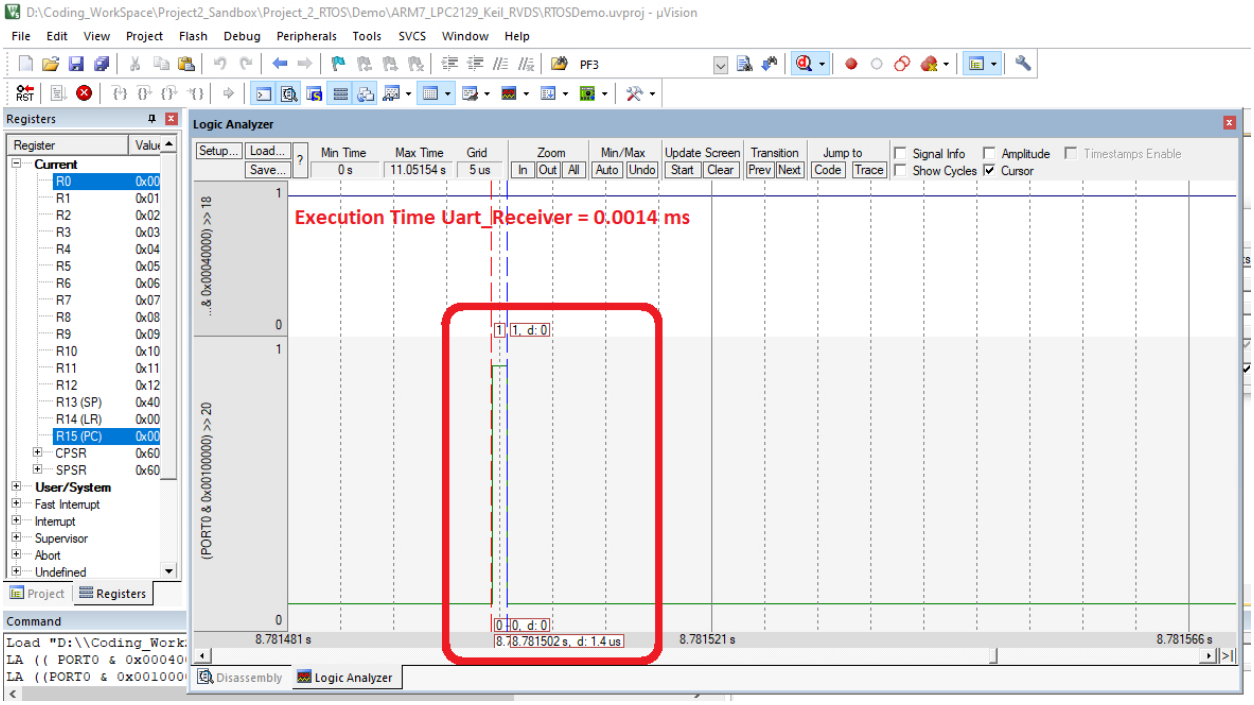
Task 2:



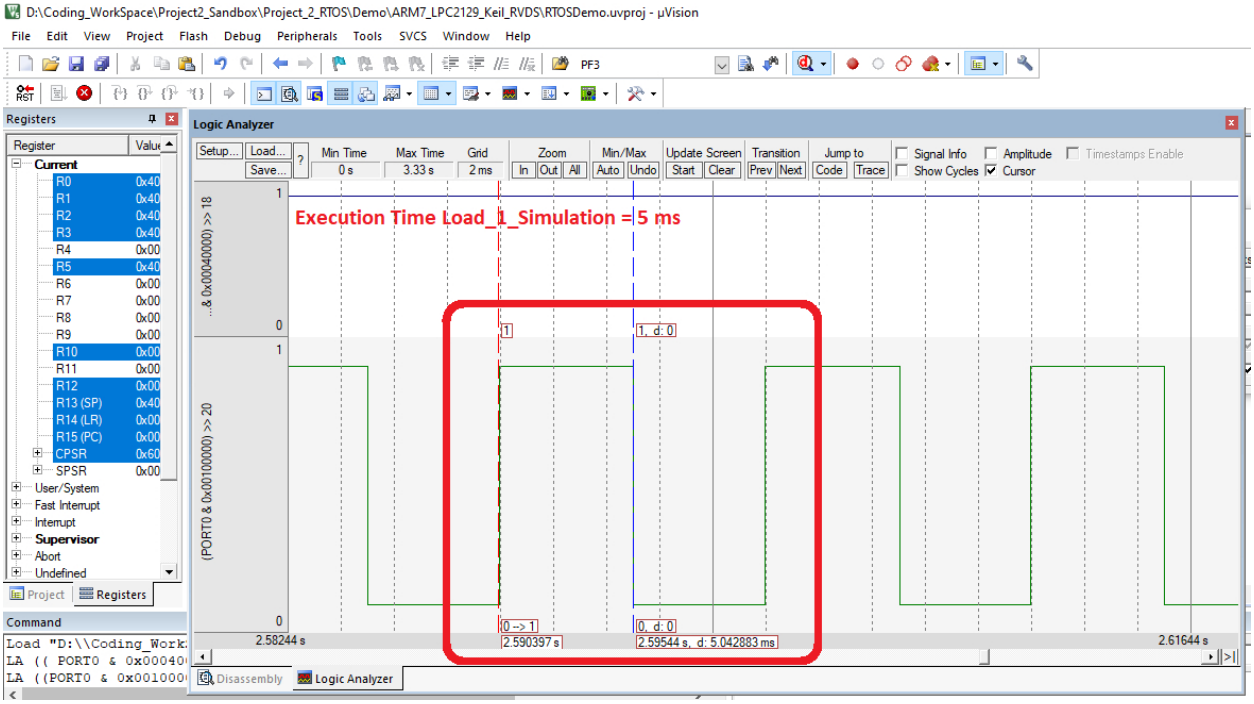
Task 3:


D:\Coding_WorkSpace\Project2_Sandbox\Project_2_RTOS\Demo\ARM7_LPC2129_Keil_RVDS\RTOSDemo.uvproj - µVision
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Logic Analyzer
Execution Time Periodic_Transmitter = 0.0013 ms
Registers
Command
Disassembly
Logic Analyzer

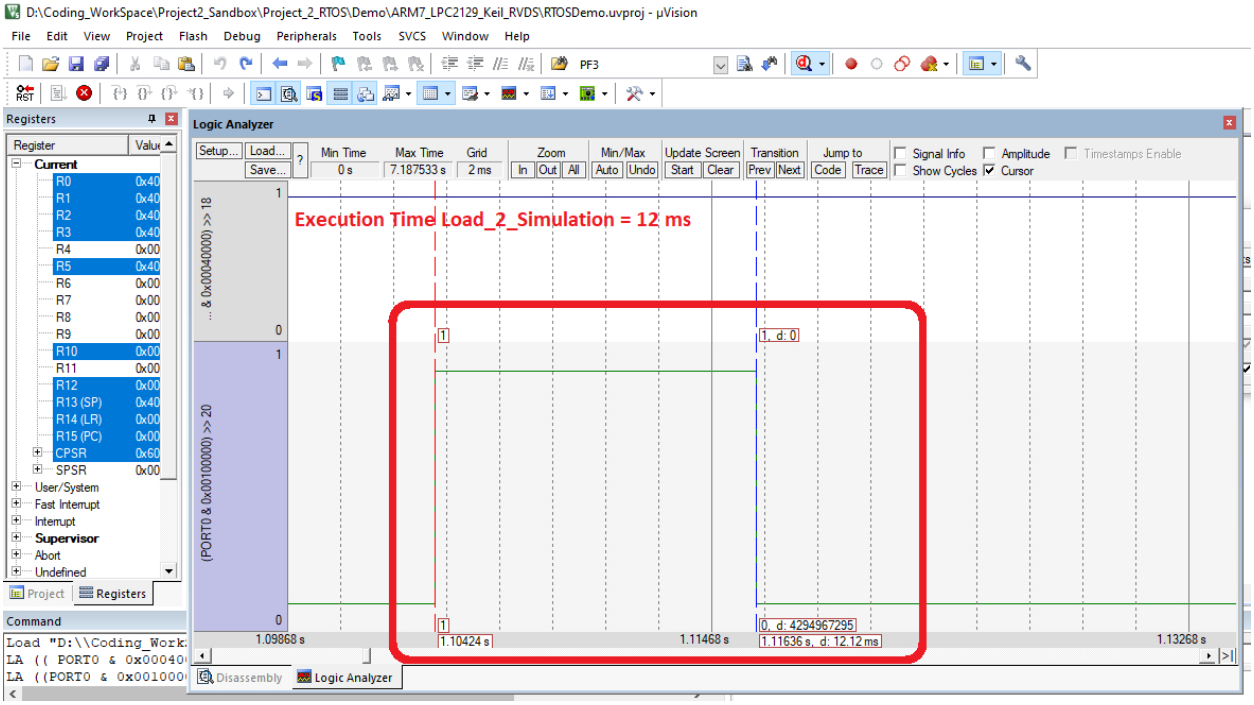
Task 4:


D:\Coding_WorkSpace\Project2_Sandbox\Project_2_RTOS\Demo\ARM7_LPC2129_Keil_RVDS\RTOSDemo.uvproj - µVision
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Logic Analyzer
Execution Time Uart_Receiver = 0.0014 ms
Registers
Command
Disassembly
Logic Analyzer

Task 5:


D:\Coding_WorkSpace\Project2_Sandbox\Project_2_RTOS\Demo\ARM7_LPC2129_Keil_RVDS\RTOSDemo.uvproj - µVision
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Logic Analyzer
Execution Time Load_1_Simulation = 5 ms
Command
Disassembly
Logic Analyzer

Task 6:


D:\Coding_WorkSpace\Project2_Sandbox\Project_2_RTOS\Demo\ARM7_LPC2129_Keil_RVDS\RTOSDemo.uvproj - µVision
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Logic Analyzer
Execution Time Load_2_Simulation = 12 ms
Command
Disassembly
Logic Analyzer

5. Rate Monotonic Utilization

- CPU Load = 0.6201

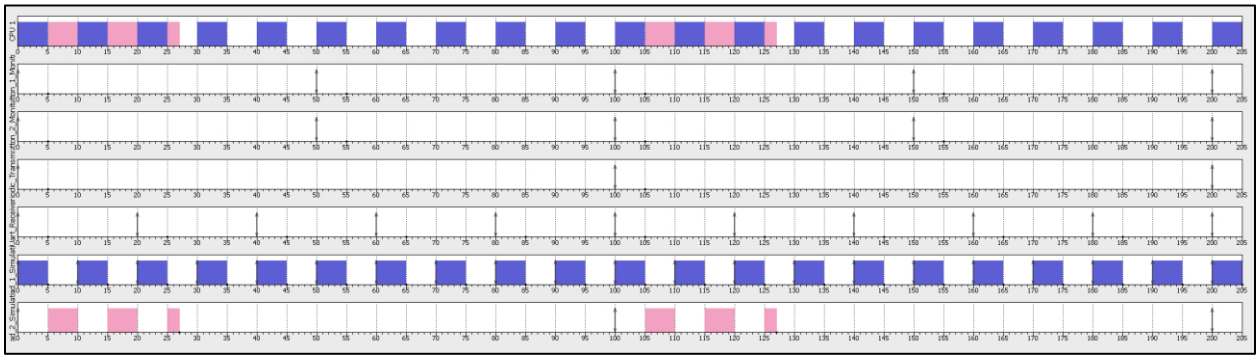
- U = CPU Load < = n * (2 pow(1 / n) - 1)

  n * (2 pow(1 / n) - 1)
  6 * (2 pow(1 / 6) - 1) = **0.7347**

  0.6201 < 0.7347

  Therefore system can be scheduleable.

6. Simso Gantt chart



7. Time Demand Analysis

task 1:
at critical time (t = 100)
time provided (i.e deadline) = 50 ms
time needed to complete execution = 0.0012 ms

time needed < time provided.
Therefore task 1 is scheduleable.
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task 2:
at critical time (t = 100)
time provided (i.e deadline) = 50 ms
time needed to complete execution = 0.0012 ms

time needed < time provided.
Therefore task 2 is scheduleable.
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task 3:
at critical time (t = 100)
time provided (i.e deadline) = 100 ms
time needed to complete execution = 0.0013 ms

time needed < time provided.
Therefore task 3 is scheduleable.
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task 4:
at critical time (t = 100)
time provided (i.e deadline) = 20 ms
time needed to complete execution = 0.0014 ms

time needed < time provided.
Therefore task 4 is scheduleable.

Task 5:
at critical time (t = 100)
time provided (i.e deadline) = 10 ms
time needed to complete execution = 5 ms

time needed < time provided.
Therefore task 5 is scheduleable.

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task 6:
at critical time (t = 100)
time provided (i.e deadline) = 100 ms
time needed to complete execution = 27 ms

time needed < time provided.
Therefore task 6 is scheduleable.