

Synchronous FIFO

Digital Verification Diploma

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Introduction

Reliable data buffering is foundational to the stability and performance of modern digital systems. The Synchronous First-In, First-Out (FIFO) buffer is a ubiquitous component used to safely manage data flow between blocks operating under a unified clock domain.

This project focused exclusively on the Verification of a provided, parameterizable Synchronous FIFO RTL implementation. The primary objective was to ensure the design's functional correctness and robustness to specifications through a rigorous, industry-standard verification methodology.

To achieve this, a SystemVerilog (SV) environment was developed. This environment facilitated the implementation of a Coverage-Driven Verification (CDV) flow, featuring constrained random stimulus generation, a golden reference model (Scoreboard) for checking data integrity, and a comprehensive set of functional and code coverage metrics. The verification effort was successfully executed to achieve a target of 100% functional and code coverage, rigorously testing all data path, control logic, boundary conditions, and error states (e.g., overflow and underflow) of the FIFO design.

RTL

Interface Code Snippets

```
@ FQO.co
1 interface FIFO_if (clk);
2     parameter FIFO_WIDTH = 16;
3     parameter FIFO_DEPTH = 8;
4     input clk;
5     logic [FIFO_WIDTH-1:0] data_in;
6     logic rst_n, wr_en, rd_en;
7     logic [FIFO_WIDTH-1:0] data_out;
8     logic wr_ack, overflow;
9     logic full, empty, almostfull, almostempty, underflow;
10
11 // Monitor subport
12 subport monitor {
13     input clk, rst_n, wr_en, rd_en;
14     input data_in, data_out;
15     input wr_ack, overflow;
16     input full, empty, almostfull, almostempty, underflow;
17 };
18
19 // Test subport
20 subport test {
21     input clk;
22     output rst_n, wr_en, rd_en, data_in;
23     input data_out, wr_ack, overflow;
24     input full, empty, almostfull, almostempty, underflow;
25 };
26
27 // DUT subport
28 subport dut {
29     input clk, rst_n, wr_en, rd_en, data_in;
30     output data_out, wr_ack, overflow;
31     output full, empty, almostfull, almostempty, underflow;
32 };
33
34 endinterface
35
```

RTL Code Snippets

```
@ FIFO.sv
1 // Author: Kareem Waseem
2 // Course: Digital Verification using SV & UVM
3 // Description: FIFO Design
4 //
5 //
6 //
7 //
8 module FIFO(FIFO_if f_if);
9
10 localparam max_fifo_addr = $clog2(f_if.FIFO_DEPTH);
11
12 reg [f_if.FIFO_WIDTH-1:0] mem [f_if.FIFO_DEPTH-1:0];
13
14 reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
15 reg [max_fifo_addr:0] count;
16
17 always @(posedge f_if.clk or negedge f_if.rst_n) begin
18     if (!f_if.rst_n) begin
19         wr_ptr <= 0;
20         f_if.overflow <= 0;
21         f_if.wr_ack <= 0;
22     end
23     else if (f_if.wr_en && count < f_if.FIFO_DEPTH) begin
24         mem[wr_ptr] <= f_if.data_in;
25         f_if.wr_ack <= 1;
26         wr_ptr <= wr_ptr + 1;
27     end
28     else begin
29         f_if.wr_ack <= 0;
30         if (f_if.full & f_if.wr_en)
31             f_if.overflow <= 1;
32         else
33             f_if.overflow <= 0;
34     end
35 end
36
37 always @(posedge f_if.clk or negedge f_if.rst_n) begin
38     if (!f_if.rst_n) begin
39         rd_ptr <= 0;
40         f_if.underflow <= 0;
41     end
42     else if (f_if.rd_en && count != 0) begin
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```

75 `ifdef SIM
76 //Assertions
77 //a
78 //FIFO_1
79 a_resetBehaviour: assert property (@(posedge f_if.clk) if_if.rst_n |> lwr_ptr && lrd_ptr && lcount);
80 a_resetBehaviour_cvr: cover property (@(posedge f_if.clk) if_if.rst_n |> lwr_ptr && lrd_ptr && lcount);
81 //b
82 //FIFO_3//FIFO_4//FIFO_5//FIFO_10//FIFO_11//FIFO_12
83 a_wr_ack: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) f_if.wr_en && if_if.full |> ##1 f_if.wr_ack);
84 a_wr_ack_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) f_if.wr_en && if_if.full |> ##1 f_if.wr_ack);
85 //c
86 //FIFO_5, FIFO_12
87 a_overflow: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) f_if.full && f_if.wr_en |> ##1 f_if.overflow);
88 a_overflow_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) f_if.full && f_if.wr_en |> ##1 f_if.overflow);
89 //d
90 //FIFO_9, FIFO_11
91 a_underflow: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) f_if.empty && f_if.rd_en |> ##1 f_if.underflow);
92 a_underflow_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) f_if.empty && f_if.rd_en |> ##1 f_if.underflow);
93 //e
94 //FIFO_8, FIFO_9
95 a_empty: assert property (@(posedge f_if.clk) lcount |> f_if.empty);
96 a_empty_cvr: cover property (@(posedge f_if.clk) lcount |> f_if.empty);
97 //f
98 //FIFO_4, FIFO_5
99 a_full: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) count == f_if.FIFO_DEPTH |> f_if.full);
100 a_full_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) count == f_if.FIFO_DEPTH |> f_if.full);
101 //g
102 //FIFO_3, FIFO_12
103 a_almostfull: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) count == f_if.FIFO_DEPTH-1 |> f_if.almostfull);
104 a_almostfull_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) count == f_if.FIFO_DEPTH-1 |> f_if.almostfull);
105 //h
106 //FIFO_11, FIFO_12
107 a_almostempty: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) count == 1 |> f_if.almostempty);
108 a_almostempty_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) count == 1 |> f_if.almostempty);
109 //i
110 //read pointer
111 a_rd_ptr_wrap: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) rd_ptr == f_if.FIFO_DEPTH-1 && f_if.rd_en && if_if.empty |> ##1 rd_ptr == 0);
112 a_rd_ptr_wrap_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) rd_ptr == f_if.FIFO_DEPTH-1 && f_if.rd_en && if_if.empty |> ##1 rd_ptr == 0);
113 //write pointer
114 a_wr_ptr_wrap: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) wr_ptr == f_if.FIFO_DEPTH-1 && f_if.wr_en && if_if.full |> ##1 wr_ptr == 0);
115 a_wr_ptr_wrap_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) wr_ptr == f_if.FIFO_DEPTH-1 && f_if.wr_en && if_if.full |> ##1 wr_ptr == 0);
116 //j
117 //k
118 //l
119 //m
120 //n
121 //o
122 //p
123 //q
124 //r
125 //s
126 //t
127 //u
128 //v
129 //w
130 //x
131 //y
132 //z
133 //aa
134 //ab
135 //ac
136 //ad
137 //ae
138 //af
139 //ag
140 //ah
141 //ai
142 //aj
143 //ak
144 //al
145 //am
146 //an
147 //ao
148 //ap
149 //aq
150 //ar
151 //as
152 //at
153 //au
154 //av
155 //aw
156 //ax
157 //ay
158 //az
159 //ba
160 //bb
161 //bc
162 //bd
163 //be
164 //bf
165 //bg
166 //bh
167 //bi
168 //bj
169 //bk
170 //bl
171 //bm
172 //bn
173 //bo
174 //bp
175 //bq
176 //br
177 //bs
178 //bt
179 //bu
180 //bv
181 //bw
182 //bx
183 //by
184 //bz
185 //ca
186 //cb
187 //cc
188 //cd
189 //ce
190 //cf
191 //cg
192 //ch
193 //ci
194 //cj
195 //ck
196 //cl
197 //cm
198 //cn
199 //co
200 //cp
201 //cq
202 //cr
203 //cs
204 //ct
205 //cu
206 //cv
207 //cw
208 //cx
209 //cy
210 //cz
211 //da
212 //db
213 //dc
214 //dd
215 //de
216 //df
217 //dg
218 //dh
219 //di
220 //dj
221 //dk
222 //dl
223 //dm
224 //dn
225 //do
226 //dp
227 //dq
228 //dr
229 //ds
230 //dt
231 //du
232 //dv
233 //dw
234 //dx
235 //dy
236 //dz
237 //ea
238 //eb
239 //ec
240 //ed
241 //ee
242 //ef
243 //eg
244 //eh
245 //ei
246 //ej
247 //ek
248 //el
249 //em
250 //en
251 //eo
252 //ep
253 //eq
254 //er
255 //es
256 //et
257 //eu
258 //ev
259 //ew
260 //ex
261 //ey
262 //ez
263 //fa
264 //fb
265 //fc
266 //fd
267 //fe
268 //ff
269 //fg
270 //fh
271 //fi
272 //fj
273 //fk
274 //fl
275 //fm
276 //fn
277 //fo
278 //fp
279 //fq
280 //fr
281 //fs
282 //ft
283 //fu
284 //fv
285 //fw
286 //fx
287 //fy
288 //fz
289 //ga
290 //gb
291 //gc
292 //gd
293 //ge
294 //gf
295 //gg
296 //gh
297 //gi
298 //gj
299 //gk
300 //gl
301 //gm
302 //gn
303 //go
304 //gp
305 //gq
306 //gr
307 //gs
308 //gt
309 //gu
310 //gv
311 //gw
312 //gx
313 //gy
314 //gz
315 //ha
316 //hb
317 //hc
318 //hd
319 //he
320 //hf
321 //hg
322 //hh
323 //hi
324 //hj
325 //hk
326 //hl
327 //hm
328 //hn
329 //ho
330 //hp
331 //hq
332 //hr
333 //hs
334 //ht
335 //hu
336 //hv
337 //hw
338 //hx
339 //hy
340 //hz
341 //ia
342 //ib
343 //ic
344 //id
345 //ie
346 //if
347 //ig
348 //ih
349 //ii
350 //ij
351 //ik
352 //il
353 //im
354 //in
355 //io
356 //ip
357 //iq
358 //ir
359 //is
360 //it
361 //iu
362 //iv
363 //iw
364 //ix
365 //iy
366 //iz
367 //ja
368 //jb
369 //jc
370 //jd
371 //je
372 //jf
373 //jg
374 //jh
375 //ji
376 //jj
377 //jk
378 //jl
379 //jm
380 //jn
381 //jo
382 //jp
383 //jq
384 //jr
385 //js
386 //jt
387 //ju
388 //jv
389 //jw
390 //jx
391 //jy
392 //jz
393 //ka
394 //kb
395 //kc
396 //kd
397 //ke
398 //kf
399 //kg
400 //kh
401 //ki
402 //kj
403 //kk
404 //kl
405 //km
406 //kn
407 //ko
408 //kp
409 //kq
410 //kr
411 //ks
412 //kt
413 //ku
414 //kv
415 //kw
416 //kx
417 //ky
418 //kz
419 //la
420 //lb
421 //lc
422 //ld
423 //le
424 //lf
425 //lg
426 //lh
427 //li
428 //lj
429 //lk
430 //ll
431 //lm
432 //ln
433 //lo
434 //lp
435 //lq
436 //lr
437 //ls
438 //lt
439 //lu
440 //lv
441 //lw
442 //lx
443 //ly
444 //lz
445 //ma
446 //mb
447 //mc
448 //md
449 //me
450 //mf
451 //mg
452 //mh
453 //mi
454 //mj
455 //mk
456 //ml
457 //mn
458 //mo
459 //mp
460 //mq
461 //mr
462 //ms
463 //mt
464 //mu
465 //mv
466 //mw
467 //mx
468 //my
469 //mz
470 //na
471 //nb
472 //nc
473 //nd
474 //ne
475 //nf
476 //ng
477 //nh
478 //ni
479 //nj
480 //nk
481 //nl
482 //nm
483 //nn
484 //no
485 //np
486 //nq
487 //nr
488 //ns
489 //nt
490 //nu
491 //nv
492 //nw
493 //nx
494 //ny
495 //nz
496 //oa
497 //ob
498 //oc
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508 //om
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510 //oo
511 //op
512 //oq
513 //or
514 //os
515 //ot
516 //ou
517 //ov
518 //ow
519 //ox
520 //oy
521 //oz
522 //pa
523 //pb
524 //pc
525 //pd
526 //pe
527 //pf
528 //pg
529 //ph
530 //pi
531 //pj
532 //pk
533 //pl
534 //pm
535 //pn
536 //po
537 //pp
538 //pq
539 //pr
540 //ps
541 //pt
542 //pu
543 //pv
544 //pw
545 //px
546 //py
547 //pz
548 //qa
549 //qb
550 //qc
551 //qd
552 //qe
553 //qf
554 //qg
555 //qh
556 //qi
557 //qj
558 //qk
559 //ql
560 //qm
561 //qn
562 //qo
563 //qp
564 //qq
565 //qr
566 //qs
567 //qt
568 //qu
569 //qv
570 //qw
571 //qx
572 //qy
573 //qz
574 //ra
575 //rb
576 //rc
577 //rd
578 //re
579 //rf
580 //rg
581 //rh
582 //ri
583 //rj
584 //rk
585 //rl
586 //rm
587 //rn
588 //ro
589 //rp
590 //rq
591 //rr
592 //rs
593 //rt
594 //ru
595 //rv
596 //rw
597 //rx
598 //ry
599 //rz
600 //sa
601 //sb
602 //sc
603 //sd
604 //se
605 //sf
606 //sg
607 //sh
608 //si
609 //sj
610 //sk
611 //sl
612 //sm
613 //sn
614 //so
615 //sp
616 //sq
617 //sr
618 //ss
619 //st
620 //su
621 //sv
622 //sw
623 //sx
624 //sy
625 //sz
626 //ta
627 //tb
628 //tc
629 //td
630 //te
631 //tf
632 //tg
633 //th
634 //ti
635 //tj
636 //tk
637 //tl
638 //tm
639 //tn
640 //to
641 //tp
642 //tq
643 //tr
644 //ts
645 //tt
646 //tu
647 //tv
648 //tw
649 //tx
650 //ty
651 //tz
652 //ua
653 //ub
654 //uc
655 //ud
656 //ue
657 //uf
658 //ug
659 //uh
660 //ui
661 //uj
662 //uk
663 //ul
664 //um
665 //un
666 //uo
667 //up
668 //uq
669 //ur
670 //us
671 //ut
672 //uu
673 //uv
674 //uw
675 //ux
676 //uy
677 //uz
678 //va
679 //vb
680 //vc
681 //vd
682 //ve
683 //vf
684 //vg
685 //vh
686 //vi
687 //vj
688 //vk
689 //vl
690 //vm
691 //vn
692 //vo
693 //vp
694 //vq
695 //vr
696 //vs
697 //vt
698 //vu
699 //vv
700 //vw
701 //vx
702 //vy
703 //vz
704 //wa
705 //wb
706 //wc
707 //wd
708 //we
709 //wf
710 //wg
711 //wh
712 //wi
713 //wj
714 //wk
715 //wl
716 //wm
717 //wn
718 //wo
719 //wp
720 //wq
721 //wr
722 //ws
723 //wt
724 //wu
725 //wv
726 //ww
727 //wx
728 //wy
729 //wz
730 //xa
731 //xb
732 //xc
733 //xd
734 //xe
735 //xf
736 //xg
737 //xh
738 //xi
739 //xj
740 //xk
741 //xl
742 //xm
743 //xn
744 //xo
745 //xp
746 //xq
747 //xr
748 //xs
749 //xt
750 //xu
751 //xv
752 //xw
753 //xx
754 //xy
755 //xz
756 //ya
757 //yb
758 //yc
759 //yd
760 //ye
761 //yf
762 //yg
763 //yh
764 //yi
765 //yj
766 //yk
767 //yl
768 //ym
769 //yn
770 //yo
771 //yp
772 //yq
773 //yr
774 //ys
775 //yt
776 //yu
777 //yv
778 //yw
779 //yx
780 //yz
781 //za
782 //zb
783 //zc
784 //zd
785 //ze
786 //zf
787 //zg
788 //zh
789 //zi
790 //zj
791 //zk
792 //zl
793 //zm
794 //zn
795 //zo
796 //zp
797 //zq
798 //zr
799 //zs
800 //zt
801 //zu
802 //zv
803 //zw
804 //zx
805 //zy
806 //zz

```

```

110 //i
111 //read pointer
112 a_rd_ptr_wrap: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) rd_ptr == f_if.FIFO_DEPTH-1 && f_if.rd_en && if_if.empty |> ##1 rd_ptr == 0);
113 a_rd_ptr_wrap_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) rd_ptr == f_if.FIFO_DEPTH-1 && f_if.rd_en && if_if.empty |> ##1 rd_ptr == 0);
114 //write pointer
115 a_wr_ptr_wrap: assert property (@(posedge f_if.clk) disable iff (if_if.rst_n) wr_ptr == f_if.FIFO_DEPTH-1 && f_if.wr_en && if_if.full |> ##1 wr_ptr == 0);
116 a_wr_ptr_wrap_cvr: cover property (@(posedge f_if.clk) disable iff (if_if.rst_n) wr_ptr == f_if.FIFO_DEPTH-1 && f_if.wr_en && if_if.full |> ##1 wr_ptr == 0);
117 //j
118 //k
119 //l
120 //m
121 //n
122 //o
123 //p
124 //q
125 //r
126 //s
127 //t
128 //u
129 //v
130 //w
131 //x
132 //y
133 //z
134 //aa
135 //ab
136 //ac
137 //ad
138 //ae
139 //af
140 //ag
141 //ah
142 //ai
143 //aj
144 //ak
145 //al
146 //am
147 //an
148 //ao
149 //ap
150 //aq
151 //ar
152 //as
153 //at
154 //au
155 //av
156 //aw
157 //ax
158 //ay
159 //az
160 //ba
161 //bb
162 //bc
163 //bd
164 //be
165 //bf
166 //bg
167 //bh
168 //bi
169 //bj
170 //bk
171 //bl
172 //bm
173 //bn
174 //bo
175 //bp
176 //bq
177 //br
178 //bs
179 //bt
180 //bu
181 //bv
182 //bw
183 //bx
184 //by
185 //bz
186 //ca
187 //cb
188 //cc
189 //cd
190 //ce
191 //cf
192 //cg
193 //ch
194 //ci
195 //cj
196 //ck
197 //cl
198 //cm
199 //cn
200 //co
201 //cp
202 //cq
203 //cr
204 //cs
205 //ct
206 //cu
207 //cv
208 //cw
209 //cx
210 //cy
211 //cz
212 //da
213 //db
214 //dc
215 //dd
216 //de
217 //df
218 //dg
219 //dh
220 //di
221 //dj
222 //dk
223 //dl
224 //dm
225 //dn
226 //do
227 //dp
228 //dq
229 //dr
230 //ds
231 //dt
232 //du
233 //dv
234 //dw
235 //dx
236 //dy
237 //dz
238 //ea
239 //eb
240 //ec
241 //ed
242 //ee
243 //ef
244 //eg
245 //eh
246 //ei
247 //ej
248 //ek
249 //el
250 //em
251 //en
252 //eo
253 //ep
254 //eq
255 //er
256 //es
257 //et
258 //eu
259 //ev
260 //ew
261 //ex
262 //ey
263 //ez
264 //fa
265 //fb
266 //fc
267 //fd
268 //fe
269 //fg
270 //fh
271 //fi
272 //fj
273 //fk
274 //fl
275 //fm
276 //fn
277 //fo
278 //fp
279 //fq
280 //fr
281 //fs
282 //ft
283 //fu
284 //fv
285 //fw
286 //fx
287 //fy
288 //fz
289 //ga
290 //gb
291 //gc
292 //gd
293 //ge
294 //gf
295 //gg
296 //gh
297 //gi
298 //gj
299 //gk
300 //gl
301 //gm
302 //gn
303 //go
304 //gp
305 //gq
306 //gr
307 //gs
308 //gt
309 //gu
310 //gv
311 //gw
312 //gx
313 //gy
314 //gz
315 //ha
316 //hb
317 //hc
318 //hd
319 //he
320 //hf
321 //hg
322 //hh
323 //hi
324 //hj
325 //hk
326 //hl
327 //hm
328 //hn
329 //ho
330 //hp
331 //hq
332 //hr
333 //hs
334 //ht
335 //hu
336 //hv
337 //hw
338 //hx
339 //hy
340 //hz
341 //ia
342 //ib
343 //ic
344 //id
345 //ie
346 //if
347 //ig
348 //ih
349 //ii
350 //ij
351 //ik
352 //il
353 //im
354 //in
355 //io
356 //ip
357 //iq
358 //ir
359 //is
360 //it
361 //iu
362 //iv
363 //iw
364 //ix
365 //iy
366 //iz
367 //ja
368 //jb
369 //jc
370 //jd
371 //je
372 //jf
373 //jg
374 //jh
375 //ji
376 //jj
377 //jk
378 //jl
379 //jm
380 //jn
381 //jo
382 //jp
383 //jq
384 //jr
385 //js
386 //jt
387 //ju
388 //jv
389 //jw
390 //jx
391 //jy
392 //jz
393 //ka
394 //kb
395 //kc
396 //kd
397 //ke
398 //kf
399 //kg
400 //kh
401 //ki
402 //kj
403 //kk
404 //kl
405 //km
406 //kn
407 //ko
408 //kp
409 //kq
410 //kr
411 //ks
412 //kt
413 //ku
414 //kv
415 //kw
416 //kx
417 //ky
418 //kz
419 //la
420 //lb
421 //lc
422 //ld
423 //le
424 //lf
425 //lg
426 //lh
427 //li
428 //lj
429 //lk
430 //ll
431 //lm
432 //ln
433 //lo
434 //lp
435 //lq
436 //lr
437 //ls
438 //lt
439 //lu
440 //lv
441 //lw
442 //lx
443 //ly
444 //lz
445 //ma
446 //mb
447 //mc
448 //md
449 //me
450 //mf
451 //mg
452 //mh
453 //mi
454 //mj
455 //mk
456 //ml
457 //mn
458 //mo
459 //mp
460 //mq
461 //mr
462 //ms
463 //mt
464 //mu
465 //mv
466 //mw
467 //mx
468 //my
469 //mz
470 //na
471 //nb
472 //nc
473 //nd
474 //ne
475 //nf
476 //ng
477 //nh
478 //ni
479 //nj
480 //nk
481 //nl
482 //nm
483 //nn
484 //no
485 //np
486 //nq
487 //nr
488 //ns
489 //nt
490 //nu
491 //nv
492 //nw
493 //nx
494 //ny
495 //nz
496 //oa
497 //ob
498 //oc
499 //od
500 //oe
501 //of
502 //og
503 //oh
504 //oi
505 //oj
506 //ok
507 //ol
508 //om
509 //on
510 //oo
511 //op
512 //oq
513 //or
514 //os
515 //ot
516 //ou
517 //ov
518 //ow
519 //ox
520 //oy
521 //oz
522 //pa
523 //pb
524 //pc
525 //pd
526 //pe
527 //pf
528 //pg
529 //ph
530 //pi
531 //pj
532 //pk
533 //pl
534 //pm
535 //pn
536 //po
537 //pp
538 //pq
539 //pr
540 //ps
541 //pt
542 //pu
543 //pv
544 //pw
545 //px
546 //py
547 //pz
548 //qa
549 //qb
550 //qc
551 //qd
552 //qe
553 //qf
554 //qg
555 //qh
556 //qi
557 //qj
558 //qk
559 //ql
560 //qm
561 //qn
562 //qo
563 //qp
564 //qq
565 //qr
566 //qs
567 //qt
568 //qu
569 //qv
570 //qw
571 //qx
572 //qy
573 //qz
574 //ra
575 //rb
576 //rc
577 //rd
578 //re
579 //rf
580 //rg
581 //rh
582 //ri
583 //rj
584 //rk
585 //rl
586 //rm
587 //rn
588 //ro
589 //rp
590 //rq
591 //rr
592 //rs
593 //rt
594 //ru
595 //rv
596 //rw
597 //rx
598 //ry
599 //rz
600 //sa
601 //sb
602 //sc
603 //sd
604 //se
605 //sf
606 //sg
607 //sh
608 //si
609 //sj
610 //sk
611 //sl
612 //sm
613 //sn
614 //so
615 //sp
616 //sq
617 //sr
618 //ss
619 //st
620 //su
621 //sv
622 //sw
623 //sx
624 //sy
625 //sz
626 //ta
627 //tb
628 //tc
629 //td
630 //te
631 //tf
632 //tg
633 //th
634 //ti
635 //tj
636 //tk
637 //tl
638 //tm
639 //tn
640 //to
641 //tp
642 //tq
643 //tr
644 //ts
645 //tt
646 //tu
647 //tv
648 //tw
649 //tx
650 //ty
651 //tz
652 //ua
653 //ub
654 //uc
655 //ud
656 //ue
657 //uf
658 //ug
659 //uh
660 //ui
661 //uj
662 //uk
663 //ul
664 //um
665 //un
666 //uo
667 //up
668 //uq
669 //ur
670 //us
671 //ut
672 //uu
673 //uv
674 //uw
675 //ux
676 //uy
677 //uz
678 //va
679 //vb
680 //vc
681 //vd
682 //ve
683 //vf
684 //vg
685 //vh
686 //vi
687 //vj
688 //vk
689 //vl
690 //vm
691 //vn
692 //vo
693 //vp
694 //vq
695 //vr
696 //vs
697 //vt
698 //vu
699 //vv
700 //vw
701 //vx
702 //vy
703 //vz
704 //wa
705 //wb
706 //wc
707 //wd
708 //we
709 //wf
710 //wg
711 //wh
712 //wi
713 //wj
714 //wk
715 //wl
716 //wm
717 //wn
718 //wo
719 //wp
720 //wq
721 //wr
722 //ws
723 //wt
724 //wu
725 //wv
726 //ww
727 //wx
728 //wy
729 //wz
730 //xa
731 //xb
732 //xc
733 //xd
734 //xe
735 //xf
736 //xg
737 //xh
738 //xi
739 //xj
740 //xk
741 //xl
742 //xm
743 //xn
744 //xo
745 //xp
746 //xq
747 //xr
748 //xs
749 //xt
750 //xu
751 //xv
752 //xw
753 //xx
754 //xy
755 //xz
756 //ya
757 //yb
758 //yc
759 //yd
760 //ye
761 //yf
762 //yg
763 //yh
764 //yi
765 //yj
766 //yk
767 //yl
768 //ym
769 //yn
770 //yo
771 //yp
772 //yq
773 //yr
774 //ys
775 //yt
776 //yu
777 //yv
778 //yw
779 //yx
780 //yz
781 //za
782 //zb
783 //zc
784 //zd
785 //ze
786 //zf
787 //zg
788 //zh
789 //zi
790 //zj
791 //zk
792 //zl
793 //zm
794 //zn
795 //zo
796 //zp
797 //zq
798 //zr
799 //zs
800 //zt
801 //zu
802 //zv
803 //zw
804 //zx
805 //zy
806 //zz

```

Bug Fixed #1

- The almostfull flag condition was wrong

Before

```

57 assign f_if.full = (count == f_if.FIFO_DEPTH)? 1 : 0;
58 assign f_if.empty = (count == 0)? 1 : 0;
59 assign f_if.underflow = (f_if.empty && f_if.rd_en)? 1 : 0;
60 assign f_if.almostfull = (count == f_if.FIFO_DEPTH-2)? 1 : 0;
61 assign f_if.almostempty = (count == 1)? 1 : 0;

```

After

```

70 assign f_if.full = (count == f_if.FIFO_DEPTH)? 1 : 0;
71 assign f_if.empty = (count == 0)? 1 : 0;
72 assign f_if.almostfull = (count == f_if.FIFO_DEPTH-1)? 1 : 0;
73 assign f_if.almostempty = (count == 1)? 1 : 0;

```

Bug Fixed #2

- Not handling the counter value when the wr_en = 1 and rd_en = 1

Before

```
45 always @(posedge f_if.clk or negedge f_if.rst_n) begin
46     if (!f_if.rst_n) begin
47         count <= 0;
48     end
49     else begin
50         if ((f_if.wr_en, f_if.rd_en) == 2'b10) && !f_if.full)
51             count <= count + 1;
52         else if ((f_if.wr_en, f_if.rd_en) == 2'b01) && !f_if.empty)
53             count <= count - 1;
54     end
55 end
```

After

```
54 always @(posedge f_if.clk or negedge f_if.rst_n) begin
55     if (!f_if.rst_n) begin
56         count <= 0;
57     end
58     else begin
59         if ((f_if.wr_en, f_if.rd_en) == 2'b11) && f_if.full)
60             count <= count - 1;
61         else if ((f_if.wr_en, f_if.rd_en) == 2'b11) && f_if.empty)
62             count <= count + 1;
63         else if ((f_if.wr_en, f_if.rd_en) == 2'b10) && !f_if.full)
64             count <= count + 1;
65         else if ((f_if.wr_en, f_if.rd_en) == 2'b01) && !f_if.empty)
66             count <= count - 1;
67     end
68 end
```

Bug Fixed #3

- The underflow flag logic was wrong, it should be sequential not combinational

Before

```
57 assign f_if.full = (count == f_if.FIFO_DEPTH)? 1 : 0;
58 assign f_if.empty = (count == 0)? 1 : 0;
59 assign f_if.underflow = (f_if.empty && f_if.rd_en)? 1 : 0;
60 assign f_if.almostfull = (count == f_if.FIFO_DEPTH-2)? 1 : 0;
61 assign f_if.almostempty = (count == 1)? 1 : 0;
```

After

```
37 always @(posedge f_if.clk or negedge f_if.rst_n) begin
38     if (!f_if.rst_n) begin
39         rd_ptr <= 0;
40         f_if.underflow <= 0;
41     end
42     else if (f_if.rd_en && count != 0) begin
43         f_if.data_out <= mem[rd_ptr];
44         rd_ptr <= rd_ptr + 1;
45     end
46     else begin
47         if (f_if.empty & f_if.rd_en)
48             f_if.underflow <= 1;
49         else
50             f_if.underflow <= 0;
51     end
52 end
```

Bug Fixed #4

- Not resetting the sequential flags when the reset is asserted

Before

```
17 always @(posedge f_if.clk or negedge f_if.rst_n) begin
18     if (!f_if.rst_n) begin
19         wr_ptr <= 0;
20     end
```

```
35 always @(posedge f_if.clk or negedge f_if.rst_n) begin
36     if (!f_if.rst_n) begin
37         rd_ptr <= 0;
38     end
```

After

```
17 always @(posedge f_if.clk or negedge f_if.rst_n) begin
18     if (!f_if.rst_n) begin
19         wr_ptr <= 0;
20         f_if.overflow <= 0;
21         f_if.wr_ack <= 0;
22     end
```

```
37 always @(posedge f_if.clk or negedge f_if.rst_n) begin
38     if (!f_if.rst_n) begin
39         rd_ptr <= 0;
40         f_if.underflow <= 0;
41     end
```

Verification Plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check			
FIFO_1	When the reset is asserted, the output flags (full, almostfull, almostempty, overflow, underflow, wr_ack) values should be low and the fifo should be empty	Directed at the start of the simulation then randomized with constraints to be off most of the time	Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The Flags are checked using both golden model and assertions			
FIFO_2	when the wr_en is asserted and the fifo size is less than FIFO_DEPTH, the write operation should take place and store the value of the data_in into the fifo and the wr_ack flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The Flags are checked using both golden model and assertions			
FIFO_3	when the wr_en is asserted and the fifo size equals FIFO_DEPTH-2, then the write operation should take place and the almostfull flag should be high and the wr_ack flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The almostfull and wr_ack flags are checked using both golden model and assertions			
FIFO_4	when the wr_en is asserted and the fifo size equals FIFO_DEPTH-1, then the write operation should take place and the full flag should be high and the wr_ack flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The full flag and wr_ack flags are checked using both golden model and assertions			
	when the wr_en is asserted and the fifo size equals FIFO_DEPTH, then the write operation should take place and the overflow flag should be high and the wr_ack flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The full, overflow and wr_ack flags are checked using both golden model and assertions			

FIFO_5	when the wr_en is asserted and the fifo size equals FIFO_DEPTH, then the write operation should not take place and the full flag should be high and the overflow flag should be high and the wr_ack flag should be low	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The full, overflow and wr_ack flags are checked using both golden model and assertions			
FIFO_6	when the rd_en is asserted and the fifo size is greater than 0, the read operation should take place and the data_out value should equal the fifo values with order of first in first out	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	Data_out value is checked using golden model only			
FIFO_7	when the rd_en is asserted and the fifo size equal to 2, then the read operation should take place and the almost empty flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The almostempty flag is checked using both golden model and assertions, Data_out value is checked using golden model only			
FIFO_8	when the rd_en is asserted and the fifo size equal to 1, then the read operation should take place and the empty flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The empty flag is checked using both golden model and assertions, Data_out value is checked using golden model only			
	when the rd_en is asserted and the fifo size equals 0, then the read operation should not take place and the underflow flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The empty and underflow flags are checked using both golden model and assertions			

	A	B	C	D	E	F	G	H
8				and rd_en				
9	FIFO_8	when the rd_en is asserted and the fifo size equal to 1, then the read operation should take place and the empty flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The empty flag is checked using both golden model and assertions, Data_out value is checked using golden model only			
10	FIFO_9	when the rd_en is asserted and the fifo size equal to 0, then the read operation should not take place, the underflow flag should be high and the empty flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The empty and underflow flags are checked using both golden model and assertions, Data_out value are checked using golden model only			
11	FIFO_10	when the rd_en and wr_en are asserted and the fifo size is less than FIFO_DEPTH and greater than 0, then the read and write operation should take place, the wr_ack flag should be high, store the value of the data_in into the fifo and the data_out value should equal the fifo values with order of first in first out, the fifo size should not change	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The wr_ack flag is checked using both golden model and assertions, Data_out value are checked using golden model only			
12	FIFO_11	when the rd_en and wr_en are asserted and the fifo size is equal to zero, the write operation only should take place and the wr_ack flag should be high, the almost empty flag should be high, and the underflow flag should be high	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The almostempty, underflow flags and wr_ack are checked using both golden model and assertions, Data_out value are checked using golden model only			

13	FIFO_12	when the rd_en and wr_en are asserted and the fifo size is equal to FIFO_DEPTH, then the read operation only should take place, the almostfull flag should be high, the wr_ack should be low, the overflow flag should be high and the data_out value should equal the fifo values with order of first in first out	Randomization with constraints only on wr_en to be active 70% of the time and rd_en to be off 70% of the times	Coverage on the values of wr_en and rd_en Coverage on the values of the fifo flags and cross coverage between them and the wr_en and rd_en	The almostfull, overflow and wr_ack flags are checked using both golden model and assertions, Data_out value are checked using golden model only			
14								
15								
16								

Testbench

Shared Package Code Snippets

```

shared_pkg.v
1 package shared_pkg;
2   logic test_finished;
3   int error_cnt, correct_cnt;
4   event emonitor;
5 endpackage
6

```

Top Code Snippets

```

FIFO_top.v
1 module top;
2   bit clk = 0;
3
4   initial forever #1 clk = ~clk;
5
6   FIFO_if f_if (clk);
7
8   FIFO_DUT (f_if);
9
10  FIFO_tb TB (f_if);
11
12  FIFO_monitor MONITOR (f_if);
13
14  //FIFO_1
15  always_comb begin
16    if (f_if.rst_n) begin
17      a_reset_1: assert final (f_if.empty && !f_if.full);
18      a_reset_2: assert final (f_if.almostempty && !f_if.almostfull);
19      a_reset_3: assert final (f_if.overflow && !f_if.underflow);
20    end
21  end
22
23 endmodule

```

Monitor Code Snippets

Scoreboard

```
1 package FIFO_scoreboard_pkg;
2 import FIFO_transaction_pkg::*;
3 import shared_pkg::*;
4
5 class FIFO_scoreboard;
6     logic [FIFO_WIDTH-1:0] data_out_ref;
7     logic wr_ack_ref, overFlow_ref;
8     logic full_ref, empty_ref, almostfull_ref, underflow_ref;
9
10    logic [FIFO_WIDTH-1:0] FIFO_refmodel [0];
11
12    function void check_data(FIFO_transaction F_txn);
13        reference_model(F_txn);
14
15        if (
16            (F_txn.data_out != data_out_ref) ||
17            (F_txn.wr_ack != wr_ack_ref) ||
18            (F_txn.overflow != overFlow_ref) ||
19            (F_txn.underflow != underflow_ref) ||
20            (F_txn.full != full_ref) ||
21            (F_txn.almostfull != almostfull_ref) ||
22            (F_txn.empty != empty_ref) ||
23            (F_txn.almostempty != almostempty_ref)
24        ) begin
25            error_cnt++;
26            $display("*****");
27            $display("ERROR - OUT Out not equal Ref Model Out");
28            $display("Input Signals:");
29            $display("rst_n:%b", F_txn.rst_n);
30            $display("wr_en:%b - rd_en:%b", F_txn.wr_en, F_txn.rd_en);
31            $display("data_in:%d", F_txn.data_in);
32            $display("-----");
33            $display("OUT Outputs:");
34            $display("data_out:%b", F_txn.data_out);
35            $display("full=%b, almostfull= %b", F_txn.full, F_txn.almostfull);
36            $display("empty=%b, almostempty= %b", F_txn.empty, F_txn.almostempty);
37            $display("overflow=%b, underflow= %b", F_txn.overflow, F_txn.underflow);
38            $display("wr_ack_ref=%b", F_txn.wr_ack);
39            $display("-----");
40            $display("Ref Model Outputs:");
41            $display("data_out:%d", data_out_ref);
42            $display("full=%b, almostfull= %b", full_ref, almostfull_ref);
```

```
3 import shared_pkg::*;
5 class FIFO_scoreboard;
12 function void check_data(FIFO_transaction F_txn);
24 ) begin
42     $display("full=%b, almostfull= %b", full_ref, almostfull_ref);
43     $display("empty=%b, almostempty= %b", empty_ref, almostempty_ref);
44     $display("overflow=%b, underflow= %b", overFlow_ref, underflow_ref);
45     $display("wr_ack_ref=%b", wr_ack_ref);
46     $display("*****");
47 end
48 else begin
49     correct_cnt++;
50     $display("*****");
51     $display("PASS");
52     $display("Input Signals:");
53     $display("rst_n:%b", F_txn.rst_n);
54     $display("wr_en:%b - rd_en:%b", F_txn.wr_en, F_txn.rd_en);
55     $display("data_in:%d", F_txn.data_in);
56     $display("-----");
57     $display("OUT Outputs:");
58     $display("data_out:%b", F_txn.data_out);
59     $display("full=%b, almostfull= %b", F_txn.full, F_txn.almostfull);
60     $display("empty=%b, almostempty= %b", F_txn.empty, F_txn.almostempty);
61     $display("overflow=%b, underflow= %b", F_txn.overflow, F_txn.underflow);
62     $display("wr_ack_ref=%b", F_txn.wr_ack);
63     $display("-----");
64     $display("Ref Model Outputs:");
65     $display("data_out:%d", data_out_ref);
66     $display("full=%b, almostfull= %b", full_ref, almostfull_ref);
67     $display("empty=%b, almostempty= %b", empty_ref, almostempty_ref);
68     $display("overflow=%b, underflow= %b", overFlow_ref, underflow_ref);
69     $display("wr_ack_ref=%b", wr_ack_ref);
70     $display("*****");
71 end
72 endfunction
73 //FIFO_1//FIFO_2//FIFO_3//FIFO_4//FIFO_5//FIFO_6//FIFO_7//FIFO_8//FIFO_9//FIFO_10//FIFO_11//FIFO_12
74 function void reference_model (FIFO_transaction F_txn);
75     if (F_txn.rst_n) begin
76         empty_ref = 1;
77         full_ref = 0;
78         underflow_ref = 0;
79         overflow_ref = 0;
```



```

FIFO_coreboard.v
3 import shared_pkg::*;
5 class FIFO_coreboard;
72 endFunction
73 //FIFO_1//FIFO_2//FIFO_3//FIFO_4//FIFO_5//FIFO_6//FIFO_7//FIFO_8//FIFO_9//FIFO_10//FIFO_11//FIFO_12
74 function void reference_model (FIFO_transaction F_txn);
75     if (!F_txn.rst_n) begin
76         empty_ref = 1;
77         full_ref = 0;
78         underflow_ref = 0;
79         overflow_ref = 0;
80         almostempty_ref = 0;
81         almostfull_ref = 0;
82         wr_ack_ref = 0;
83         FIFO_refmodel.delete();
84     end
85     else begin
86
87         wr_ack_ref = (F_txn.wr_en && FIFO_refmodel.size() < FIFO_DEPTH) ? 1 : 0;
88
89         //Write
90         if (F_txn.wr_en && !full_ref) begin
91             FIFO_refmodel.push_back(F_txn.data_in);
92         end
93         else begin
94             overflow_ref = (F_txn.wr_en && full_ref) ? 1 : 0;
95         end
96         //Read
97         if (F_txn.rd_en && !empty_ref) begin
98             data_out_ref = FIFO_refmodel.pop_front();
99         end
100        else begin
101            underflow_ref = (F_txn.rd_en && empty_ref) ? 1 : 0;
102        end
103
104        full_ref = (FIFO_refmodel.size() == FIFO_DEPTH) ? 1 : 0;
105        empty_ref = (FIFO_refmodel.size() == 0) ? 1 : 0;
106        almostfull_ref = (FIFO_refmodel.size() == FIFO_DEPTH-1) ? 1 : 0;
107        almostempty_ref = (FIFO_refmodel.size() == 1) ? 1 : 0;
108    end
109 endFunction
110 endclass

```

Coverage

```

FIFO_coverage.v
1 package FIFO_coverage_pkg;
2 import FIFO_transaction_pkg::*;
3 class FIFO_coverage;
4     FIFO_transaction F_cvg_txn;
5     covergroup FIFO_cvr;
6
7         //FIFO_2//FIFO_3//FIFO_4//FIFO_5//FIFO_6//FIFO_7//FIFO_8//FIFO_9//FIFO_10//FIFO_11//FIFO_12
8         write_en: coverpoint F_cvg_txn.wr_en;
9         read_en: coverpoint F_cvg_txn.rd_en;
10        full: coverpoint F_cvg_txn.full;
11        almostfull: coverpoint F_cvg_txn.almostfull;
12        empty: coverpoint F_cvg_txn.empty;
13        almostempty: coverpoint F_cvg_txn.almostempty;
14        overflow: coverpoint F_cvg_txn.overflow;
15        underflow: coverpoint F_cvg_txn.underflow;
16        write_ack: coverpoint F_cvg_txn.wr_ack;
17
18        cross_full: cross write_en, read_en, full{
19            ignore_bins full1 = binsof (write_en) intersect {1} && binsof (read_en) intersect {1} && binsof (full) intersect {1};
20            ignore_bins full2 = binsof (write_en) intersect {0} && binsof (read_en) intersect {1} && binsof (full) intersect {1};
21        }
22        cross_almostfull: cross write_en, read_en, almostfull;
23        cross_empty: cross write_en, read_en, empty;
24        cross_almostempty: cross write_en, read_en, almostempty;
25        cross_overflow: cross write_en, read_en, overflow{
26            ignore_bins overflow1 = binsof (write_en) intersect {0} && binsof (read_en) intersect {1} && binsof (overflow) intersect {1};
27            ignore_bins overflow2 = binsof (write_en) intersect {0} && binsof (read_en) intersect {0} && binsof (overflow) intersect {1};
28        }
29        cross_underflow: cross write_en, read_en, underflow{
30            ignore_bins underflow1 = binsof (write_en) intersect {1} && binsof (read_en) intersect {0} && binsof (underflow) intersect {1};
31            ignore_bins underflow2 = binsof (write_en) intersect {0} && binsof (read_en) intersect {0} && binsof (underflow) intersect {1};
32        }
33        cross_write_ack: cross write_en, read_en, write_ack{
34            ignore_bins wr_ack1 = binsof (write_en) intersect {0} && binsof (read_en) intersect {1} && binsof (write_ack) intersect {1};
35            ignore_bins wr_ack2 = binsof (write_en) intersect {0} && binsof (read_en) intersect {0} && binsof (write_ack) intersect {1};
36        }
37    endgroup
38
39    function new();
40        FIFO_cvr = new;
41    endFunction

```

```

40 function new();
41     FIFO_cvr = new;
42 endfunction
43
44 function void sample_data(FIFO_transaction F_txn);
45     this.F_cvg_txn = F_txn;
46     FIFO_cvr.sample();
47 endfunction
48 endclass
49 endpackage

```

Monitor

```
FIFO_monitor.vv
1  import FIFO_transaction_pkg::*;
2  import shared_pkg::*;
3  module FIFO_monitor (FIFO_if fifo_if);
4
5      FIFO_transaction F_txn;
6      FIFO_scoreboard F_scrbrd;
7      FIFO_coverage F_cvg;
8
9      initial begin
10         F_txn = new;
11         F_scrbrd = new;
12         F_cvg = new;
13         forever begin
14             wait (emonitor.triggered);
15             @(negedge fifo_if.clk);
16             F_txn.rst_n = fifo_if.rst_n;
17             F_txn.wr_en = fifo_if.wr_en;
18             F_txn.rd_en = fifo_if.rd_en;
19             F_txn.data_in = fifo_if.data_in;
20             F_txn.data_out = fifo_if.data_out;
21             F_txn.full = fifo_if.full;
22             F_txn.almostfull = fifo_if.almostfull;
23             F_txn.empty = fifo_if.empty;
24             F_txn.almostempty = fifo_if.almostempty;
25             F_txn.overflow = fifo_if.overflow;
26             F_txn.underflow = fifo_if.underflow;
27             F_txn.wr_ack = fifo_if.wr_ack;
28             fork
29                 begin
30                     F_cvg.sample_data(F_txn);
31                 end
32                 begin
33                     F_scrbrd.check_data(F_txn);
34                 end
35             join
36             if (test_finished) begin
37                 $display("Correct Tests = %d, Error Tests = %d", correct_cnt, error_cnt);
38                 $stop;
39             end
40         end
41     end
42 endmodule
```

Testbench Code Snippets

```
FIFO_tb.vv
1  import shared_pkg::*;
2  import FIFO_transaction_pkg::*;
3  module FIFO_tb (FIFO_if f_if);
4
5      logic [FIFO_WIDTH-1:0] FIFO_refmodel [$];
6      logic [FIFO_WIDTH-1:0] data_out_ref;
7      logic wr_ack_ref, overflow_ref;
8      logic full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref;
9      FIFO_transaction F_txn;
10
11      int error_cnt_tb = 0, correct_cnt_tb = 0;
12
13      initial begin
14         F_txn = new;
15         correct_cnt = 0;
16         error_cnt = 0;
17         test_finished = 0;
18         //FIFO_1
19         f_if.rst_n = 0;
20         f_if.wr_en = 0;
21         f_if.rd_en = 0;
22         f_if.data_in = 0;
23         ->emonitor;
24         repeat(4)@(negedge f_if.clk);
25         check_data();
26         //FIFO_2//FIFO_3//FIFO_4//FIFO_5//FIFO_6//FIFO_7//FIFO_8//FIFO_9//FIFO_10//FIFO_11//FIFO_14
27         repeat(3000) begin
28             assert(F_txn.randomize());
29             f_if.rst_n = F_txn.rst_n;
30             f_if.wr_en = F_txn.wr_en;
31             f_if.rd_en = F_txn.rd_en;
32             f_if.data_in = F_txn.data_in;
33             ->emonitor;
34             @(negedge f_if.clk);
35             check_data();
36         end
37         test_finished = 1;
38         ->emonitor;
39         $display("Correct Test @TB = %d, Error Test @TB = %d", correct_cnt_tb, error_cnt_tb);
40     end
41 end
```

```

FIFO_tb.v
3 module FIFO_tb (FIFO_if f_if);
42
43     task check_data;
44         ref_model();
45         if (data_out_ref != f_if.data_out) begin
46             error_cnt_tb++;
47             $display("Error - DUT out: %h != Ref Model out: %h", f_if.data_out, data_out_ref);
48         end
49         else begin
50             correct_cnt_tb++;
51         end
52     endtask
53
54     task ref_model;
55         if (f_if.rst_n) begin
56             empty_ref = 1;
57             full_ref = 0;
58             underflow_ref = 0;
59             overflow_ref = 0;
60             almostempty_ref = 0;
61             almostfull_ref = 0;
62             wr_ack_ref = 0;
63             FIFO_refmodel.delete();
64         end
65         else begin
66
67             wr_ack_ref = (f_if.wr_en && FIFO_refmodel.size() < FIFO_DEPTH) ? 1 : 0;
68
69             //Write
70             if (f_if.wr_en && !full_ref) begin
71                 FIFO_refmodel.push_back(f_if.data_in);
72             end
73             else begin
74                 overflow_ref = (f_if.wr_en && full_ref) ? 1 : 0;
75             end
76
77             //Read
78             if (f_if.rd_en && !empty_ref) begin
79                 data_out_ref = FIFO_refmodel.pop_front();
80             end
81             else begin
82                 underflow_ref = (f_if.rd_en && empty_ref) ? 1 : 0;
83             end
84         end
85     endtask
86 endmodule

```

```

81         underflow_ref = (f_if.rd_en && empty_ref) ? 1 : 0;
82     end
83
84     full_ref = (FIFO_refmodel.size() == FIFO_DEPTH) ? 1 : 0;
85     empty_ref = (FIFO_refmodel.size() == 0) ? 1 : 0;
86     almostfull_ref = (FIFO_refmodel.size() == FIFO_DEPTH-1) ? 1 : 0;
87     almostempty_ref = (FIFO_refmodel.size() == 1) ? 1 : 0;
88 end
89 endtask
90
91 endmodule
92
93

```

DO

```

run.do
1 # 1. Setup and Compile with coverage enabled
2 vlib work
3 vlog -f src_files.list +cover -covercells +define+SIM
4
5 # 2. Start simulation
6 vsim -voptargs+=acc work.top -classdebug -cover
7
8 # 3. Add waves for debugging
9 add wave /top/f_if/*
10 add wave -position insertpoint \
11     sim:/top/DUT/nem \
12     sim:/top/DUT/wr_ptr \
13     sim:/top/DUT/rd_ptr \
14     sim:/top/DUT/count
15 add wave -position insertpoint \
16     sim:/top/MONITOR/F_txn
17 add wave -position end sim:/top/MONITOR/F_scrbrd
18 add wave -position end sim:/top/MONITOR/F_cvg
19 add wave -position insertpoint \
20     sim:/shared_pkg:error_cnt \
21     sim:/shared_pkg:correct_cnt
22
23 # Add Assertion Waves for debugging
24 add wave /top/a_reset_1 /top/a_reset_2 /top/a_reset_3 /top/DUT/a_resetBehaviour /top/DUT/a_wr_ack /top/DUT/a_overflow /top/DUT/a_underflow /top/DUT/a_empty /top/DUT/a_full /top/DUT/
25
26 # 4. Run the simulation to completion
27 run -all
28
29 # 5. Save the collected coverage data to a file
30 coverage save FIFO.ucdb -onexit
31
32 coverage exclude -cvgpath {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_full/<auto[1],auto[1],auto[1]>} {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_full/<auto[0],auto[1],aut
33 coverage exclude -cvgpath {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_overflow/<auto[0],auto[1],auto[1]>} {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_overflow/<auto[0],aut
34 coverage exclude -cvgpath {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_underflow/<auto[1],auto[0],auto[1]>} {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_underflow/<auto[0],a
35 coverage exclude -cvgpath {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_write_ack/<auto[0],auto[1],auto[1]>} {/FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr/cross_write_ack/<auto[0],a
36

```

Coverage

Code Coverage

Branch

FIFO_cvr.txt - Notepad				
File Edit Format View Help				
FIFO.sv(114) 0 1				
/top/DUT/a_count_thr FIFO.sv(115) 0 1				
Branch Coverage:				
Enabled Coverage	Bins	Hits	Misses	Coverage
-----	----	----	-----	-----
Branches	27	27	0	100.00%
=====Branch Details=====				
Branch Coverage for instance /top/DUT				
Line	Item	Count	Source	
-----	----	----	-----	
File FIFO.sv				
-----IF Branch-----				
18		3270	Count coming in to IF	
18	1	554	if (!f_if.rst_n) begin	
23	1	1701	else if (f_if.wr_en && count < f_if.FIFO_DEPTH) begin	
28	1	1015	else begin	
Branch totals: 3 hits of 3 branches = 100.00%				
-----IF Branch-----				
30		1015	Count coming in to IF	
30	1	240	if (f_if.full & f_if.wr_en)	
32	1	775	else	
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
38		3270	Count coming in to IF	
38	1	554	if (!f_if.rst_n) begin	
42	1	684	else if (f_if.rd_en && count != 0) begin	
46	1	2032	else begin	
Branch totals: 3 hits of 3 branches = 100.00%				
-----IF Branch-----				
47		2032	Count coming in to IF	
47	1	112	if (f_if.empty & f_if.rd_en)	
49	1	1920	else	
Branch totals: 2 hits of 2 branches = 100.00%				
Ln 1, Col 1 50% Windows (CRLF) UTF-8				

FIFO_cvr.txt - Notepad				
File Edit Format View Help				
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
55		3005	Count coming in to IF	
55	1	547	if (!f_if.rst_n) begin	
58	1	2458	else begin	
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
59		2458	Count coming in to IF	
59	1	76	if ((f_if.wr_en, f_if.rd_en) == 2'b11) && f_if.full)	
61	1	83	else if ((f_if.wr_en, f_if.rd_en) == 2'b11) && f_if.empty)	
63	1	1212	else if ((f_if.wr_en, f_if.rd_en) == 2'b10) && !f_if.full)	
65	1	202	else if ((f_if.wr_en, f_if.rd_en) == 2'b01) && !f_if.empty)	
885 All False Count				
Branch totals: 5 hits of 5 branches = 100.00%				
-----IF Branch-----				
70		1817	Count coming in to IF	
70	1	138	assign f_if.full = (count == f_if.FIFO_DEPTH)? 1 : 0; //first mistake	
70	2	1679	assign f_if.full = (count == f_if.FIFO_DEPTH)? 1 : 0; //first mistake	
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
71		1817	Count coming in to IF	
71	1	283	assign f_if.empty = (count == 0)? 1 : 0;	
71	2	1534	assign f_if.empty = (count == 0)? 1 : 0;	
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
72		1817	Count coming in to IF	
72	1	187	assign f_if.almostfull = (count == f_if.FIFO_DEPTH-1)? 1 : 0;	
72	2	1630	assign f_if.almostfull = (count == f_if.FIFO_DEPTH-1)? 1 : 0;	
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
73		1817	Count coming in to IF	
73	1	319	assign f_if.almostempty = (count == 1)? 1 : 0;	
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Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
112		2760	Count coming in to IF	
112	1	2244	if (f_if.rst_n) begin	
516 All False Count				
Branch totals: 2 hits of 2 branches = 100.00%				

Statement

FIFO_cvr.tbt - Notepad

File Edit Format View Help

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

-----Statement Details-----

Statement Coverage for instance /top/DUT --

Line	Item	Count	Source
File FIFO.sv			
8			module FIFO(FIFO_if,DUT f_if);
9			
10			localparam max_fifo_addr = \$clog2(FIFO_DEPTH);
11			
12			reg [f_if.FIFO_WIDTH-1:0] mem [f_if.FIFO_DEPTH-1:0];
13			
14			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
15			reg [max_fifo_addr:0] count;
16			
17	1	3270	always @(posedge f_if.clk or negedge f_if.rst_n) begin
18			if (!f_if.rst_n) begin
19	1	554	wr_ptr <= 0;
20	1	554	f_if.overflow <= 0;
21	1	554	f_if.wr_ack <= 0;
22			end
23			else if (f_if.wr_en && count < f_if.FIFO_DEPTH) begin
24	1	1701	mem[wr_ptr] <= f_if.data_in;
25	1	1701	f_if.wr_ack <= 1;
26	1	1701	wr_ptr <= wr_ptr + 1;

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FIFO_cvr.tbt - Notepad

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26		1701	wr_ptr <= wr_ptr + 1;
27			end
28			else begin
29	1	1015	f_if.wr_ack <= 0;
30			if (f_if.full & f_if.wr_en)
31	1	240	f_if.overflow <= 1;
32			else
33	1	775	f_if.overflow <= 0;
34			end
35			end
36			
37	1	3270	always @(posedge f_if.clk or negedge f_if.rst_n) begin
38			if (!f_if.rst_n) begin
39	1	554	rd_ptr <= 0;
40	1	554	f_if.underflow <= 0;
41			end
42			else if (f_if.rd_en && count != 0) begin
43	1	684	f_if.data_out <= mem[rd_ptr];
44	1	684	rd_ptr <= rd_ptr + 1;
45			end
46			else begin
47			if (f_if.empty & f_if.rd_en)
48	1	112	f_if.underflow <= 1;
49			else
50	1	1920	f_if.underflow <= 0;

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```
FIFO_cvr.bit - Notepad
File Edit Format View Help

49         else
50             1          1920          f_if.underFlow <= 0;
51         end
52     end
53
54     1          3005    always @(posedge f_if.clk or negedge f_if.rst_n) begin
55         if (!f_if.rst_n) begin
56             1          547          count <= 0;
57         end
58         else begin
59             if ( ((f_if.wr_en, f_if.rd_en) == 2'b11) && f_if.full)
60                 1          76          count <= count - 1;
61             else if ( ((f_if.wr_en, f_if.rd_en) == 2'b11) && f_if.empty)
62                 1          83          count <= count + 1;
63             else if ( ((f_if.wr_en, f_if.rd_en) == 2'b10) && !f_if.full)
64                 1          1212         count <= count + 1;
65             else if ( ((f_if.wr_en, f_if.rd_en) == 2'b01) && !f_if.empty)
66                 1          202         count <= count - 1;
67         end
68     end
69
70     1          1818    assign f_if.full = (count == f_if.FIFO_DEPTH)? 1 : 0; //first mistake
71     1          1818    assign f_if.empty = (count == 0)? 1 : 0;
72     1          1818    assign f_if.almostfull = (count == f_if.FIFO_DEPTH-1)? 1 : 0;
73     1          1818    assign f_if.almostempty = (count == 1)? 1 : 0;

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```

```
FIFO_cvr.bit - Notepad
File Edit Format View Help

70     1          1818    assign f_if.full = (count == f_if.FIFO_DEPTH)? 1 : 0; //first mistake
71     1          1818    assign f_if.empty = (count == 0)? 1 : 0;
72     1          1818    assign f_if.almostfull = (count == f_if.FIFO_DEPTH-1)? 1 : 0;
73     1          1818    assign f_if.almostempty = (count == 1)? 1 : 0;
74
75     `ifdef SIM
76     //Assertions
77     //a
78     a_resetBehaviour: assert property (@(posedge f_if.clk) !f_if.rst_n |> !wr_ptr && !rd_ptr && !count);
79     a_resetBehaviour_cvr: cover property (@(posedge f_if.clk) !f_if.rst_n |> !wr_ptr && !rd_ptr && !count);
80     //b
81     a_wr_ack: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) f_if.wr_en && !f_if.full |> ##1 f_if.wr_ack);
82     a_wr_ack_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) f_if.wr_en && !f_if.full |> ##1 f_if.wr_ack);
83     //c
84     a_overflow: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) f_if.full && f_if.wr_en |> ##1 f_if.overflow);
85     a_overflow_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) f_if.full && f_if.wr_en |> ##1 f_if.overflow);
86     //d
87     a_underflow: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) f_if.empty && f_if.rd_en |> ##1 f_if.underflow);
88     a_underflow_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) f_if.empty && f_if.rd_en |> ##1 f_if.underflow);
89     //e
90     a_empty: assert property (@(posedge f_if.clk) !count |> f_if.empty);
91     a_empty_cvr: cover property (@(posedge f_if.clk) !count |> f_if.empty);
92     //f
93     a_full: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == f_if.FIFO_DEPTH |> f_if.full);
94     a_full_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == f_if.FIFO_DEPTH |> f_if.full);

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```

FIFO_cvr.bit - Notepad

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```
89                                     //e
90     a_empty: assert property (@(posedge f_if.clk) !count |-> f_if.empty);
91     a_empty_cvr: cover property (@(posedge f_if.clk) !count |-> f_if.empty);
92     //f
93     a_full: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == f_if.FIFO_DEPTH |-> f_if.Full);
94     a_full_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == f_if.FIFO_DEPTH |-> f_if.Full);
95     //g
96     a_almostfull: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == f_if.FIFO_DEPTH-1 |-> f_if.almostfull);
97     a_almostfull_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == f_if.FIFO_DEPTH-1 |-> f_if.almostfull);
98     //h
99     a_almostempty: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == 1 |-> f_if.almostempty);
100    a_almostempty_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) count == 1 |-> f_if.almostempty);
101
102    //i
103    //read pointer
104    a_rd_ptr_wrap: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) rd_ptr == f_if.FIFO_DEPTH-1 && f_if.rd_en && !f_if.empty |->
105    #1 rd_ptr == 0);
106    a_rd_ptr_wrap_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) rd_ptr == f_if.FIFO_DEPTH-1 && f_if.rd_en && !f_if.empty
107    |-> #1 rd_ptr == 0);
108    //write pointer
109    a_wr_ptr_wrap: assert property (@(posedge f_if.clk) disable iff (!f_if.rst_n) wr_ptr == f_if.FIFO_DEPTH-1 && f_if.wr_en && !f_if.Full |->
110    #1 wr_ptr == 0);
111    a_wr_ptr_wrap_cvr: cover property (@(posedge f_if.clk) disable iff (!f_if.rst_n) wr_ptr == f_if.FIFO_DEPTH-1 && f_if.wr_en && !f_if.Full
112    |-> #1 wr_ptr == 0);
113
114    //j
115    always_comb begin
```

Ln 1, Col 150%Windows (CRLF)UTF-8

Toggle

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
-----	----	----	-----	-----
Toggles	20	20	0	100.00%

=====Toggle Details=====

Toggle Coverage for instance /top/DUT --

Node	1H->0L	0L->1H	"Coverage"
-----	-----	-----	-----
count[3-0]	1	1	100.00
rd_ptr[2-0]	1	1	100.00
wr_ptr[2-0]	1	1	100.00

Total Node Count = 10
Toggled Node Count = 10
Untoggled Node Count = 0
Toggle Coverage = 100.00% (20 of 20 bins)

=====

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
-----	----	----	-----	-----
Toggles	86	86	0	100.00%

=====Toggle Details=====

Toggle Coverage for instance /top/f_if --

Node	1H->0L	0L->1H	"Coverage"
-----	-----	-----	-----
almostempty	1	1	100.00
almostfull	1	1	100.00
clk	1	1	100.00
data_in[15-0]	1	1	100.00
data_out[15-0]	1	1	100.00
empty	1	1	100.00
full	1	1	100.00
overflow	1	1	100.00
rd_en	1	1	100.00
rst_n	1	1	100.00
underflow	1	1	100.00
wr_ack	1	1	100.00
wr_en	1	1	100.00

Total Node Count = 43
Toggled Node Count = 43
Untoggled Node Count = 0
Toggle Coverage = 100.00% (86 of 86 bins)

Functional Coverage

Note: Some Exclusion have been done to achieve the 100% functional coverage

- 1- Exclusion of bin wr_en = 1, rd_en = 1 and full = 1 because that cannot happen
- 2- Exclusion of bin wr_en = 0, rd_en = 1 and full = 1 because that cannot happen
- 3- Exclusion of bin wr_en = 0, rd_en=1 and overflow =1 because that cannot happen
- 4- Exclusion of bin wr_en = 0, rd_en = 0 and overflow = 1 because that cannot happen
- 5- Exclusion of bin wr_en = 1, rd_en = 0 and underflow = 1 because that cannot happen
- 6- Exclusion of bin wr_en = 0, rd_en = 0 and underflow = 1 because that cannot happen
- 7- Exclusion of bin wr_en = 0, rd_en = 1 and wr_ack = 1 because that cannot happen
- 8- Exclusion of bin wr_en = 0, rd_en = 0 and wr_ack = 1 because that cannot happen

fcover_report.txt - Notepad

File Edit Format View Help

Coverage Report by instance with details

=====
Instance: /FIFO_coverage_pkg
Design Unit: work.FIFO_coverage_pkg
=====

Covergroup Coverage:

Covergroups	1	na	na	100.00%
Coverpoints/Crosses	16	na	na	na
Covergroup Bins	66	66	0	100.00%

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/FIFO_cvr	100.00%	100	-	Covered
covered/total bins:	66	66	-	
missing/total bins:	0	66	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
type_option.strobe=0				
type_option.merge_instances=auto(1)				
Coverpoint write_en	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	850	1	-	Covered
bin auto[1]	2153	1	-	Covered
Coverpoint read_en	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2116	1	-	Covered
bin auto[1]	867	1	-	Covered
Coverpoint full	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2639	1	-	Covered

Ln 1, Col 1 50% Windows (CRLF) UTF-8

fcover_report.txt - Notepad				
File	Edit	Format	View	Help
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2639	1	-	Covered
bin auto[1]	363	1	-	Covered
Coverpoint almostfull	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2709	1	-	Covered
bin auto[1]	293	1	-	Covered
Coverpoint empty	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2565	1	-	Covered
bin auto[1]	437	1	-	Covered
Coverpoint almosempty	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2492	1	-	Covered
bin auto[1]	510	1	-	Covered
Coverpoint overflow	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2704	1	-	Covered
bin auto[1]	298	1	-	Covered
Coverpoint underflow	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2871	1	-	Covered
Ln 1, Col 1 50% Windows (CRLF) UTF-8				

fcover_report.txt - Notepad				
File	Edit	Format	View	Help
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	2871	1	-	Covered
bin auto[1]	131	1	-	Covered
Coverpoint write_ack	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
bin auto[0]	1301	1	-	Covered
bin auto[1]	1701	1	-	Covered
Cross cross_full	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[0]>	632	1	-	Covered
bin <auto[0],auto[1],auto[0]>	255	1	-	Covered
bin <auto[1],auto[0],auto[1]>	302	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1219	1	-	Covered
bin <auto[0],auto[0],auto[1]>	61	1	-	Covered
bin <auto[0],auto[0],auto[0]>	533	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin_full2	0	-	-	ZERO
ignore_bin_full1	0	-	-	ZERO
Cross cross_almostfull	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	128	1	-	Covered
bin <auto[0],auto[1],auto[1]>	21	1	-	Covered
bin <auto[1],auto[0],auto[1]>	90	1	-	Covered
bin <auto[0],auto[0],auto[1]>	54	1	-	Covered
bin <auto[1],auto[1],auto[0]>	504	1	-	Covered
bin <auto[0],auto[1],auto[0]>	234	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1431	1	-	Covered
bin <auto[0],auto[0],auto[0]>	540	1	-	Covered
Cross cross_empty	100.00%	100	-	Covered
covered/total bins:	8	8	-	
Ln 1, Col 1 50% Windows (CRLF) UTF-8				

fcover_report.txt - Notepad				
File	Edit	Format	View	Help
Cross cross_empty	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	67	1	-	Covered
bin <auto[0],auto[1],auto[1]>	92	1	-	Covered
bin <auto[1],auto[0],auto[1]>	145	1	-	Covered
bin <auto[0],auto[0],auto[1]>	133	1	-	Covered
bin <auto[1],auto[1],auto[0]>	565	1	-	Covered
bin <auto[0],auto[1],auto[0]>	163	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1376	1	-	Covered
bin <auto[0],auto[0],auto[0]>	461	1	-	Covered
Cross cross_almostempty	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	179	1	-	Covered
bin <auto[0],auto[1],auto[1]>	37	1	-	Covered
bin <auto[1],auto[0],auto[1]>	199	1	-	Covered
bin <auto[0],auto[0],auto[1]>	95	1	-	Covered
bin <auto[1],auto[1],auto[0]>	453	1	-	Covered
bin <auto[0],auto[1],auto[0]>	218	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1322	1	-	Covered
bin <auto[0],auto[0],auto[0]>	499	1	-	Covered
Cross cross_overflow	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	91	1	-	Covered
bin <auto[1],auto[0],auto[1]>	207	1	-	Covered
bin <auto[1],auto[1],auto[0]>	541	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1314	1	-	Covered
bin <auto[0],auto[1],auto[0]>	255	1	-	Covered
bin <auto[0],auto[0],auto[0]>	594	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin overflow2	0	-	-	ZERO
ignore_bin overflow1	0	-	-	ZERO
Cross cross_underflow	100.00%	100	-	Covered

Ln 1, Col 1 50% Windows (CRLF) UTF-8

fcover_report.txt - Notepad				
File	Edit	Format	View	Help
bin <auto[1],auto[1],auto[0]>	541	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1314	1	-	Covered
bin <auto[0],auto[1],auto[0]>	255	1	-	Covered
bin <auto[0],auto[0],auto[0]>	594	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin overflow2	0	-	-	ZERO
ignore_bin overflow1	0	-	-	ZERO
Cross cross_underflow	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	97	1	-	Covered
bin <auto[1],auto[1],auto[0]>	535	1	-	Covered
bin <auto[0],auto[1],auto[1]>	34	1	-	Covered
bin <auto[0],auto[1],auto[0]>	221	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1521	1	-	Covered
bin <auto[0],auto[0],auto[0]>	594	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin underflow2	0	-	-	ZERO
ignore_bin underflow1	0	-	-	ZERO
Cross cross_write_ack	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
type_option.weight=1				
type_option.goal=100				
type_option.comment=				
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	489	1	-	Covered
bin <auto[1],auto[0],auto[1]>	1212	1	-	Covered
bin <auto[1],auto[1],auto[0]>	143	1	-	Covered
bin <auto[1],auto[0],auto[0]>	309	1	-	Covered
bin <auto[0],auto[1],auto[0]>	255	1	-	Covered
bin <auto[0],auto[0],auto[0]>	594	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin wr_ack2	0	-	-	ZERO
ignore_bin wr_ack1	0	-	-	ZERO

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%

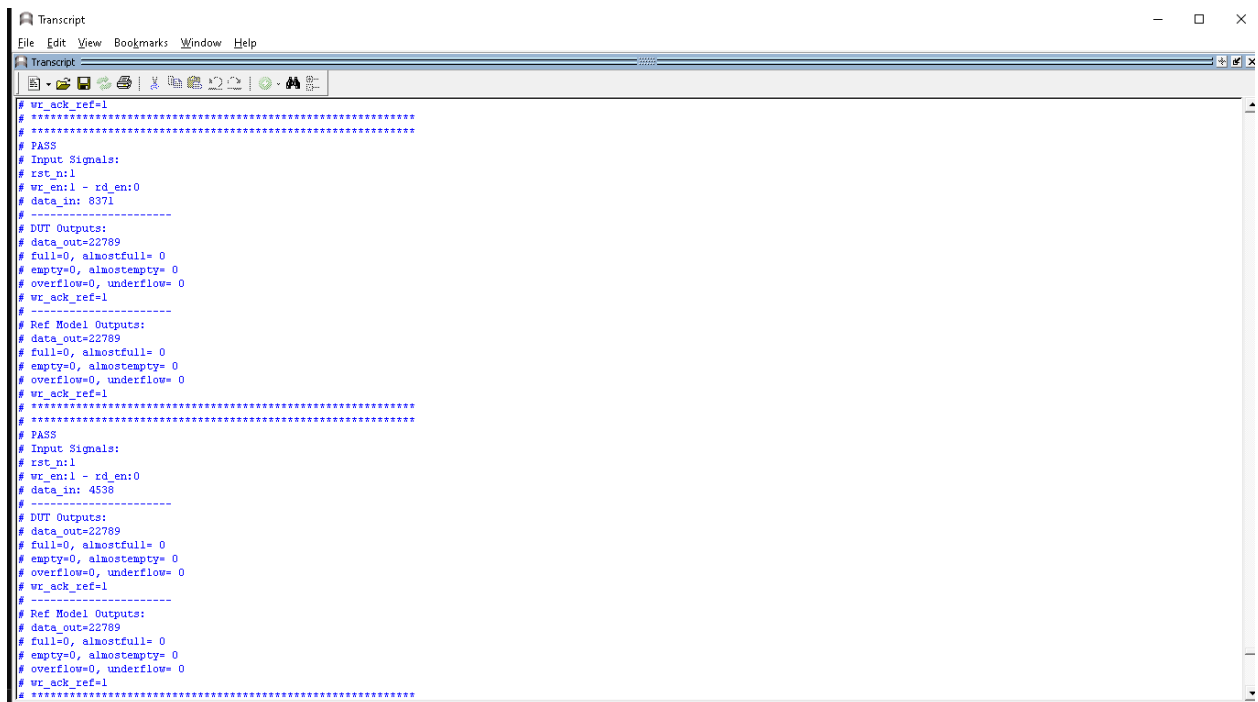
Assertion Coverage

DIRECTIVE COVERAGE:						
Name	Design Unit	Design Unit Type	Lang	File(Line)	Hits	Status
/top/DUT/a_resetBehaviour_cvr	FIFO	Verilog	SVA	FIFO.sv(80)	288	Covered
/top/DUT/a_wr_ack_cvr	FIFO	Verilog	SVA	FIFO.sv(84)	1546	Covered
/top/DUT/a_overflow_cvr	FIFO	Verilog	SVA	FIFO.sv(88)	211	Covered
/top/DUT/a_underflow_cvr	FIFO	Verilog	SVA	FIFO.sv(92)	97	Covered
/top/DUT/a_empty_cvr	FIFO	Verilog	SVA	FIFO.sv(96)	682	Covered
/top/DUT/a_full_cvr	FIFO	Verilog	SVA	FIFO.sv(100)	322	Covered
/top/DUT/a_almostfull_cvr	FIFO	Verilog	SVA	FIFO.sv(104)	269	Covered
/top/DUT/a_almostempty_cvr	FIFO	Verilog	SVA	FIFO.sv(108)	463	Covered
/top/DUT/a_rd_ptr_wrap_cvr	FIFO	Verilog	SVA	FIFO.sv(113)	21	Covered
/top/DUT/a_wr_ptr_wrap_cvr	FIFO	Verilog	SVA	FIFO.sv(116)	110	Covered
TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 10						
ASSERTION RESULTS:						
Name	File(Line)	Failure Count	Pass Count			
/top/a_reset_1	FIFO_top.sv(17)	0	1			
/top/a_reset_2	FIFO_top.sv(18)	0	1			
/top/a_reset_3	FIFO_top.sv(19)	0	1			
/top/DUT/a_resetBehaviour	FIFO.sv(79)	0	1			
/top/DUT/a_wr_ack	FIFO.sv(83)	0	1			
/top/DUT/a_overflow	FIFO.sv(87)	0	1			
/top/DUT/a_underflow	FIFO.sv(91)	0	1			
/top/DUT/a_empty	FIFO.sv(95)	0	1			
/top/DUT/a_full	FIFO.sv(99)	0	1			
/top/DUT/a_almostfull	FIFO.sv(103)	0	1			
/top/DUT/a_almostempty	FIFO.sv(107)	0	1			
/top/DUT/a_rd_ptr_wrap	FIFO.sv(112)	0	1			
/top/DUT/a_wr_ptr_wrap	FIFO.sv(115)	0	1			
/top/DUT/a_rd_ptr_thr	FIFO.sv(121)	0	1			
/top/DUT/a_wr_ptr_thr	FIFO.sv(122)	0	1			
/top/DUT/a_count_thr	FIFO.sv(123)	0	1			
/top/TB/#ublk#182146786#28/immed__29						

Simulation

Transcript

Transcript	
File Edit View Bookmarks Window Help	
Transcript	
# Input Signals: # rst_n:0 # wr_en:0 - rd_en:0 # data_in:30422 # ----- # DUT Outputs: # data_out=22789 # full=0, almostfull= 0 # empty=1, almostempty= 0 # overflow=0, underflow= 0 # wr_ack_ref=0 # ----- # Ref Model Outputs: # data_out=22789 # full=0, almostfull= 0 # empty=1, almostempty= 0 # overflow=0, underflow= 0 # wr_ack_ref=0 # ***** # Correct Test \$TB = 3001, Error Test \$TB = 0 # ***** # PASS # Input Signals: # rst_n:0 # wr_en:0 - rd_en:0 # data_in:30422 # ----- # DUT Outputs: # data_out=22789 # full=0, almostfull= 0 # empty=1, almostempty= 0 # overflow=0, underflow= 0 # wr_ack_ref=0 # ----- # Ref Model Outputs: # data_out=22789 # full=0, almostfull= 0 # empty=1, almostempty= 0 # overflow=0, underflow= 0 # wr_ack_ref=0 # ***** # Correct Tests = 3003, Error Tests = 0 # ** Note: \$stop : FIFO_monitor.sv(40) # Time: 6008 ns Iteration: 1 Instance: /top/MONITOR	



Waveform

