Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
SLAVE_1	When the rst_n is asserted, the output MISO value should be low & the state cs turns back to IDLE	Directed at the start of the simulation, and then randomized with constraint that drives the reset to be off 99% of the simulation time	-	A checker in the reference model to check for the synchronous reset functionality
SLAVE_2	When the reset is deasserted, SS_n is asserted to tell the slave that the master starts communication & then deasserted to end communication	Randomized with constraint that drives the SS_n to be on every 13 clk cycles if the current state is normal operations or to be on every 23 clk cycles if the current state is read data	Covers transaction duration: 1 → 0 [*13] → 1 for normal operations & Check extended transaction: 1 → 0 [*23] → 1 for read data	A checker in the reference model to check for the functionality
SLAVE_4	When the reset is deasserted, the slave receives MOSI bit by bit & converts the data from serial "MOSI" to parallel	Randomized with a constraint that ensures that the most significant 3 bits follow the sequence of write address -> write data -> read address -> read data	Covers validate correct transition: 0->0->0 (for write address), 0->0->1 (for write data),1->1->0 (for read address), 1->1->1(for read data)	A checker in the reference model to check for the functionality
SLAVE_5	When the reset is deasserted, tx_valid is asserted when the slave is ready to send the parallel data to the RAM	Randomized with constraint that drives the tx_valid to be on when the current state is read data & the data is ready to be transmitted (when the counter indicates that)	-	A checker in the reference model to check for the functionality