A Fully CMOS Integrated RF Transceiver for Ubiquitous Networks in Sub-GHz ISM-band

Hae-Moon Seo, Yeon-Kug Moon, Yong-Kuk Park, Sang-Shin Lee, Tae-Ho Hwang, Byoung-Gwan Min, Kwang-Ho Won, Myung-Hyun Yoon, Jun-Jae Yoo, Seong-Dong Kim

Ubiquitous Computing Research Center, Korea Electronics Technology Institute (KETI)
#68, Yatap-Dong, Bundang-Gu, Sungnam-Si, KyungGi-Do, Korea
E-mail: bmoons@keti.re.kr

Abstract — A fully CMOS integrated radio frequency (RF) transceiver for wireless sensor networks in sub-GHz ISM-band applications is implemented and measured. The IC is fabricated in 0.18-μm CMOS technology and packaged in LPCC package. The fully monolithic transceiver consists of a receiver, a transmitter and a RF synthesizer with on-chip VCO. The chip fully complies with the IEEE 802.15.4 WPAN standard in sub-GHz mode. The receiver sensitivity is –98dBm and the transmitter achieves less than 6.3% error vector magnitude (EVM) for 40kbps mode. The chip uses 1.8V power supply and the current consumption is 14mA for reception mode ad 16mA for transmission mode.

Index terms – wireless sensor network, integrated circuit, CMOS, RF transceiver, low power

1. INTRODUCTION

Recently, the desire for wireless connectivity has led an exponential growth in wireless communication. In particular, wireless sensor networks are potential wireless network application for the following future ubiquitous computing system. Wireless sensor networks are an emerging research area with potential applications in environmental monitoring, surveillance, military, health and security [1]. The power dissipation of wireless sensor networks does require low power consumption for several years' operation.

There has been a great deal of interest in realizing low power, low cost, compact RF transceiver for wireless sensor networks. Several technological trends that are driving the technical evolution of wireless technology include the process scaling of CMOS transistors and higher and higher bandwidth available at ISM bands. Almost all of the license free bands propose both linear and nonlinear modulation standards for wireless applications, thus requiring different design optimizations in the RF transceiver. Along with these issues, there exists the challenge to develop fully integrated wireless solutions in silicon-based substrates [2].

In this paper we present the development of a fully single chip 0.18-μm CMOS RF transceiver targeted towards ubiquitous wireless sensor networks in sub-GHz ISM-band applications.

Section 2 of this paper describes the architecture and implementation of RF transceiver. The measurement results are presented in Section 3, then some final conclusions are offered in Section 4.

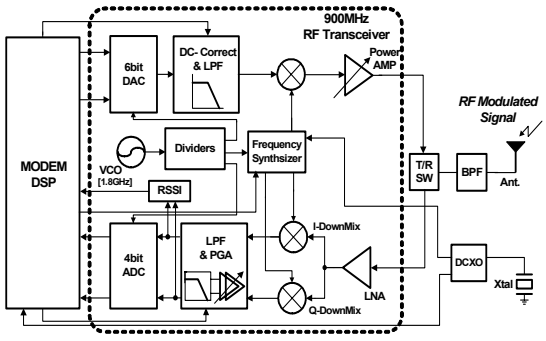

Fig.1 RF transceiver block diagram supporting wireless sensor networks in sub-GHz ISM-band

2. RF SYSTEM IMPLEMENTATION

2.1 RF transceiver architecture

The communication nodes are required to integrate with one die for low power and low cost wireless sensor network applications. With first step, we did implement RF transceiver chip including an ADC and a DAC. Fig.1 shows the architecture of a radio chip, which consists of a receiver, a transmitter, and a frequency synthesizer with on-chip VCO.

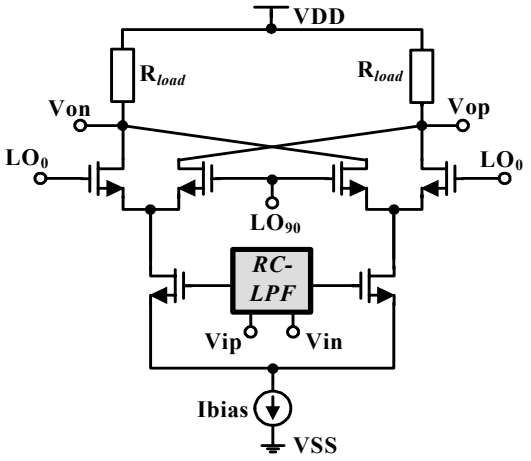

Fig.2 Up-conversion mixer with RC low-pass filter.

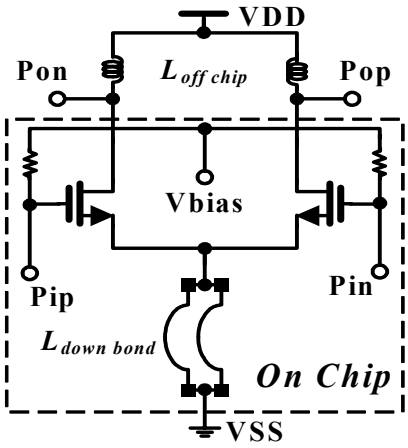

Fig.3 Power amplifier with off-chip inductor

The receiver adopts zero-IF architecture [3], [4] to have low power consumption, low cost and small size. The sub-GHz RF signal is first amplified by a low noise amplifier (LNA) and then down-converted to zero-IF I/Q signals by two identical mixers driven by quadrature local-oscillator (LO) signals from a frequency synthesizer. At the analog baseband stage, using a third-order RC filter and programmable gain amplifier simultaneously performs channel selection filtering, signal amplification, and dc-offset cancellation. And I/Q 4bit dual flash-ADCs are connected for interface of MODEM block.

The transmitter adopts a general zero-IF modulation with up-conversion mixer. Baseband BPSK signals generated by digital modulator in MODEM block are followed a 6-bit DAC. A mixer up-converts the baseband signal directly 900-MHz, which is combined by RC low-pass filter. Since BPSK modulation is a constant envelop modulation, a nonlinear power amplifier with high efficiency can be used.

For generating 900-MHz LO signals with 2-MHz channel spacing, an integer-N frequency synthesizer derived from a 30-MHz crystal oscillator with 30ppm accuracy is implemented. A 1.8GHz LO signal is generated by a voltage-controlled oscillator (VCO) with a small area and high Q on-chip inductor. The 900-MHz LO I/Q signals are then generated by a divide-by-two circuit. The frequency synthesizer is implemented in fully differential type, for immunity to common mode noise.

2.2 RF transceiver design

RF transceiver is designed using 0.18-μm CMOS process including six metal layers with 2-um thick top metal. This process provides high gain and good quality factor Q for on-chip inductor, resulting in low power consumption in RF and analog circuits.

In the transmitter path, the BPSK modulated baseband signal is converted digital-to-analog before being applied to frequency up-translation block. Fig.2 shows the schematic of up-conversion mixer with RC low-pass filter. The baseband analog signal is filtered by second RC low-pass filter, and then is translated into RF frequency by modulator with conventional CMOS Gilbert cell. This double-balanced mixer converts baseband signal directly up 900-MHz and deliver –20dBm differential signal to power amplifier. LO emission is due to differential mismatch in the mixer circuit, while spectrum regrowth is due to LO (0/90 degree) quardrature imbalance and nonlinearity of the mixer. Layout is fulfilled very carefully to maintain symmetry for differential and quardrature signals, which minimizes both LO emission and spectrum regrowth. Fig.3 show the power amplifier of a differential common source topology with off-chip inductor, having a high Q. The multiple down-bond wire inductors are applied for the minimization of spectrum regrowth. The estimated DC current consumption of a transmitter path is 8mA.

The front-end of receiver chain consists of low-noise amplifier (LNA), quardrature down-conversion mixer. The fully balanced sub-GHz

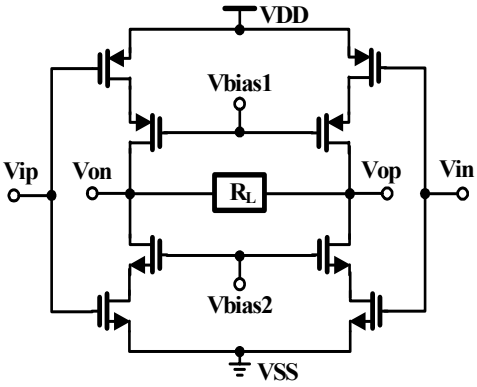

Fig.4 Low noise amplifier circuit

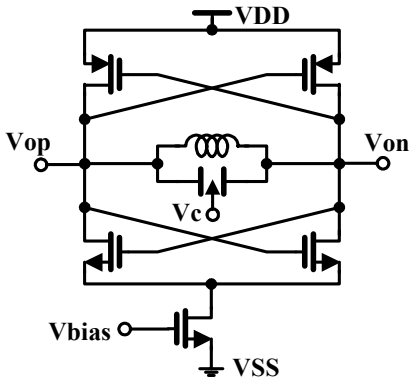

Fig.5 Voltage-controlled oscillator circuit

LNA shown in Fig. 4 uses current- reuse complementary technique (pMOS and nMOS) without inductor requiring large area. Input matching is realized by external passive components. The LNA features 2.6-dB noise figure (NF) and a third-order input intercept point (IIP3) of -5.2dBm at maximum gain. The output of LNA is down-converted directly into a common analog baseband path by a Gilbert-cell-based quadrature frequency demodulator. The selection of the vertical bipolar transistors in the switching quadrant decrease the gain of mixer, however, the average integrated noise floor in the direct-conversion receiver improves due to the reduced 1/f noise. The large voltage headroom achieved by Gilbert multiplier type with source grounded topology helps maximize the contribution of linearity in the overall IIP3. The estimated IIP3 is 6dBm. Gain control is distributed into two programmable gain amplifiers (PGAs) located before and after channel selection filters. The range of gain control is 63dB with 1dB-step. The I/Q third-order Sallen-and-key RX filters are implemented as a cascade of second biquad cell and single pole cell. And I/Q 4bit dual flash-ADCs are designed for interface of MODEM block. The estimated maximum DC current consumption of a receiver path is 6mA.

The integer-N frequency synthesizer, using a second-order passive loop filter, generates the LO signal for transmit/receive mode. A crystal reference of 30-MHz is internally divided. To minimize pulling, the 900-MHz LO signals are generated by 1.8-GHz voltage controlled oscillator (VCO), shown in Fig.5. The LC-resonator consists of four-turn spiral inductor and varactor.

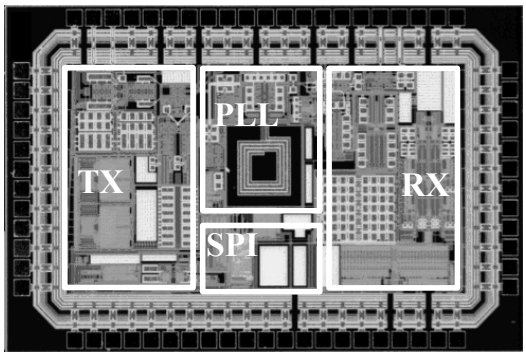

Fig.6 Die microphotograph

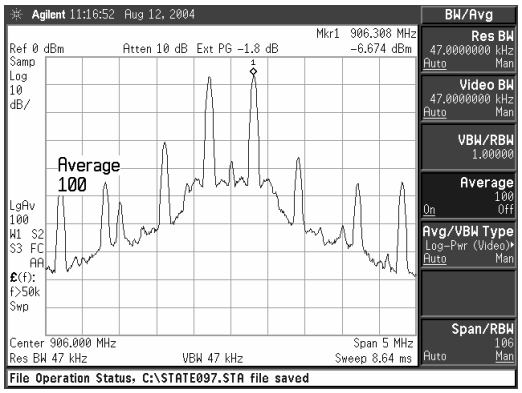

Fig.7 Transmitter single-tone output

The negative-Gm core cell has nMOS/pMOS complementary topology for high power efficiency and gain.

$$f_{OSC} = \frac{1}{2\pi\sqrt{LC_{eff}}} \quad (1)$$

The oscillation frequency of VCO is shown as

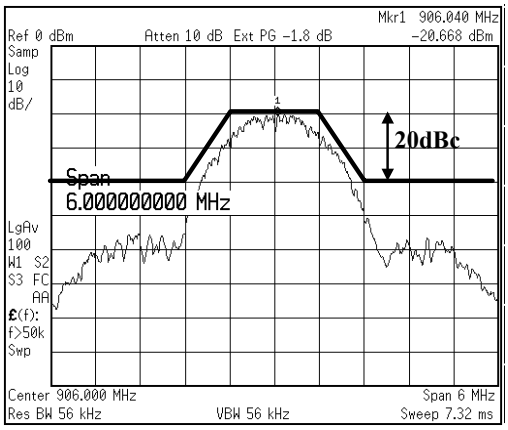

Fig.8 Transmitter output spectrum mask

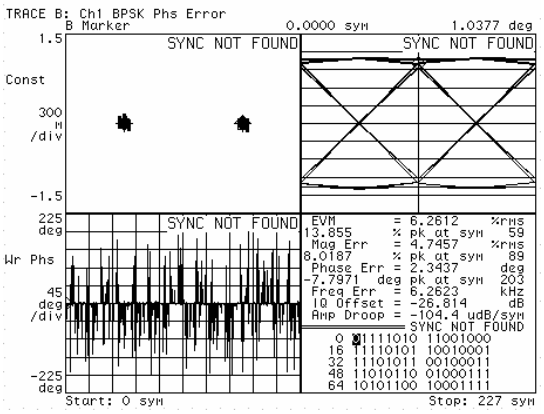

Fig.9 Transmitter output error vector magnitude (EVM)

equation (1). The tuning frequency of VCO is simulated from 1.6-GHz to 2.2-GHz. The divider circuit for high frequency has a structure of negative-feedback type using two latches. The phase frequency detector (PFD) consists of two D-flip-flop (DFF), AND-gate, and delay-time block for locking speed and high linearity of phase transfer function. The charger-pump circuit has a structure of nMOS/pMOS cascade-type to minimize of up/down current mismatch and output switching noise. The clock generation block provides a reference clock of PLL and sampling-clocks of ADC/DAC using an external 30-MHz crystal-oscillator.

3. MEASURED RESULTS

A radio transceiver die microphotograph, which

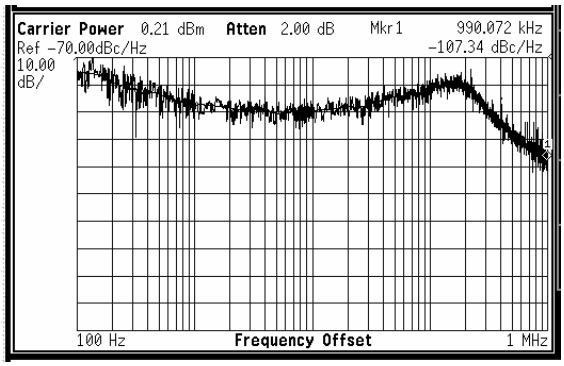

Fig.10 Frequency synthesizer: phase noise

TABLE I
THE MEASURED RESULTS OF RF TRANSCEIVER

Specification	Simulated	Measured
VDD	1.8V	1.8V
DC current consumption	Rx./Tx.:14 /15mA	Rx./Tx.:14/16mA
Die size	1.6*2.4mm^2 (containing PAD)	
NF/Sensitivity	8dB/-99dBm	9dB/-98dBm
IIP3	-5dBm	-7dBm
Max. gain	90dB	88dB
AGC gain range	86	86
Selectivity (@5MHz)	-50dBc	-48dBc
TX power	+3dBm	0dBm
EVM	-	6.3%
P1-dB (output)	+4dBm	+1dBm
LO phase noise(@1MHz)	-110dBc	-108dBc

consists of transmitter, receiver, and frequency synthesizer with on-chip VCO, is shown in Fig. 6. The total die area is 1.6*2.4mm^2 and it consumes only 29mW in the transmit-mode and 25mW in the receive-mode, and a LPCC48 package is used. The single-tone output of transmitter chain is shown in Fig. 7. The 300-KHz baseband single signal is up-converted by 906-MHz RF carrier signal and wanted-signals are above 25-dBc than third-order harmonics. The spectrum at the output of transmitter satisfies the required spectrum mask as shown in Fig. 8, which is above 28-dBc at the ±1.2-MHz offset frequency. Due to the low in-band integrated phase noise and the digital calibration that eliminates I/Q mismatch and baseband filter mismatch, transmitter EVM is dominated by nonlinearities [4-5]. As shown in Fig.9, a reference design achieves 6.3% EVM for an output power of –3dBm for sub-GHz ISM-band. The output P1-dB

of transmitter is +1dBm. The receiver features an NF of 9 dB for 900-MHz band and achives –98dBm sensitivity at the input of chip for the IEEE 802.15.4 BPSK mode [6-7]. Receive IIP3 is –7dBm and the maximum gain of receiver is 88dB. The automatic gain control (AGC) of receiver is 86dB with 1dB step and selectivity is –48dBc at 5-MHz offset frequency. As shown in Fig.10, the in band phase noise of frequency synthesizer is –75dBc/Hz and phase noise of VCO is –108dBc at 1-MHz offset frequency. The Table I show the simulated and measured results of radio transceiver.

4. CONCLUSON

A fully CMOS integrated radio frequency (RF) transceiver for wireless sensor networks in sub-GHz ISM-band applications is implemented and measured. The IC is fabricated in 0.18-µm CMOS technology and packaged in LPCC package. The fully monolithic transceiver consists of a receiver, a transmitter and a RF synthesizer with on-chip VCO. The chip fully complies with the IEEE 802.15.4 WPAN standard in sub-GHz mode. The receiver sensitivity is –98dBm and the transmitter achieve less than 6.3% error vector magnitude (EVM) for 40kbps mode. The chip uses 1.8V power supply and the current consumption is 14mA for reception mode ad 16mA for transmission mode.

REFERENCE

[1] Hae-Moon Seo, Yong-Kuk Park, et al, “Low Power RF Receiver Requirements of Low-rate WPAN for Coexistence with Various Wireless Devices in 2.4GHz ISM-band”, Asia-Pacific Microwave Conference, India, IEEE, Dec. 2004.

[2] Saikat Sarkar, Padmanava Sen, et al,“Development of 2.4 GHz RF Transceiver Front-end Chipset in 0.25µm CMOS”, Proceedings of the 16th International Conference on VLSI Design, 2003.

[3] I. Bouras, S. Bouras, at.al, “A digitally calibrated 5.15- 5.825 GHz transceiver for 802.11A wireless LANS in 0.18u/m CMOS,” in IEEE Int. Solid-State Conf. Dig.Tech. Papers, Feb. 2003, pp. 352–353.

[4] I. Vassiliou, K. Vavelidis, et.al, “A single-chip digitally calibrated 5.15 GHz-5.825 GHz 0.18-um CMOS transceiver for 802.11a wireless LAN”, IEEE J. Solid-State Circuits, vol. 38, pp. 2221–2231, Dec. 2003.

[5] K. Vavelidis, I. Vassilioui, et. Al, “ A dual-band 5.15-5.35-GHz, 2.4-2.5-GHz 0.18um CMOS Transceiver for 802.11a/b/g wireless LAN”, IEEE J. Solid-State Circuits, vol. 39, pp. 1180-1185, July, 2004.

[6] IEEE Computer Society, “IEEE Standard for Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low Rate Wireless Personal Area Networks (LR-WPANs)”, IEEE Std 802.15.4TM-2003.

[7] Sean Middleton, “IEEE 802.15 WPAN Low Rate Study Group PAR”, Document number IEEE P802.15-00/248r3, submitted Sept. 2000.