A CMOS Continuous-Time Gm-C Filter and Programmable Gain Amplifier for WPAN Receivers

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Abstract: This paper describes a low-voltage and low-power channel selection analog front end with continuous-time low pass filters and highly linear programmable-gain amplifier(PGA). The filters were realized as balanced Gm-C biquadratic filters to achieve low current consumption. High linearity and constant wide bandwidth are achieved by using a new transconductance(Gm) cell. The PGA has a voltage gain varying from 0 to 65dB, while maintaining a constant bandwidth. A filter tuning circuit that requires an accurate time base but no external components is presented. Both the filter and PGA were implemented in a 0.18um 1P6M n-well CMOS process. They consume 3.2mW from a 1.8V power supply and occupy an area of 0.19mm^2.

1. Introduction

The demand for low-cost low-power wireless tranceivers operating in the Wireless Personal Area Network(WPAN) has led to extensive research on RF circuit design[1]. Particularly, since one of the characteristics of such a WPAN transceiver is that it has wider channel spacing than the BW channel has, its filter attenuation requirement is lower than other wireless communication specifications[2]. Thus, it is possible to use a filter of a lower order, and it necessarily requires characteristics of low power consumption and low cost. This paper suggests that the Analog Front End in transceiver is relevant to this WPAN.

2. Analog Front End

Figure 1 shows the Analog Front End (AFE) of the designed receiver. The third Butterworth filter was implemented using cascade composition of the biquad cell and the single pole cell, and the programmable gain cell was stationed at the middle to improve the cascaded dynamic range. For the 1/f noise, a significant problem in a DCR structure, the interference element is removed by using the single pole of the current driving type at the output stage of the Mixer. And it suggests the offset cancellation structure using DAC to improve the problem of the DC offset.

2.1 Channel Selection Filter

The Channel filter allows a signal of the desired band to pass, and attenuates the adjacent channel and the alternate channel interferer. The filter requirement in this paper is as follows. Since it is a DCR structure, 1/f noise should be reduced and DC offset should be small. And in order to alleviate the SFDR requirements of PGA and ADC, most of the interference is filtered in the first part. Figure 2 shows the designed third Butterworth LPF. The interference element is removed by using the single pole of the current driving type at the output stage of the Mixer, and the loss at in-band is compensated by using the overshoot of biquad. Figure 3 shows a Gm-cell. Two Gm-cells are used as one to reduce the area that LPF occupies. Passive R and the size of MOS should be properly adjusted to improve the linearity of the Gm-cell.

2.2 Programmable-Gain Amplifier

The signal level of RF input requires a minimum dynamic range of 72dB as – 92dBm ~ -20dBm. The AGC control signal receives the digital control signal from the Modem to control the gain of the receiver. Figure 4 shows the circuit of PGA, and the PGA of this receiver utilizes the three gain stages to control the gain of 0 ~ 65dB with 1 dB step. The resistor switching method was utilized in order to not lose the linearity of PGA.

2.3 Filter Tuning Circuit

Since the mask characteristics of the Gm-C filter are decided by the Gm value, the Gm has to be maintained as a proper value to keep a pole frequency. And since the Gm value should not be changed even by process variation or outer environment changes, here, as shown in Figure 5, it chose Gm Setting type, and the required current for sinking or sourcing is designed to minimize changes of Gm by minimizing current change due to the temperature variation from Bias Block. Current I1 in Figure 5 offsets the MOS of the Bias part as well as the temperature variation of resistance so as to minimize the changes of voltage V_{ab} due to the temperature and to evenly maintain the input voltage of the Gm-cell. If the cut-off frequency differs from the designed value as a parameter set up the first time it distorts the value of Gm by the process variations, Gm should be adjusted by changing current I2 by fusing.

2.4 DC Offset Adjustment

For DC offset adjustment, 8-bit digital data for I/Q from the Modem are input to control the DC offset at the back side of PGA1 to use the feedback loop to reduce the offset at the LPF output. Figure 6 shows the DAC to convert the 8-bit data into the input voltage of the PGA. The resolution for 1 bit is 5mV, and the DC offset change at the LPF output is ±640mV. The size of MOS used as a current mirror of the DAC circuit has to be appropriate in consideration of the current mismatch.

3. Measurement Results

The chip photograph of the proposed Analog Front End is shown in Figure 7, and the active chip area excluding pads is 0.19mm^2. The 2-T signal of the same power was applied by RF input, and the powers of the fundamental

signal and IM3 element were measured as gradually increasing the power of the input signal. V_{IIP3} is about $6V_{rms}$. Figure 8 shows the mask characteristics of LPF, and Figure 9 shows the PGA output spectrum after applying the signal of -65dBm by RF input and setting the PGA Gain as 39dB. With a 1-Vrms differential input and output, the filter achieves -85dB THD and a 78dB signal-to-noise ratio. Table 1 shows the related output characteristics of AFE.

References

[1] Pilsoon Choi et.al, "An Experimental Coin-Sized Radio for Extremely Low-Power WPAN Application at 2.4GHz," IEEE J. Solid-State Circuits, vol. 38, no.12, pp. 2258~2268, Dec. 2003

[2] C. Cojocaru et.al, "A 43mW Bluetooth transceiver with –91dBm sensitivity," ISSCC Dig. Tech. Papers, pp. 90~91, Feb. 2003.

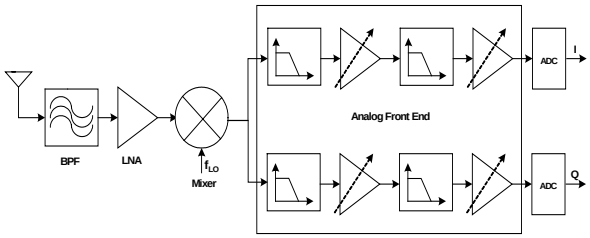

Fig. 1. Block diagram of the analog front end

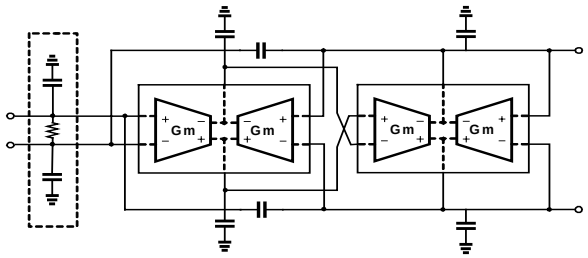

Fig. 2. The designed 3rd Butterworth LPF

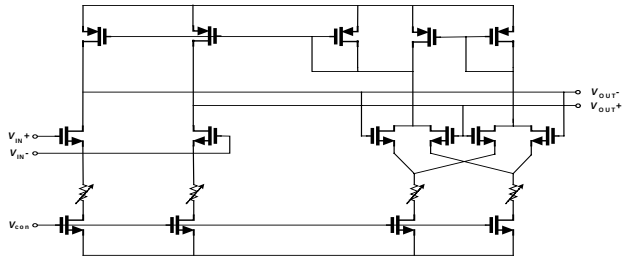

Fig. 3. Circuit diagram of Gm-cell

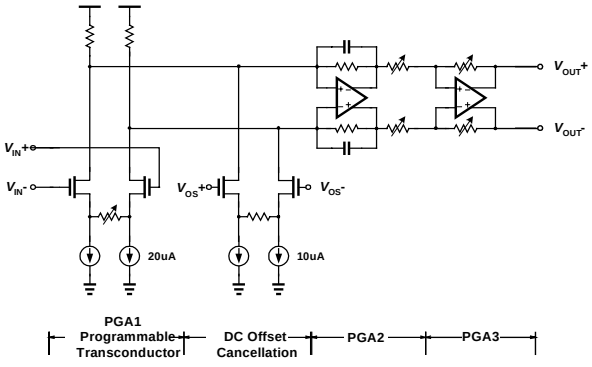

Fig. 4. Circuit schematic of PGA

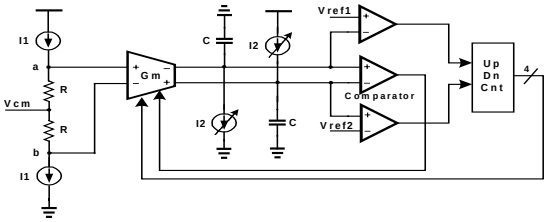

Fig. 5. Tuning Circuit

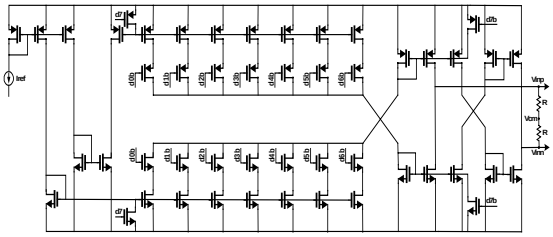

Fig. 6. DAC for DC offset adjustment

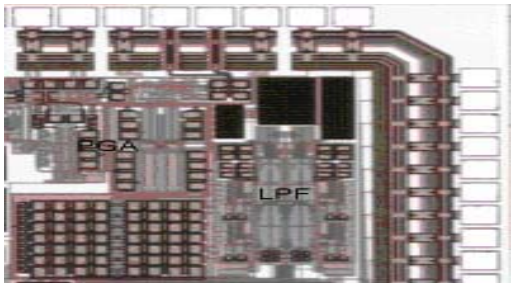

Fig. 7. Chip photograph

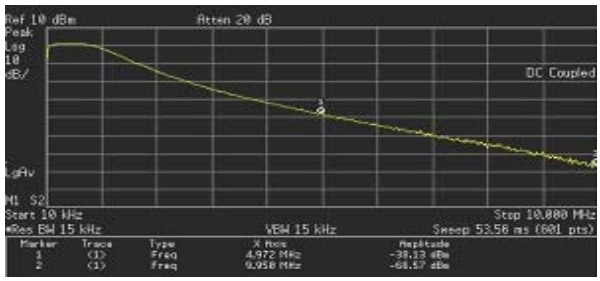

Fig. 8. The mask characteristics of LPF

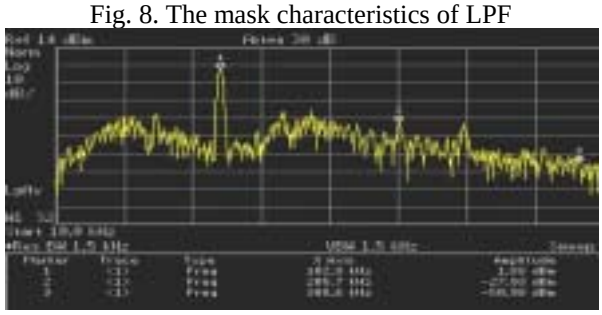

Fig. 9. PGA output spectrum

Table 1. Summary of measured Results

Power Supply	1.8V
Technology	0.18u CMOS
Chip Area	$0.19mm^2$
Power Dissipation	3.2mW
-3dB Bandwidth	900kHz to 2MHz
-3dB Variation	< ±1%
Group Delay	62nsec
VGA gain	0 ~ 65dB
V_{IIP3}	6 V_{rms}
THD	-85dB