Digital Backend Design of Implantable RFID Tag

Yong-Ju Park, Hyun-Suk Ahn, Young-Han Kim, Yong-Suk Lim,
Seung-Ok Lim and Myung-Hyun Yoon
Network Convergence Research Center
Korea Electronics Technology Institute (KETI)
1599 Sangam-dong Mapo-gu, Seoul, Korea
[suede8247, hsahn, ekmyph, busytom, solim and mhyoon]@keti.re.kr

***Abstract*—Passively powered radio frequency identification (RFID) tags are devices powered via harvested ultra-high frequency (UHF) radiation emitted by a reader device. These devices are relegated to a form wireless barcode and also applications from simple product identification to more complex applications such as environment sensing. In this paper, we propose and implement a small-size low-power digital logic design for a baseband RFID tag and baseband modem. We will demonstrate a potential solution for security problems in EPCglobal Gen2 protocol by using a novel block cipher designed for low-power and area-constrained devices to encrypt and transmit sensor data.**

Keywords—Implantable RFID tag; Baseband modem SoC; Mobile localization; EPCgrobal Generation2

I. INTRODUCTION

RFID (Radio Frequency Identification) technique is based on the exchange of information via wireless communication to read and utilize data stored in tag devices. RFID tag (trans-ponder) devices, in form of labels or cards, etc., is placed on each object, and the reader device acts as a master to exchange the information with tag devices that are within the possible effective communication range.

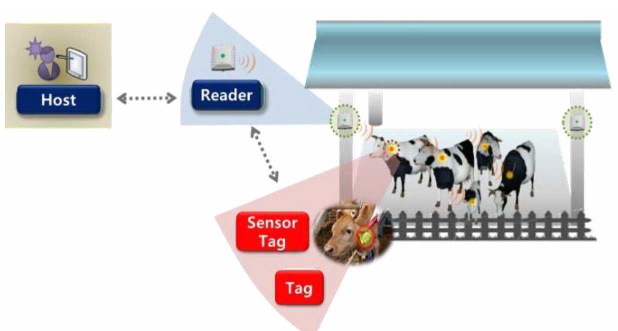


Fig. 1. The service diagram of full RFID system

Figure 1 shows the service diagram of the full RFID system that we propose in this paper. We implement an implantable RIFD tag that utilizes the standard 900 MHz RFID service profile to obtain basic information (ex. object number, position) and biometric information (ex. temperature, mating season) from sensors for the application in livestock management. We define the control methods and procedures of the RFID host and tag to obtain the basic and biometric information stored in the livestock.

II. IMPLEMENTATION OF THE DIGITAL MODELE

As shown in Figure 2, RFID sensor tag for livestock management used in this paper can be divided into three parts: RFID host, reader and tag. The sensor-tag system uses internal memory for storing sensor information for efficient memory management.

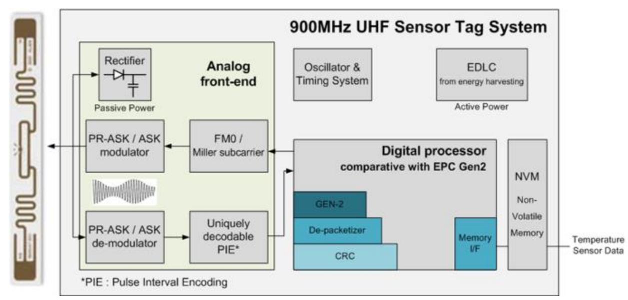


Fig. 2. The block diagram of components for 900MHz RFID tag

The RFID sensor-tag network consists of sensor-tags which collect biometric information, RFID readers that request and read the information of sensor-tags, and the RFID host that collects collected information from RFID readers.

The RFID host is the service providing apparatus that monitors information and data. A sensor-tag is a device composed of a tag that communicates with the reader, sensors that measure biological information, a memory in which the data is stored, and a memory controller which arbitrates the memory access between the tag and sensors.

As shown in Figure 3, digital back-end blocks of the RFID tag are defined as the Input Interface block, Tag Control block, Output Interface block.

First, the Input Interface block, which interprets the data supplied from the RF stage, is composed of blocks of PIE (Pulse Interval Encoding) Decoder, Command (CMD) Decoder, and CRC Decoder. PIE Decoder interprets the demodulated physical-layer incoming signal from the RF stage into a digital signal of data 0 or 1 by comparing the signal to the length of data-0 or Tari determined by the reader. CMD Decoder extracts the parameter values from the RFID reader commands.

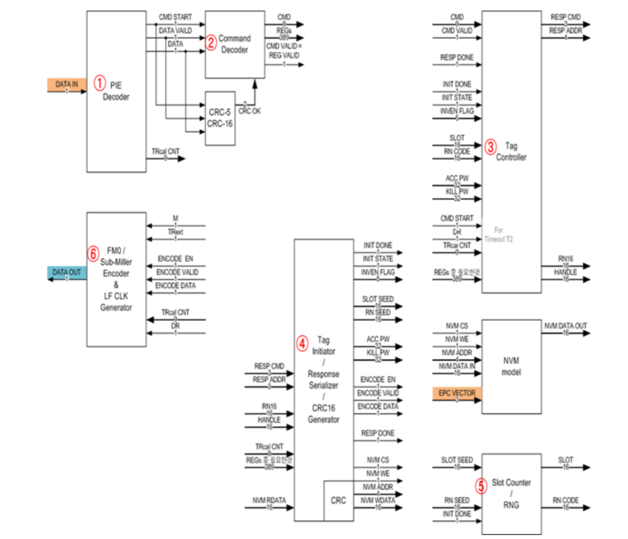
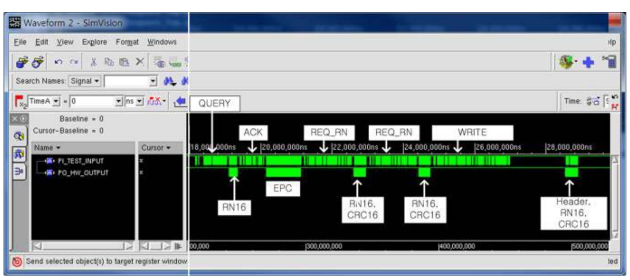


Fig. 3. Block diagram of the RFID digital module

Second, the Tag Control block is composed of Tag Initializer, Response Serializer, Slot Counter, and Tag Controller that control RFID tag operation and tag selection algorithm. Tag Controller controls the RFID tag operation including Tag Population Inventory Round. Tag Initializer initialize tag operation setting after power-up, and Response Serializer generates a serial communication data stream contained in the backscatter signal for the RFID reader.

Finally, the Output Interface block, which consists of FM0 Encoder, Miller Encoder, and Slot Counter, encrypts the outgoing data and delivers it to the RF/analog block. Tari is the period of the data-0 in range of 6.25us to 25us. Data transmission method used by the reader is the Pulse Interval Encoding and data rate is up to 160 Kbps ~ 200Kbps. The tag responds by the backscatter method of ASK or PSK modulation and uses the FM0 or Miller Subcarrier encoding method.

To measure the RFID tag communication signal, we use a FPGA-implemented RFID tag system, network analyzer and a commercial UHF RFID reader.



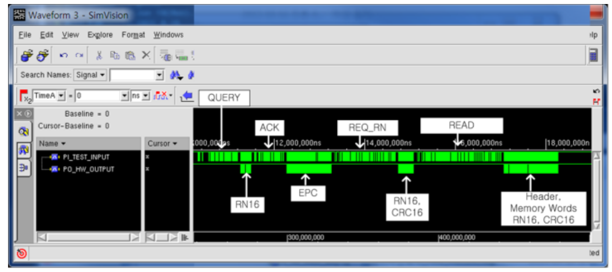


Fig. 4. Read and write command measure between the reader and the tag

We set up a test board RF, analog front end, and antenna for verifying the RFID tag digital backend. We control the RFID reader to send commands to the tag to transfer the data.

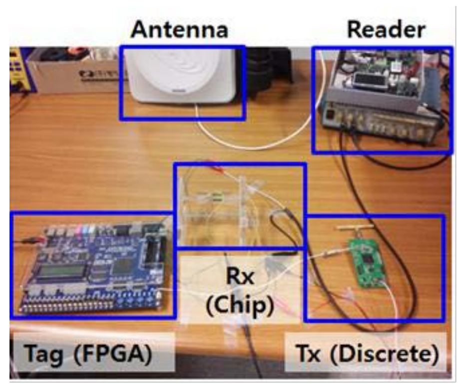


Fig. 5. Tag communication test equipment and server

III. Conclusion

In this paper, we designed a RFID tag digital block including the main baseband modem and multi-protocol algorithm block supporting the UHF band of ISO 18000-6B, EPC Class 1, EPC Class1 Gen2 standard. As a result, we are in the process of securing the primary IP of an implantable RFID digital tag. In future, the implantable RFID IP may be applied in various fields of miniaturized RFID Reader and tags.

Acknowledgment

This work was partly supported by the IT R&D program of MSIP/KEIT [10041749, Development of livestock traceability system using non-contact sensor tags].

References

[1] ISO/IEC FDIS 18000-6, Information technology

[2] 860MHz–930MHz EPC Class I Radio Frequency Identification Tag Radio Frequency & Logical Communication Interface Specification Candidate Recommendation, Version 1.0.1, AUTO-ID CENTER, 2002.

[3] EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz 960 MHz Version 1.0.9, EPCglobal, 2005.