A Low Power Fully CMOS Integrated RF Transceiver for Wireless Sensor Networks in Sub-GHz ISM-band

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Abstract: A fully CMOS integrated radio frequency (RF) transceiver for wireless sensor networks in sub-GHz ISM-band applications is implemented and measured. The IC is fabricated in 0.18-μm CMOS technology and packaged in LPCC package. The fully monolithic transceiver consists of a receiver, a transmitter and a RF synthesizer with on-chip VCO. The chip fully complies with the IEEE 802.15.4 WPAN standard in sub-GHz mode. The receiver sensitivity is –98dBm and the transmitter achieves less than 6.3% error vector magnitude (EVM) for 40kbps mode. The chip uses 1.8V power supply and the current consumption is 14mA for reception mode ad 16mA for transmission mode.

Index terms – wireless sensor network, integrated circuit, CMOS, RF transceiver, low power

1. Introduction

Recently, the desire for wireless connectivity has led an exponential growth in wireless communication. In particular, wireless sensor networks are potential wireless network application for the following future ubiquitous computing system. Wireless sensor networks are an emerging research area with potential applications in environmental monitoring, surveillance, military, health and security [1]. The power dissipation of wireless sensor networks does require low power consumption for several years' operation. In this paper we present the development of a fully single chip 0.18-μm CMOS RF transceiver targeted towards ubiquitous wireless sensor networks in sub-GHz ISM-band applications.

2. Radio System Implementation

The communication nodes are required to integrate with one die for low power and low cost wireless sensor network applications. With first step, we did implement RF transceiver chip including an ADC and a DAC. Fig.1 shows the architecture of a radio chip, which consists of a receiver, a transmitter, and a frequency synthesizer with on-chip VCO.

2.1 RF transceiver architecture and design

The receiver adopts zero-IF architecture [2], [3] to have low power consumption, low cost and small size. The sub-GHz RF signal is first amplified by a low noise amplifier (LNA) and then down-converted to zero-IF I/Q signals by two identical mixers driven by quadrature local-oscillator (LO) signals from a frequency synthesizer. At the analog baseband stage, using a third-order RC filter and programmable gain amplifier. The transmitter adopts a general zero-IF modulation with up-conversion mixer. Baseband BPSK signals generated by digital modulator in MODEM block are followed a 6-bit DAC. A mixer up-converts the baseband signal directly 900-MHz, which is combined by RC low-pass filter. Since BPSK modulation is a constant envelop modulation, a nonlinear power amplifier with high efficiency can be used For generating 900-MHz LO signals with 2-MHz channel spacing, an integer-N frequency synthesizer derived from a 30-MHz crystal oscillator with 30ppm accuracy is implemented. A 1.8GHz LO signal is generated by a voltage-controlled oscillator (VCO) with a small area and high Q on-chip inductor. The 900-MHz LO I/Q signals are then generated by a divide-by-two circuit. The frequency synthesizer is implemented in fully differential type, for immunity to common mode noise.

2.2 Mesured results

A radio transceiver die microphotograph, which consists of transmitter, receiver, and frequency synthesizer with on-chip VCO, is shown in Fig. 2. The total die area is 1.6*2.4mm2 and it consumes only 29mW in the transmit-mode and 25mW in the receive-mode, and a LPCC48 package is used. The 300-KHz baseband single signal is up-converted by 906-MHz RF carrier signal and wanted-signals are above 25-dBc than third-order harmonics. The spectrum at the output of transmitter satisfies the required spectrum mask as shown in Fig. 3, which is above 28-dBc at the ±1.2-MHz offset frequency. As shown in Fig.4, a reference design achieves 6.3% EVM for an output power of –3dBm for sub-GHz ISM-band. The output P1-dB of transmitter is +1dBm. The receiver features an NF of 9 dB for 900-MHz band and achives –98dBm sensitivity at the input of chip for the IEEE 802.15.4 BPSK mode [4]. Receive IIP3 is –7dBm and the maximum gain of receiver is 88dB. The automatic gain control (AGC) of receiver is 86dB with 1dB step and selectivity is − 48dBc at 5-MHz offset frequency. As shown in Fig.5, the in band phase noise of frequency synthesizer is –75dBc/Hz and phase noise of VCO is –108dBc at 1-MHz offset frequency. The Table I show the simulated and measured results of radio transceiver.

References

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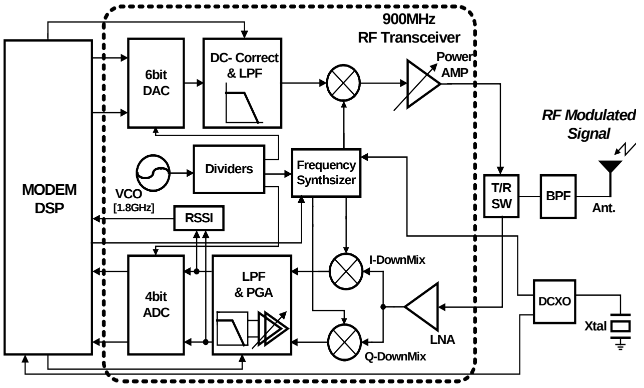

Fig.1 RF transceiver block diagram supporting wireless sensor networks in sub-GHz ISM-band.

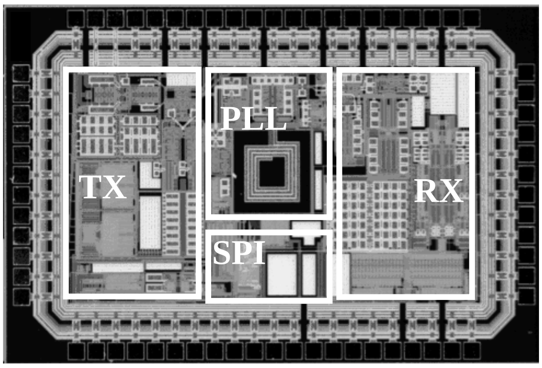

Fig.2 Die microphotograph

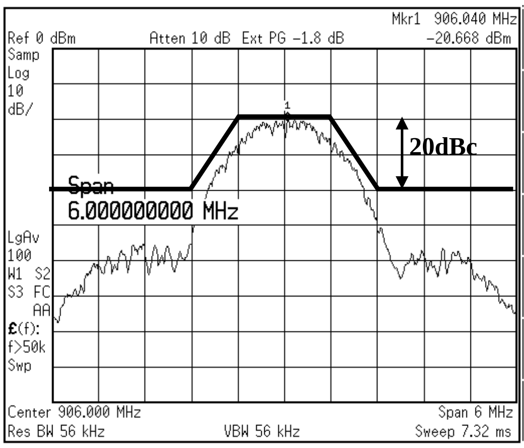

Fig.3 Transmitter output spectrum mask

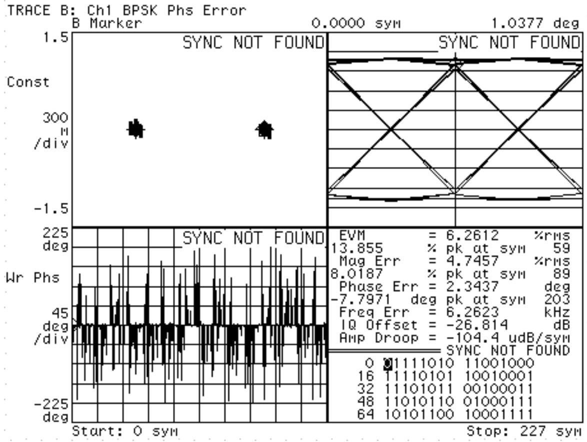

Fig.4 Transmitter output error vector magnitude (EVM)

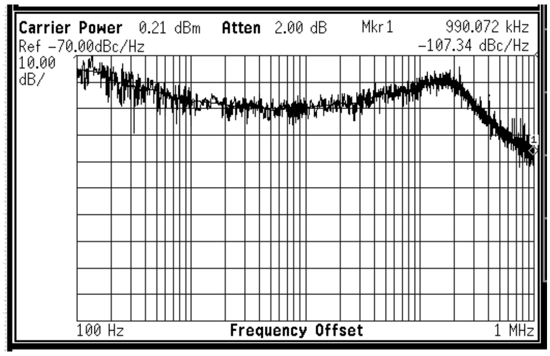

Fig.5 Frequency synthesizer: phase noise

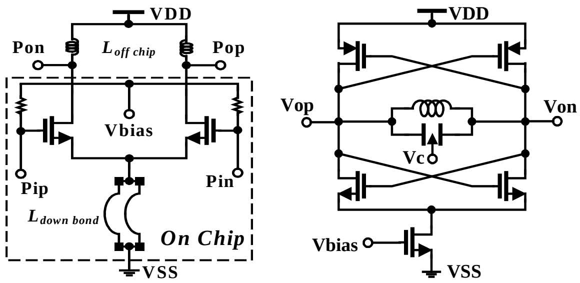

Fig.6 Power amplifier with off-chip inductor and LC-VCO

TABLE I
THE MEASURED RESULTS OF RF TRANSCEIVER

Specification	Simulated	Measured
VDD	1.8V	1.8V
DC current consumption	Rx./Tx.:14/15mA	Rx./Tx.:14/16mA
Die size	1.6*2.4mm^2 (containing PAD)	
NF/Sensitivity	8dB/-99dBm	9dB/-98dBm
IIP3	-5dBm	-7dBm
Max. gain	90dB	88dB
AGC gain range	86	86
Selectivity	-50dBc(@5MHz)	-48dBc(@5MHz)
TX power	+3dBm	0dBm
EVM	-	6.3%
P1-dB (output)	+4dBm	+1dBm
LO phase noise	-110dBc(@1MHz)	-1080dBc(@1MHz)