CMOS

,   ,   ,   ,   ,   ,   ,   ,
,
Tel: +82-31-789-7514, Fax: +82-31-789-7519
E-mail: ykmoon@keti.re.kr

Design of a CMOS Analog Front End for a WPAN Receiver

Yeon Kug Moon, Hae-Moon Seo, Yong-Kuk Park, Seung Ok Lim, Kwang-Ho Won, Myung-Hyun Yoon,
June-Jae Yoo, Myung Soo Lee, and Seong-Dong Kim
Ubiquitous Computing Research Center, Korea Electronics Technology Institute (KETI)

Abstract

This paper describes a low-voltage and low-power channel selection analog front end with continuous-time low pass filters and highly linear programmable-gain amplifier(PGA). The filters were realized as balanced Gm-C biquadratic filters to achieve a low current consumption. High linearity and a constant wide bandwidth are achieved by using a new transconductance(Gm) cell. The PGA has a voltage gain varying from 0 to 65dB, while maintaining a constant bandwidth. A filter tuning circuit that requires an accurate time base but no external components is presented. With a 1-Vrms differential input and output, the filter achieves -85dB THD and a 78dB signal-to-noise ratio. Both the filter and PGA were implemented in a 0.18um 1P6M n-well CMOS process. They consume 3.2mW from a 1.8V power supply and occupy an area of 0.19mm^2.

Index terms – Channel selection filters, DC offset, programmable gain amplifier, tuning circuit

I. Introduction

The demand for low-cost, low-power wireless tranceivers operating in the Wireless Personal Area Network(WPAN) has led to extensive research on RF circuit design[1][2]. Particularly, since one of the characteristics of such a WPAN transceiver is that it has a wider channel spacing than the bandwith of a channel has[3], its filter attenuation requirement is lower than other wireless communication specifications[4][5][6][7]. Thus, it is possible to use a filter of a lower order, and this will lead to a lower power dissipation and cost. This paper suggests that the Analog Front End in transceiver is relevant to this WPAN.

II. Analog Front End Design

Figure 1 shows the Analog Front End (AFE) of a realized WPAN receiver. The third order Butterworth filter was implemented cascading a biquad cell and a single pole cell, and the programmable gain cell was stationed at the middle to improve the cascaded dynamic range. The AFE design is concentrated on optimizing the dynamic range and keeping the required die area small and low power consumption. The baseband noise is dominated by the thermal noise of the

PMOS current sources at the Mixer output. The flicker noise is not a significant problem at baseband since all transistors are designed for a long channel length for better matching. And the output of the DAC is DC blocked using a Modem control signal to minimize the effect of the internal DC offsets from limiting the dynamic range of the receiver.
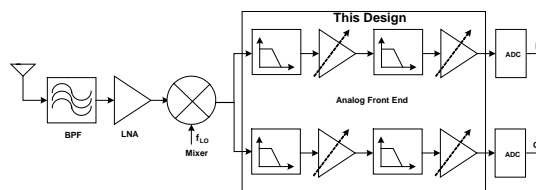

Fig. 1. Block diagram of the analog front end

2.1 Channel Selection Filter

The Channel filter allows a signal of the desired band to pass, and attenuates the adjacent channel and the alternate channel. The filter requirement in this paper is as follows. Since it is a DCR structure, 1/f noise should be reduced and the DC offset should be small. And in order to alleviate the SFDR requirements of the PGA and the ADC, most of the interference is filtered in the

first part. Figure 2 shows the designed third Butterworth LPF. Using the single pole of the passive RC at the output stage of the Mixer reduces the interference whose cannot affect the dynamic range at the baseband input stage, and using the overshoot of biquad compensates the in-band loss. Figure 3(a) shows the proposed Gm-cell with degeneration resistor. Two Gm-cells are
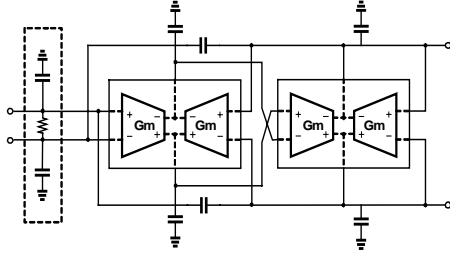

Fig. 2. The designed third order Butterworth LPF

used as one to reduce the area that LPF occupies, as shown in Figure 3(b). the lumped resistor and the size of MOS should be properly adjusted to improve the linearity of the Gm-cell.
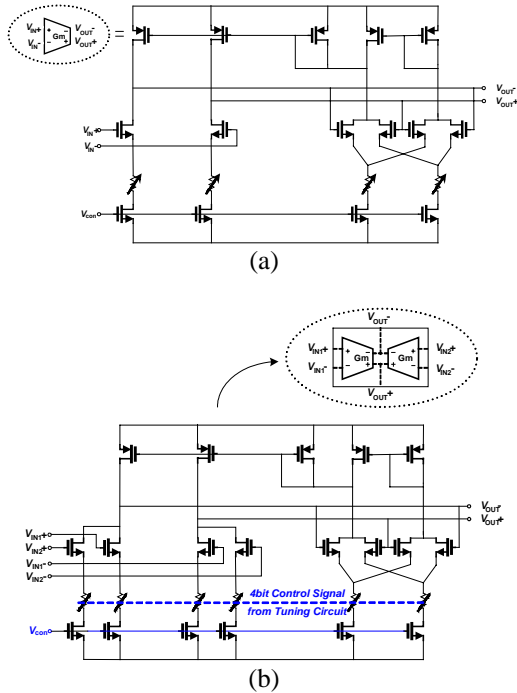

(a)

(b)

Fig. 3. Circuit Diagram of (a) the Proposed Transconductance Cell (b) Realization of the Transconductance Cell

2.2 Programmable-Gain Amplifier

The signal level of the RF input requires a minimum dynamic range of 72dB, namely from -92dBm to -20dBm. The AGC control signal receives the digital control signal from the Modem to control the gain of the receiver. Figure 4 shows the circuit of the PGA, and the PGA of this receiver utilizes the three gain stages to control the gain of 0 ~ 65dB with a 1 dB step. The resistor switching method was utilized in order to not lose the linearity of PGA.
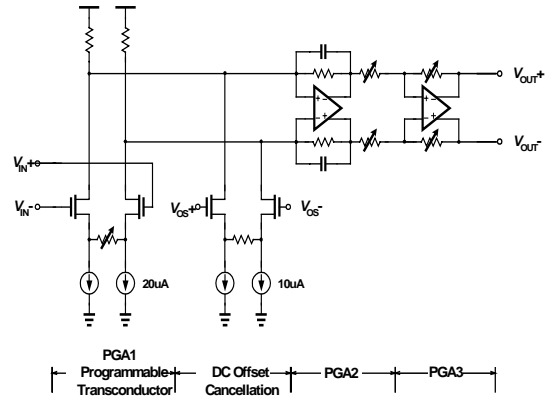

Fig. 4. Circuit schematic of the PGA

2.3 Filter Tuning Circuit

Figure 5 shows the proposed automatic-tuning circuit, which is based on indirect tuning method. Since the filter characteristics of the Gm-C filter are determined by the gm value, the gm has to be controlled to keep a fixed pole frequency. And since the gm value should not be changed even by process variation or outer environment changes, here, as shown in Figure 5, it is important to keep a gm value and a ratio of gm output current to gm input voltage with equal, and the required current for sinking or sourcing is designed to minimize changes of gm by minimizing current change due to the temperature variation from bias block.
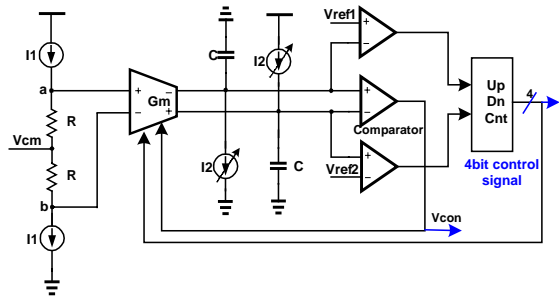

Fig. 5. Tuning Circuit

Current I1 in Figure 5 offsets the MOS of the bias part as well as the temperature variation of resistance so as to minimize the changes of voltage V_{ab} due to the temperature and to evenly

maintain the input voltage of the gm-cell. The converging time of tuning circuit is designed to less than 100usec. If the cut-off frequency differs from the designed value as a parameter set up the first time it distorts the value of gm by the process variations, gm should be adjusted by changing current I2 by fusing. Fusing is controlled by serial port interface (SPI), and there is no change in value once it is put in. Figure 6 is the circuit diagram of fusing cell.
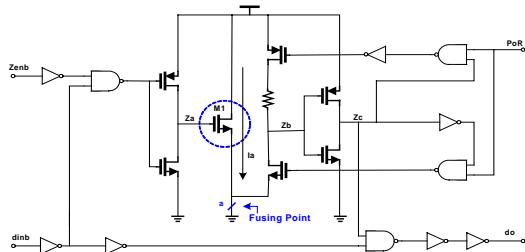

Fig. 6. The circuit schematic of fusing cell

The fusing cell is a circuit which amplifies the voltage, which is set in ratio of PMOS channel resistance to NMOS channel resistance within the range of power on reset ('Low' PoR signal) at power-on, to inverting amp, latches the signal and displays the latched value without change while normal operation ('High' PoR signal). 'Zenb' here is a signal of 'fusing enable', 'dinb' is a 'data input signal' controllable via SPI. 'PoR' is a signal for 'enable' at the mode of 'power on reset', while 'do' is an output signal of fusing cell. Once the fusing signal turns to 'enable', the output signal of fusing cell is fixed regardless the data input signal. The current capacity of M1 should have more than 1mA in order to disconnect the node a of fusing point, at transmitting the fusing enable signal.

2.4 DC Offset Adjustment

For DC offset adjustment, 8-bit digital data for I/Q from the Modem are input to control the DC offset at the back side of PGA1 to use the feedback loop to reduce the offset at the LPF output. Figure 7 shows the DAC to convert the 8-bit data into the input voltage of the PGA.
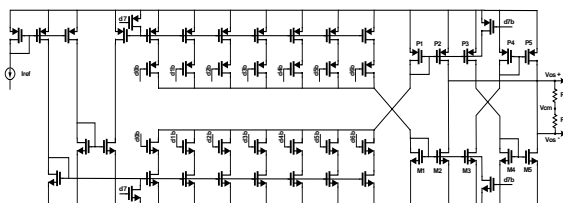

Fig. 7. DAC for DC offset adjustment

The resolution for 1 bit is 5mV, and the DC offset change at the LPF output is ±640mV. The size of MOS (P1~P5, M1~M5) used as a current mirror of the DAC circuit has to be appropriate in consideration of the current mismatch. The aspect ratio of the MOS is used by 20u/2u.

III. Measurement Results

The chip photograph of the proposed Analog Front End is shown in Figure 8, and the active chip area excluding pads is 0.19mm^2.
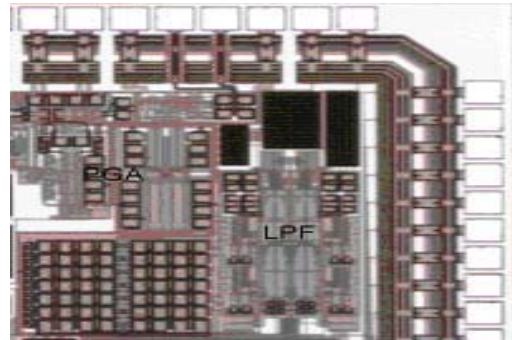

Fig. 8. Chip photograph

Figure 9 shows the in-band, third-order intercept point of the Analog Front End. A two-tone signal of the same power was applied by RF input, and the powers of the fundamental signal and IM3 element were measured as gradually increasing the power of the input signal. V_{IIP3} is about 6 V_{rms}. The designed gm of biquad has excellent linearity compared with the other structures as it determined by lumped resistor. In gain block used PGA, the gain is valued by the lumped resistor determined by degeneration and the lumped resistor in type of active RC, which ensures the linearity superior to the other structures using active devices.
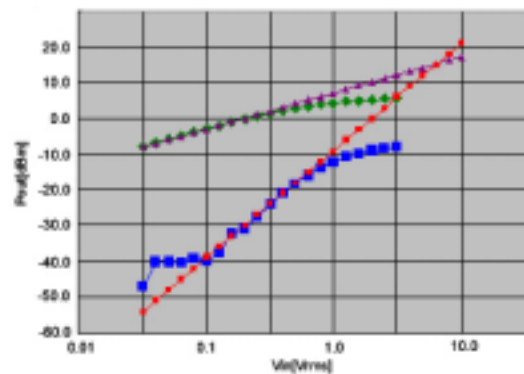

Fig. 9. The third-order intercept point of the AFE

Figure 10 shows the filter characteristic of the LPF, and Figure 11 shows the PGA output spectrum after applying the signal of -65dBm by RF input and setting the PGA Gain to 39dB.
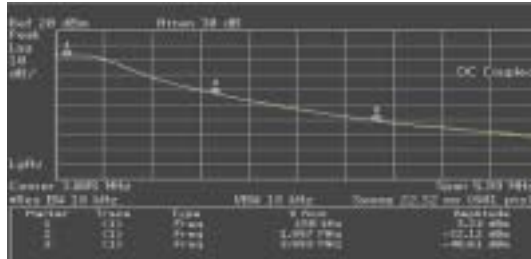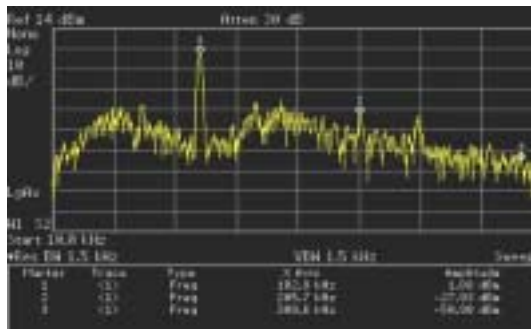

Fig. 10. The mask characteristics of LPF

Fig. 11. PGA output spectrum

With a 1-Vrms differential input and output, the filter achieves -85dB THD and a 78dB signal-to-noise ratio. The measured cutoff frequency varied from 900kHz to 2MHz, which is very close to the simulated range(850kHz to 2.1MHz). The passband flatness is measured below 0.2dB and The group delay time is 62nsec. Table 1 shows the related output characteristics of AFE.

Table 1. Summary of measured Results

Power Supply	1.8V
Technology	0.18u CMOS
Chip Area	0.19mm^2
Power Dissipation	3.2mW
-3dB Bandwidth	900kHz to 2MHz
-3dB Variation	$< \pm 1\%$
Group Delay	62nsec
VGA gain	0 ~ 65dB
V_{IIP3}	6 V_{rms}
THD	-85dB

IV. Conclusions

A fully CMOS integrated channel selection analog front end with continuous-time low pass filters and highly linear programmable-gain amplifier is implemented and measured. The IC is fabricated in 0.18-µm CMOS technology and packaged in a LPCC package. The analog front end can be utilized to reduce power consumption in applications demanding high linearity and low supply-voltage operation. DC offset cancellation is essential in a ZIF receiver, and this must be able to handle gain-dependent errors as well as static components. The tuning circuits are shown to converge to the design target after the chip is powered on.

References

[1] Pilsoon Choi et.al, "An Experimental Coin-Sized Radio for Extremely Low-Power WPAN Application at 2.4GHz," IEEE J. Solid-State Circuits, vol. 38, no.12, pp. 2258~2268, Dec. 2003

[2] C. Cojocaru et.al, "A 43mW Bluetooth transceiver with –91dBm sensitivity," ISSCC Dig. Tech. Papers, pp. 90~91, Feb. 2003.

[3] IEEE Computer Society, "IEEE Standard for Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low Rate Wireless Personal Area Networks (LR-WPANs)", IEEE Std 802.15.4TM-2003.

[4] Mario Valla et.al, "A 72-mW CMOS 802.11a Direct Conversion Front-End With 3.5-dB NF and 200-kHz 1/f Noise Corner," IEEE J. Solid-State Circuits, vol. 40, no.4, pp. 970~977, April 2005

[5] Angelika Schneider et.al, "Nonlinear Analysis of Noise in Current-Steering Variable Gain Amplifiers," IEEE J. Solid-State Circuits, vol. 39, no.2, pp. 290~296, Feb. 2004

[6] Jose Silva-Martinez et.al, "A 10.7-MHz 68-dB SNR CMOS Continuous-Time Filter with On-Chip Automatic Tunig," IEEE J. Solid-State Circuits, vol. 27, no.12, pp.1843~1853, Dec. 1992

[7] Yorgos palaskas et.al, "A "Divide and Conquer" Technique for Implementing Wide Dynamic Range Continuous-Time Filters," IEEE J. Solid-State Circuits, vol. 39, no.2, pp.297~307, Feb. 2004