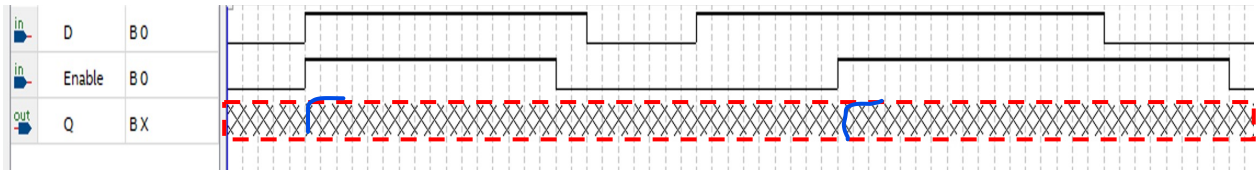
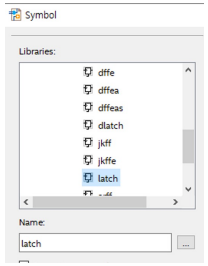
실습 1

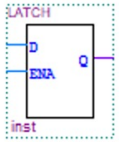
다음 회로의 동작을 확인하시오

1. Quartus로 Clock의 주기에 따른 D flip-flop과 Latch 의 Qout의 출력을 확인하시오

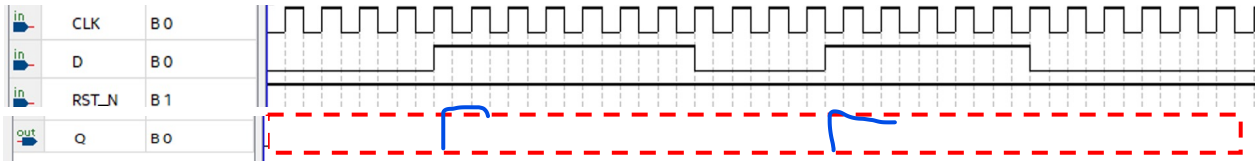
① Latch (Asynchronous) 동작 결과를 보고 그 이유를 간단하게 서술하시오

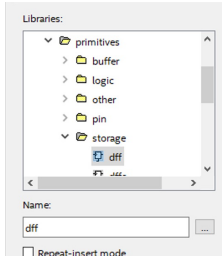






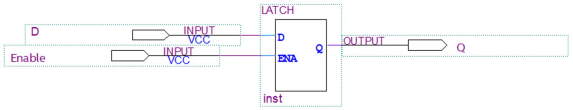
② D Flip-Flop (Synchronous) 동작 결과를 보고 그 이유를 간단하게 서술하시오



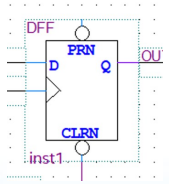


Schematic에서 A 클릭하면 글씨 써집니다 영어로

write in 1~2 line why the Q output comes out like this.

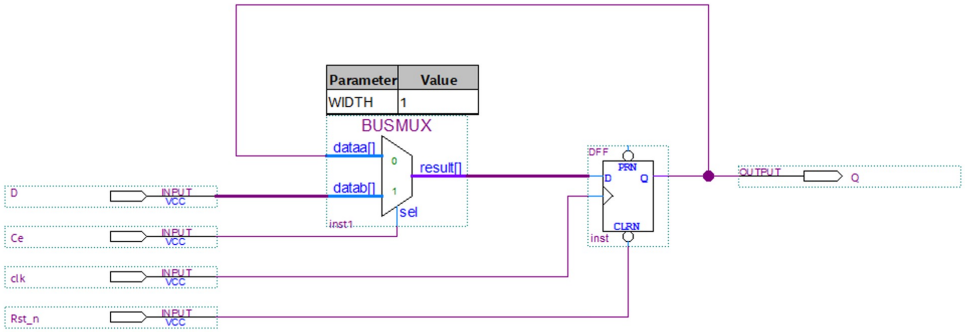


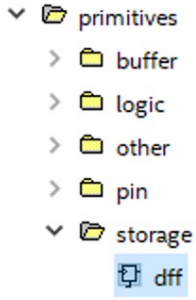
예시



실습 2

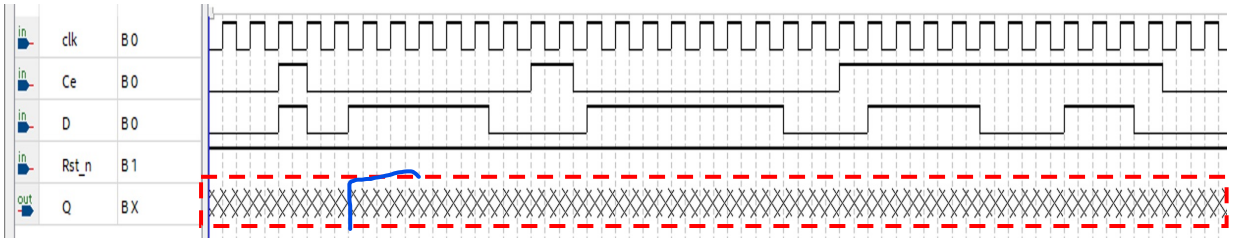
다음 회로의 동작을 확인하시오.

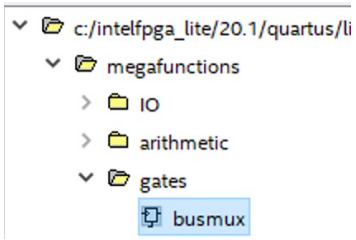




D Flip-Flop schematic

① Clock Synchronous

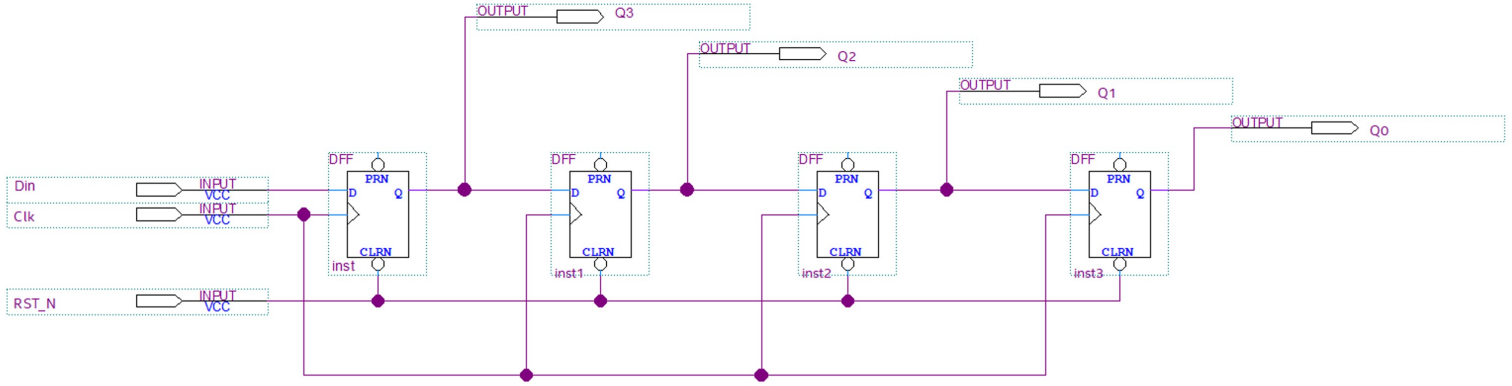




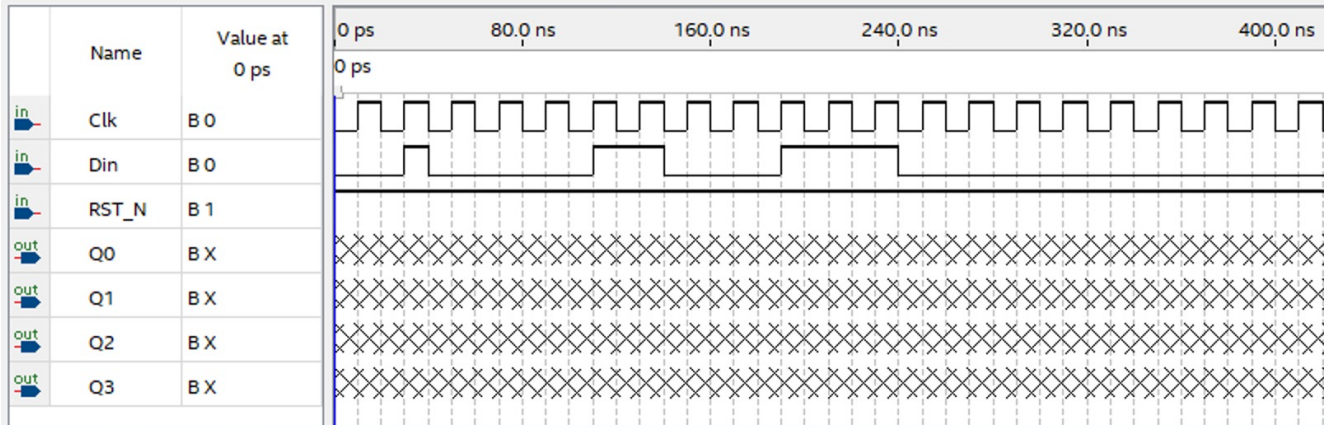
Mux schematic

실습 3

다음 회로의 동작을 확인하시오 (shift register)



① Clock Synchronous

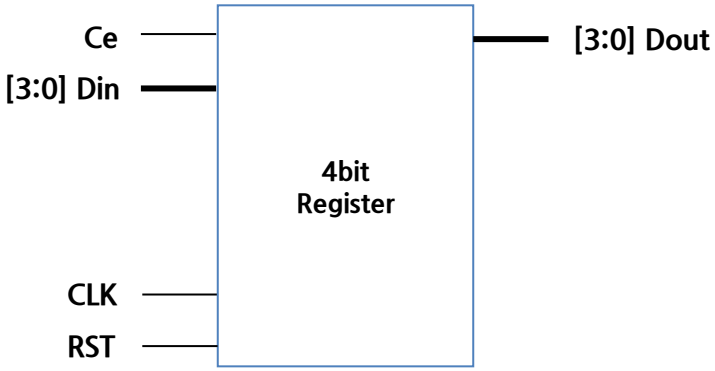


실습 4

아래 기능을 만족하는 4bit Register를 구현하시오

입력 : Ce, [3:0] Din, CLK, RST
출력 : [3:0] Dout

Ce가 0이면 현재 값을 유지하고,
Ce가 1이면 [3:0] Din의 값으로 초기화되는 4bit Register

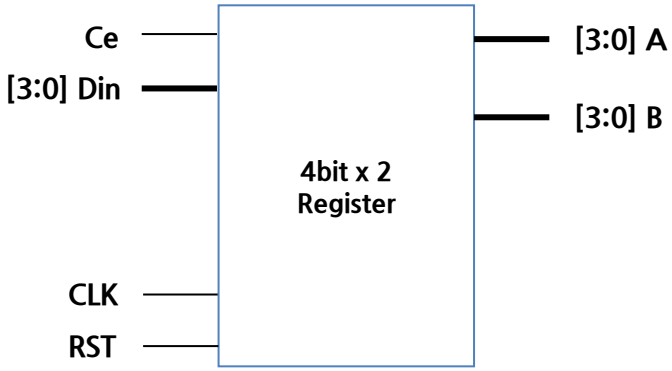


실습 5

아래 기능을 만족하는 4bit x 2 Shift Register를 구현하시오

입력 : Ce, [3:0] Din, CLK, RST
출력 : [3:0] A, [3:0] B

Ce가 0이면 현재 값(Dout)을 유지하고,
Ce가 1이면 [3:0] Din의 값이 Shift 되는 4bit Register
B는 첫번째 레지스터의 출력 값(중간 값)
A는 두번째 레지스터의 출력 값(Shift Register의 결과 값)

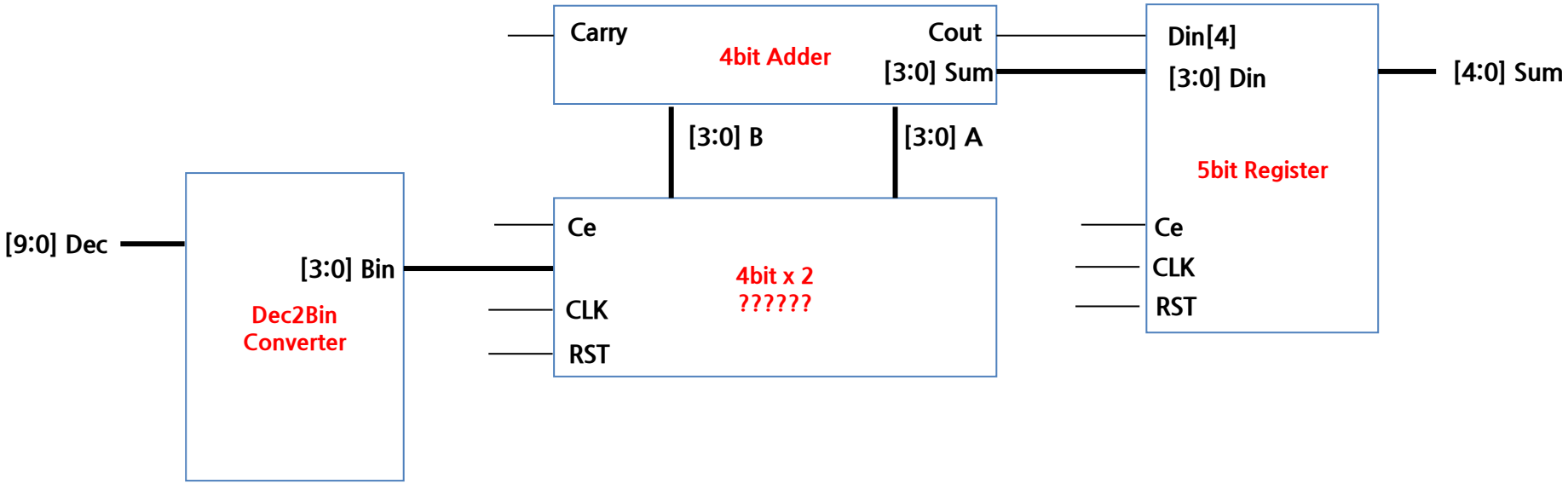


실습 6

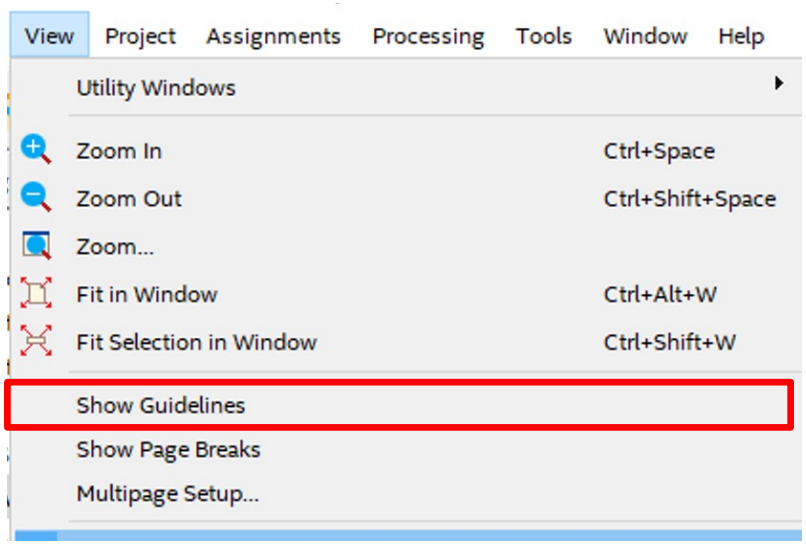
아래 기능을 만족하는 회로를 완성하고 동작을 확인하시오

입력 : [9:0] Dec, CLK, RST, CE, Carry
출력 : [4:0] SUM

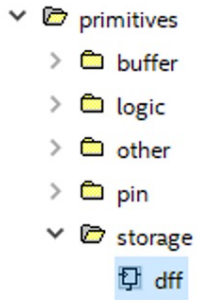
0~9에 해당하는 Dec 값을 2번 입력하면 해당 값을 더해서 저장하는 회로



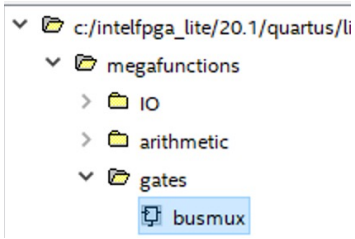
참고사항



실선 없어집니다.

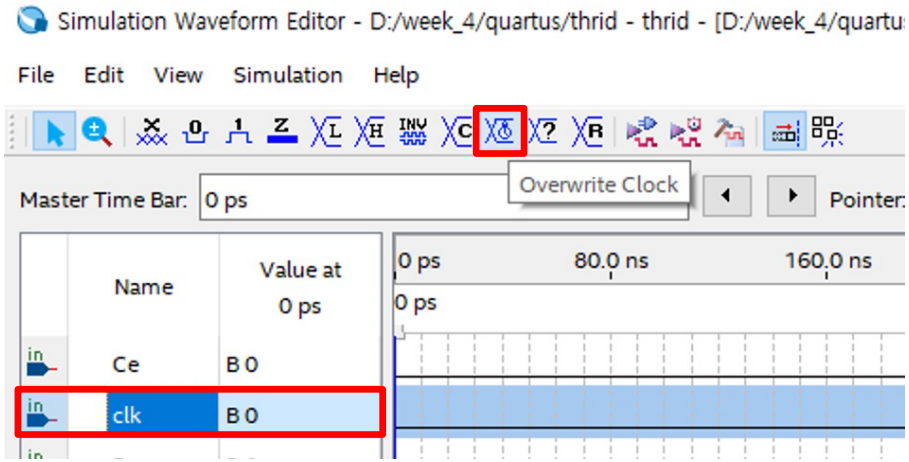


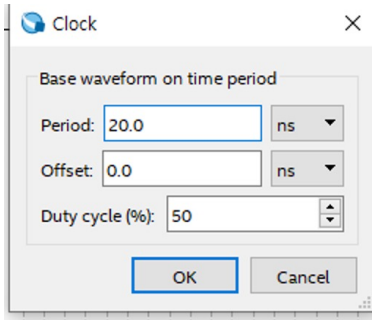
D Flip-Flop schematic

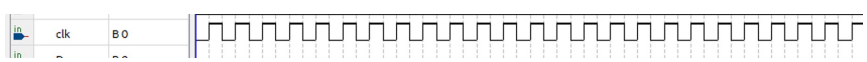


Mux schematic

Clock 주기 주는 방법

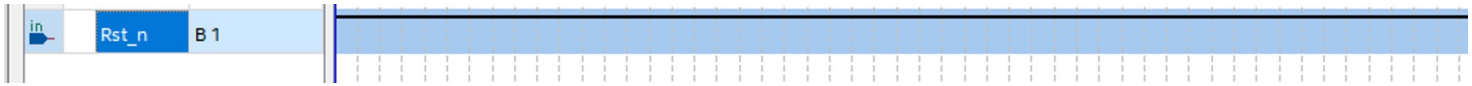






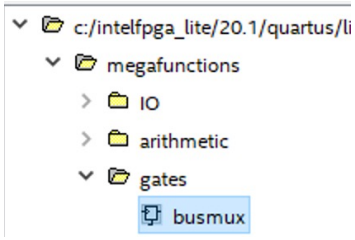
Appendix(2)

주의사항 : DFF 사용시에 CLRN(clear negative)의 신호 입력을
항상 1로 해야 데이터를 받음

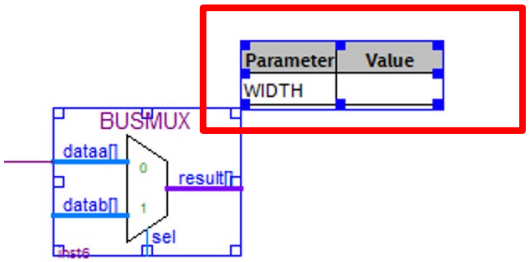


Appendix(2)

Quartus BUSMUX

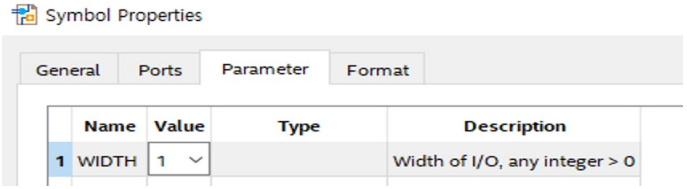


Mux schematic



더블 클릭

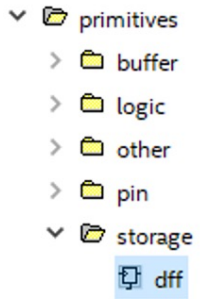
Symbol Properties



위와 같이 설정시 2x1 mux 사용 가능

Appendix(3)

Quartus D Flip Flop



D Flip-Flop schematic