R06921048　李友岐

2.

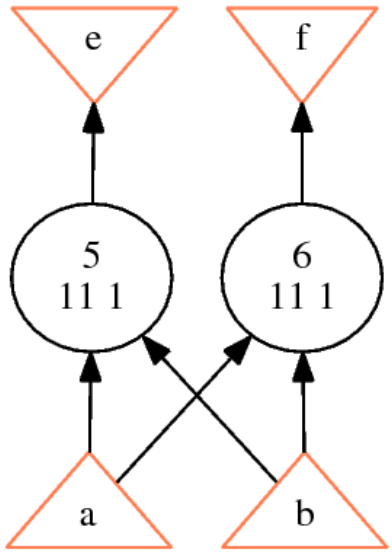
(a)

(1)

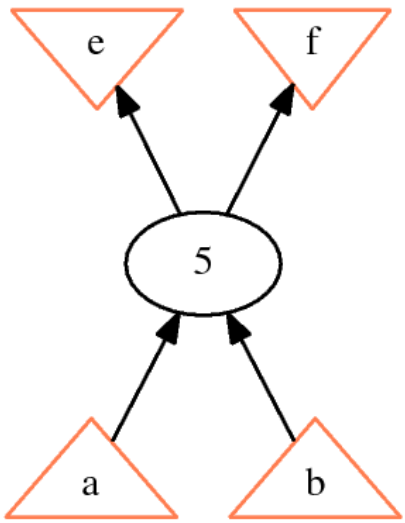
Given an example of two output e and f, let e=a*b and f=b*a. If we use command “aig”, then e and f will be viewed as two different nodes. By contrast, if we use command “strash”, then e and f will be viewed as the same node.

```
.model test
.inputs a b
.outputs e f
.names a b e
11 1


.names b a f
11 1

.end
```

aig:



strash:

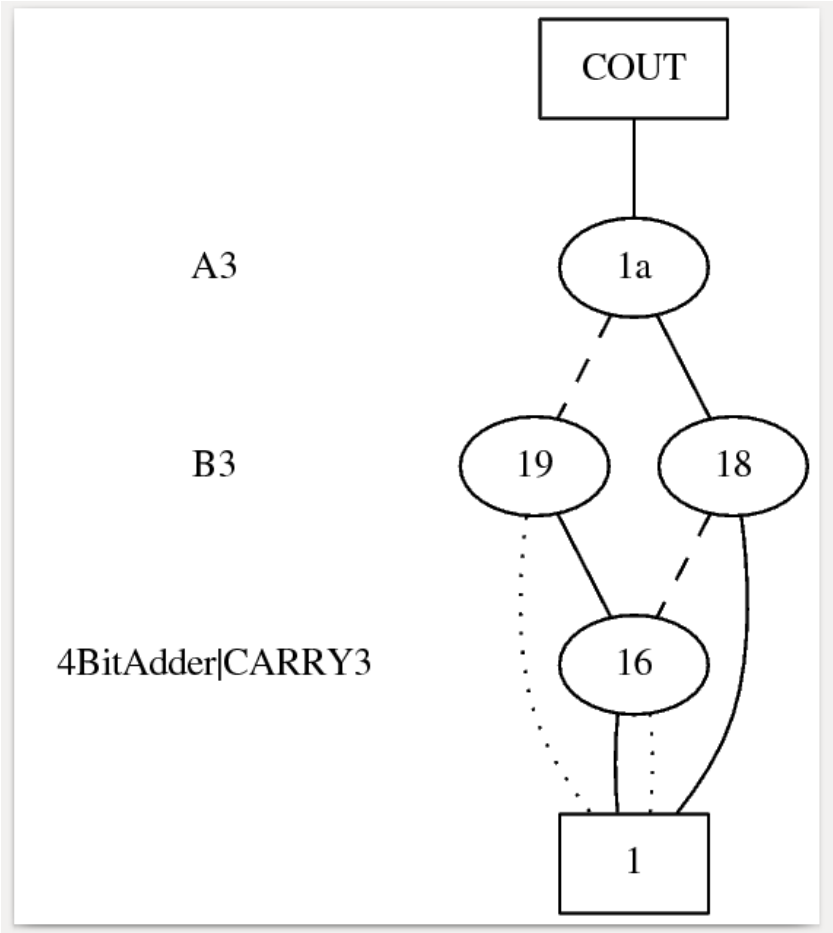


(2)

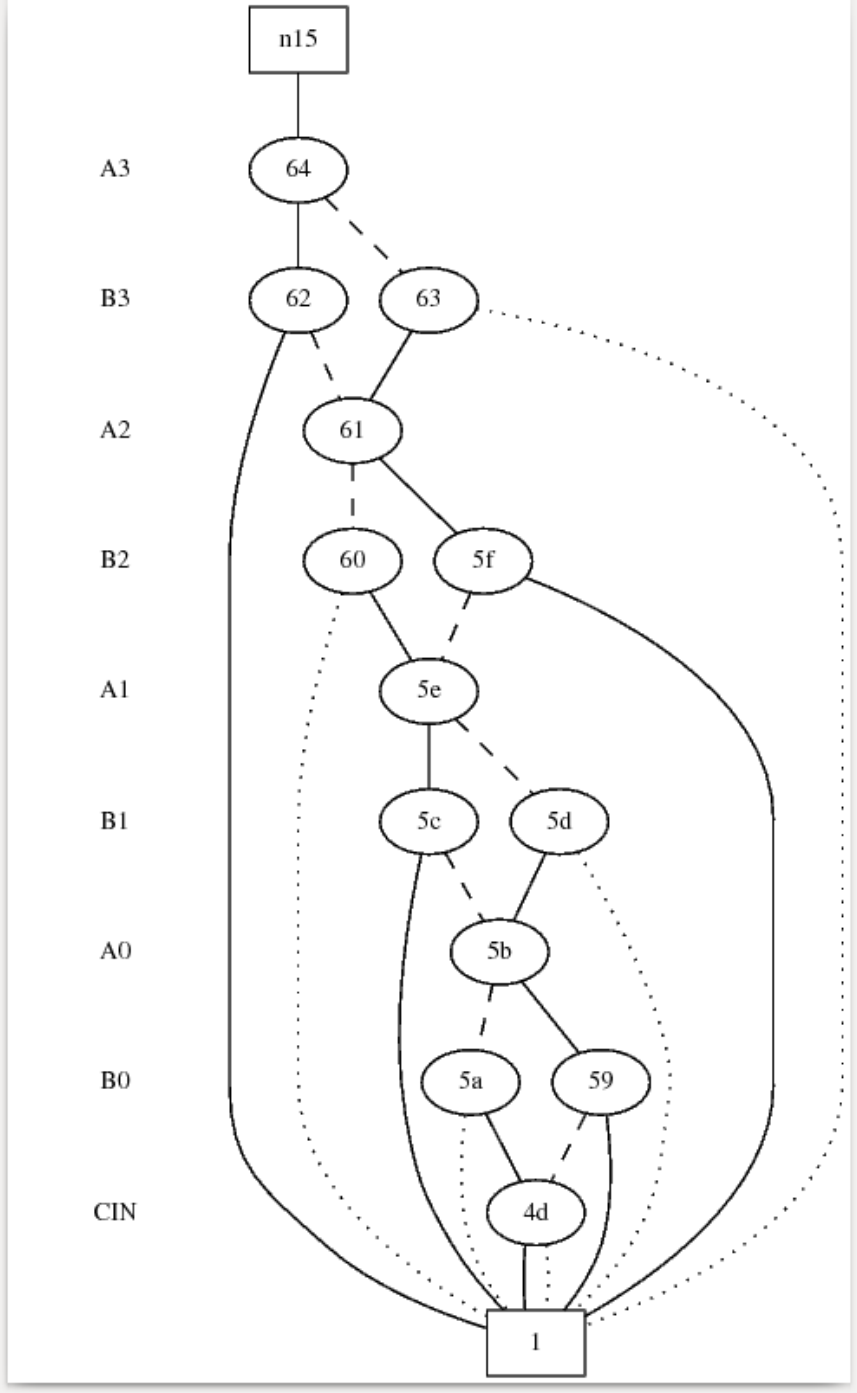
Take the 4 bit adder circuit (4BitAdder.blif) as example. Consider the output COUT. For the whole cirucit, the inputs of COUT are A3, A2, A1, A0, B3, B2, B1, B0, CIN. However, for the subcircuit full adder, the inputs of COUT are A3, B3, CARRY3. The command “bdd” produces the latter, while the command “collapse” produces the former.

```
.model 4BitAdder
.inputs A3 A2 A1 A0 B3 B2 B1 B0 CIN
.outputs COUT S3 S2 S1 S0
.subckt fulladder a=A0 b=B0 cin=CIN s=S0 cout=CARRY1
.subckt fulladder a=A1 b=B1 cin=CARRY1 s=S1 cout=CARRY2
.subckt fulladder a=A2 b=B2 cin=CARRY2 s=S2 cout=CARRY3
.subckt fulladder a=A3 b=B3 cin=CARRY3 s=S3 cout=COUT
.end

.model fulladder
.inputs a b cin
.outputs s cout
.names a b k
10 1
01 1
.names k cin s
10 1
01 1
.names a b cin cout
11- 1
1-1 1
-11 1
.end
```

bdd:



collapse:



2.
(b)
We can simply use the command “renode” to accomplish the requirement. It will convert a structurally hashed AIG(strash) to a logic network in SOP.