

系統晶片驗證 (SoC Verification)

105 學年下學期 電機系電子所選修課程 943 U0250

Homework #1 [Getting Familiar with V3 Framework]

(Due: 9:00pm, Thursday, March 23, 2017)

[Objectives]

1. Getting familiar with the verification framework “V3” (developed by Design Verification Lab in NTU).
2. Writing monitors (assertions) and performing simulation-based verification on a provided RTL design.

[Problems]

1. Please refer to “V3_readme” in the homework directory to download and install the V3 framework, or simply execute “install.sh”. Describe the environment of your workstation, capture the screenshot of your successful compilation, and put the description and screenshot in a file “*hw1.1.{txt,doc,pdf}*” under the “reports” directory.
2. Go through the “Read and Write Designs” tutorial in Chapter 1 of “tutorials/V3_tutorial.pdf” and repeat it for the “vending.v” design under the “vending-simple” directory. In essence, do the following:
 - (a) Read the spec of the design “SPEC-vending machine.pdf” to understand architecture and design of the vending machine.
 - (b) Read in the original RTL design and write it out into “rtl”, “btor”, and “aig” formats. Name them as “vending-rtl.v”, “vending.btor”, and “vending.aig” and put them in the same (i.e. “vending-simple”) directory.
 - (c) Report the network statistics by the command “`print ntk -verbose`” for the three output designs in (a). Put the output message into a file “*hw1.2c.{txt,doc,pdf}*” under the “reports” directory.
 - (d) Plot the “rtl” and “aig” networks by the command “`plot ntk -level k -png`”. Choose the proper “k” value so that the entire network can be plotted. Name the output files “*plot.vending-rtl.png*” and “*plot.vending-aig.png*” and put them in the “reports” directory.

3. Go through the “*Design Simulation*” tutorial in Chapter 2 of “tutorials/V3_tutorial.pdf”. Please note that the vending machine design inside this tutorial is the original (more complicated) one. In this problem, you are asked to perform simulation for the simplified one (i.e. “*vending.v*” under the “*vending-simple*” directory).

Please note there is at least one bug in the design and the monitor “*p*” in line 112 is enough to reveal it. This monitor signifies the bug that when there is no transaction or the transaction fails (e.g. not enough changes), the output changes are NOT equal to the input changes. The input pattern file “*input.pattern*” is for your reference. You should try to generate more test patterns to reveal the bug and figure out the cause(s). Please refer to Appendix B of V3’s tutorial for the format of the simulation pattern, and please pay attention to the order of the input variables in the pattern file.

Create a subdirectory “*debug*” under the “*vending-simple*” directory, and put your input pattern file(s) and output log(s) in it. You should also include a file “*hw1.3.{txt,doc,pdf}*” to describe how you find the bug and fix it.

4. Save the rectified design as “*vending-fixed.v*” in the “*vending-simple*” directory. In order to verify the design, you should write more “monitors” to guard the potential bugs and generate more patterns to check if any of the monitors can be triggered. If another bug is found, you need to debug. Note that sometimes it is not a bug in the design, but a bug in the monitors you write. Repeat this process (i.e. writing more monitors and creating more patterns) until you think the verification quality is good enough.

Since the manual pattern creation process is very tedious, you are encouraged to write some “driver” program to automatically generate legal patterns for simulation.

Put your input pattern file(s) and output log(s) in the subdirectory “*verify*” under “*vending-simple*”. You should also write a report “*hw1.4.{txt,doc,pdf}*” in the same directory to describe: (1) your monitors and how sound you think they can guard the design, and (2) the test patterns and their verification results.

[Submission of homework]

Please name the files and place them in directories properly or as suggested by the problem description above. Rename the root directory “*hw1*” as “*hw1_yourStudentID*” and compress it (MUST be under Linux/OSX workstation) by the command:

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“tar zcvf hw1_yourStudentID.tgz hw1_yourStudentID”.
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Submit the .tgz file only. Failure to abide by the above rules may result in deduction of your HW grade.