Computer-Aided VLSI System Design

HW4 - DFT/ATPG

Due in: 12:00 5/15/2018 (Tue)

助教聯絡方式：
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Purpose

In this homework, you have to perform DFT insertion to the synthesized *Frequency Analysis System* gate-level netlist (HW2). You also have to generate test patterns by using TetraMAX® ATPG.

Goal

Learn how to insert scan chain which is based on your design and generate the test patterns

Problem 1: Perform DFT insertion

1. Perform DFT insertion with **X scan chains** and fix any DRC violation.
2. Save the dft insertion results.
3. Modify the testbench and verify the dft inserted design. Make sure your dft inserted design still work in functional mode.

Hint:

***Scan chain number is based on your design's DFF number. We usually link 100 DFF with one scan chain.**

***You can follow the step on Lab4 but sometimes you may need to modify some parameters (that all based on your design).**

Problem 2: Generate stuck-at fault test patterns

4. Generate stuck-at fault test patterns for the scan-ready design.
5. Save the ATPG results.
6. Verify the Verilog format test patterns (optional).

Hint:

In this homework, all you need is to make sure that your test coverage will over than 98%. You can do some experiments to find the minimum pattern count.

Online Submission (FTP):

Please submit a zipped file named *StudentID_HW4_vk.zip*, including:

(k is the number of version, k =1,2,…)

FTP:

Deadline	12:00 5/15/2018
IP	140.112.18.84
Port	1232
Account	CVSD_STUDENT
Password	cvsd2018

Script Files:

1. "dft.tcl" : dft insertion script
2. "atpg.tcl" : atpg script

Synthesis Results:

3. "FAS_syn.v" : gate level netlist (non-scan)
4. "FAS_syn.sdf" : pre-scan (non-scan) sdf file
5. "report_FAS_syn.txt" : pre-scan report summarizing timing, power, and area

DFT Insertion Results:

6. FAS_dft.v" : gate level netlist (scan-ready)
7. "FAS_dft.sdf" : post-scan (scan-ready) sdf file
8. "report_dft.txt" : post-scan report summarizing timing, power, and area
9. "FAS_dft.spf" : test protocol file
10. "FAS_dft.scan_path" : scan path report
11. "FAS_dft.scan_cell" : scan cell report

ATPG Results:

12. "FAS_atpg.stil" : STIL format test patterns

Questions:

13. "Answers.txt": answer the following questions by **your results**. All answers must base on your own result. There is no golden answer for all students.

    (A)

    A-1.How many flip-flops are chained?

    A-2.How many scan cells in every scan chain, respectively?

A-3. What are the inputs and outputs of these scan chains?

A-4. What is the name of the scan enable pin for your scan chain?

(B)

B-1. What is the area before scan chain insertion?

B-2. What is the area after scan chain insertion?

B-3. How much is the area overhead percentage of scan chain?

B-4. Try to explain why scan chain introduces area overhead.

(C) Ignore the input external and output external delay.

C-1. How long (ns) is the critical path delay before scan chain insertion?

C-2. How long the critical path after scan chain insertion?

C-3. How many percent is the path delay overhead? If the endpoint of the critical path is a register type gate, consider the setup time in your critical path delay. Sometimes, the most critical path changes. If your designs do so, try to explain why.

C-4. Sometimes, the individual gate delay changes in the critical path. Try to explain why?

(D)

D-1. How many total faults (uncollapsed) are there in the circuit?

D-2. How many patterns do we have?

D-3. What is the test coverage (%)?

D-4. What is the fault coverage (%)?

Revised by Bing-Chuan Bai, 2011
Revised by Kuan-Yu Liao, 2012
Revised by Chieh-Fu Chu, 2013
Revised by Guo-Yu Lin, 2014
Revised by Kuan-Yen Huang, 2015
Revised by Po-Wei Chen, 2018