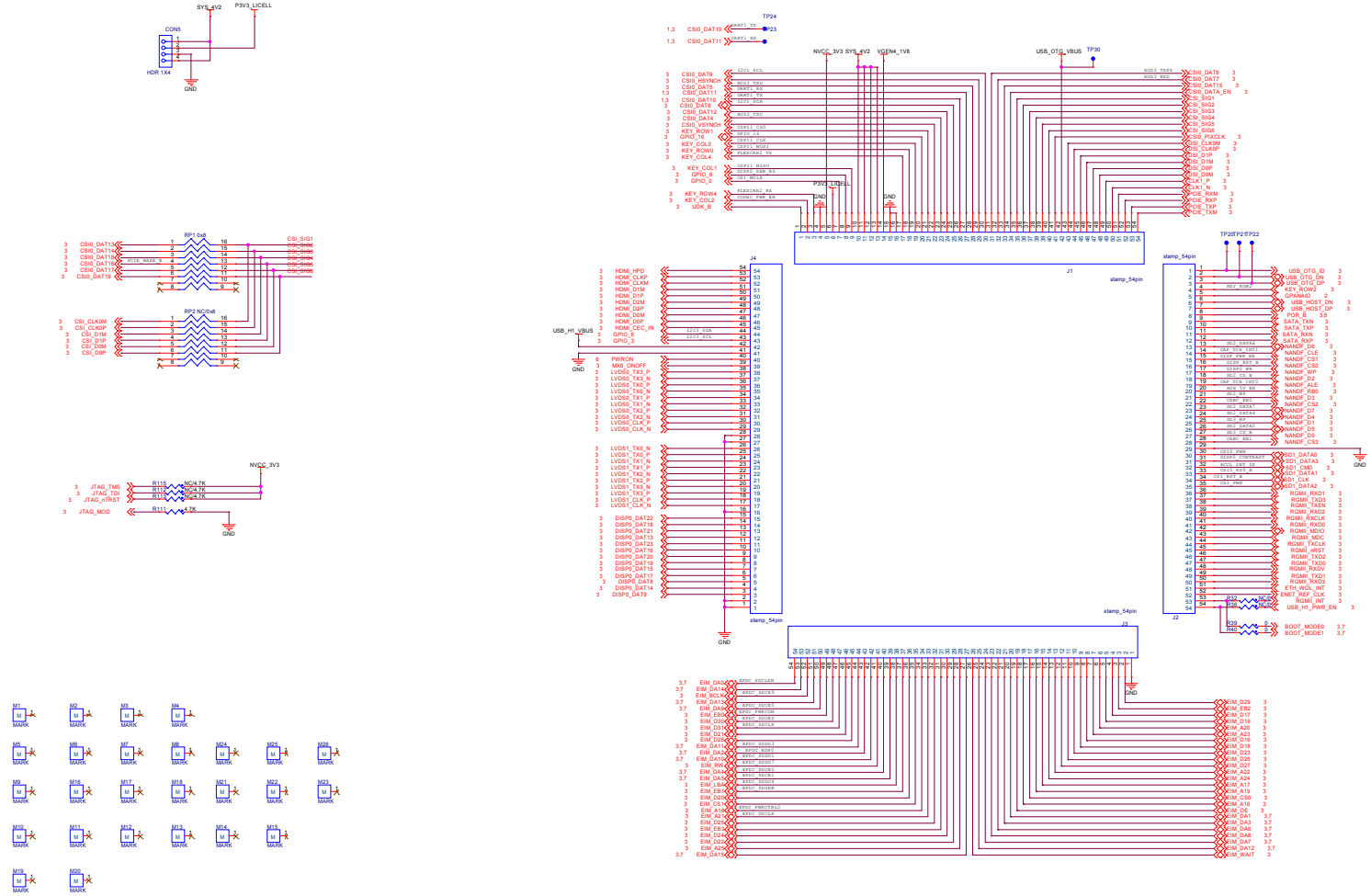
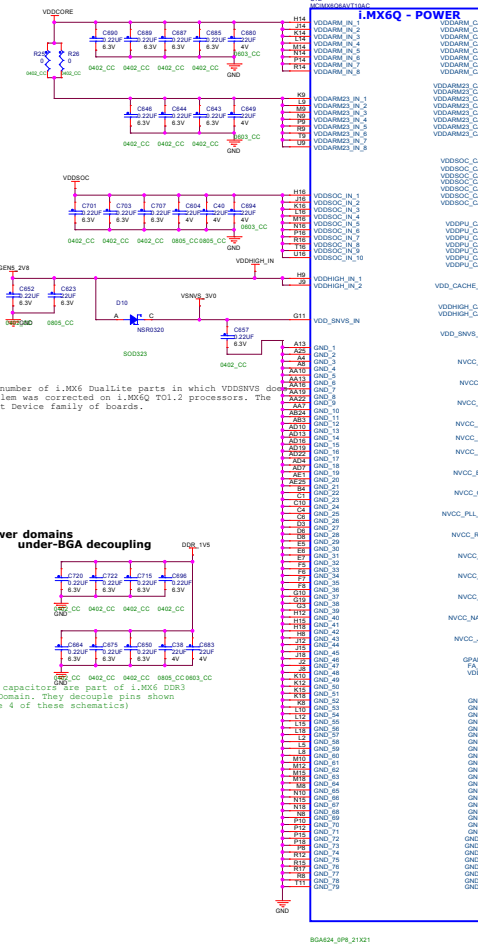


D-Chip Co.,Ltd		
Title :	01 CONNECTOR	
Size D	Document Number : i.MX6_Core_S3.2.1.DSN	Rev 3.2
Date: Wednesday, December 07, 2016	Sheet 1 of 7	



NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 Dualite parts in which VDDSNVS does not come up when VDDHIGH IN is applied. A similar problem was corrected on i.MX6Q TO1.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

MX6 power domains under-BGA decoupling

(These capacitors are part of i.MX6 DDR3 Power Domain. They decouple pins shown on Page 4 of these schematics)

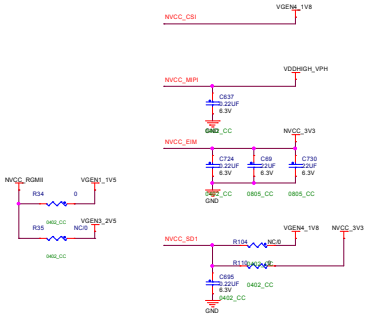
NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 Duallite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and Duallite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

Figure 1. All-In-One circuit

Table 4. VDDARMxx_xx Power Connections

	i.MX 6Quad	i.MX 6Dual	i.MX 6DualLite	i.MX 6Solo
SH1	Shorted	Open	Shorted	Shorted
SH2	Shorted	Open	Shorted	Shorted
R1	Open	Shorted	Open	Open
R2	Open	Shorted	Open	Open



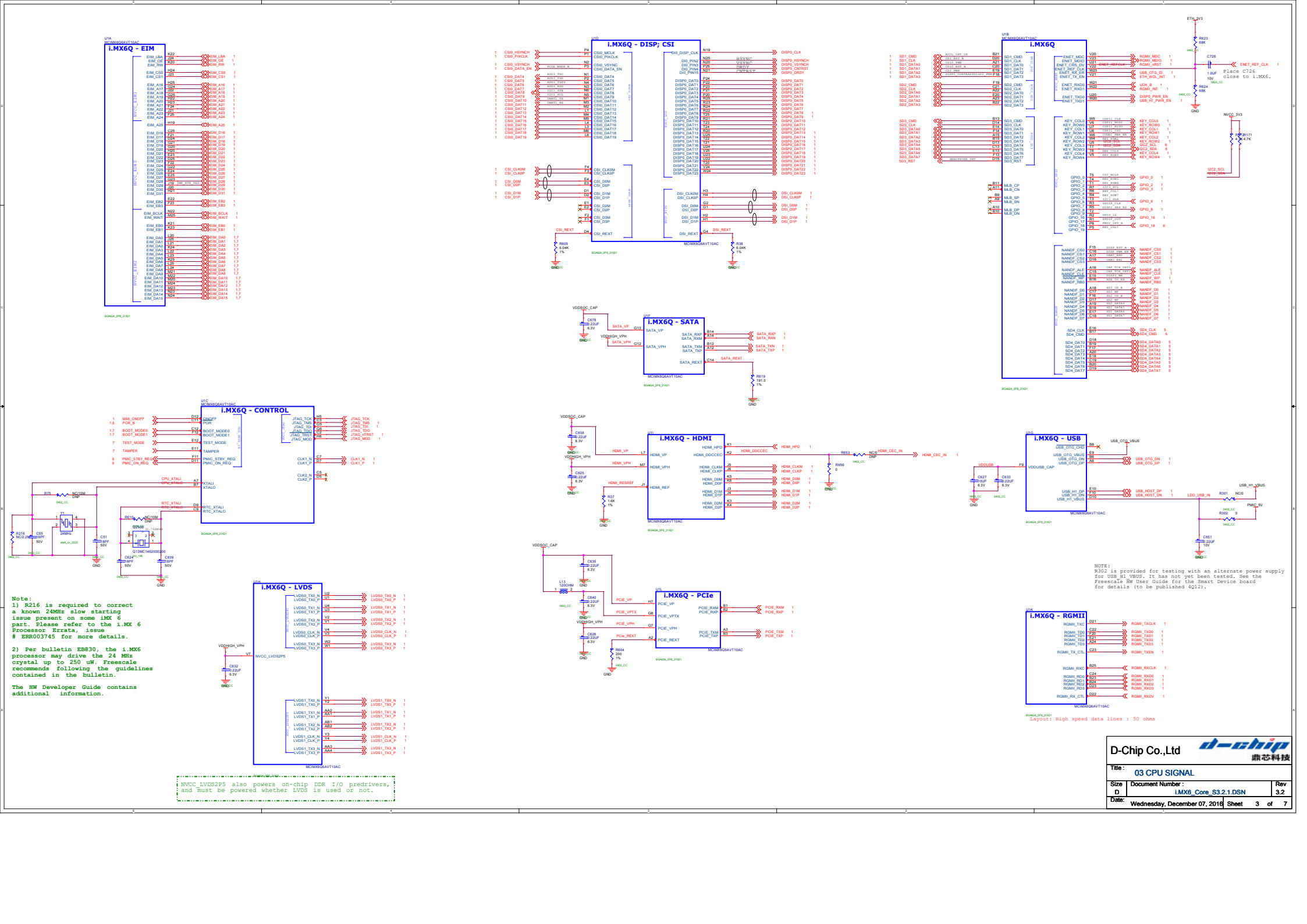
NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

D-Chip Co.,Ltd

Title : 02 CPU POWER

Size	Document Number :	Rev
D	i.MX6_Core_S3.2.1.DSN	3.2

Date: Wednesday, December 07, 2016 Sheet 2 of 7


i.MX6Q - EIM
i.MX6Q - DISP; CSI
i.MX6Q
i.MX6Q - CONTROL
i.MX6Q - SATA
i.MX6Q - HDMI
i.MX6Q - USB
i.MX6Q - LVDS
i.MX6Q - PCIe
i.MX6Q - RGMII
Note:
1) R216 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.
2) Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.
The HW Developer Guide contains additional information.
NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.
Place C726 close to i.MX6.
NOTE:
R302 is provided for testing with an alternate power supply for USB_H1_VBUS. It has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).
Layout: High speed data lines : 50 ohms
D-Chip Co.,Ltd
03 CPU SIGNAL
Size D
Document Number : i.MX6_Core_S3.2.1.DSN
Rev 3.2
Date: Wednesday, December 07, 2016
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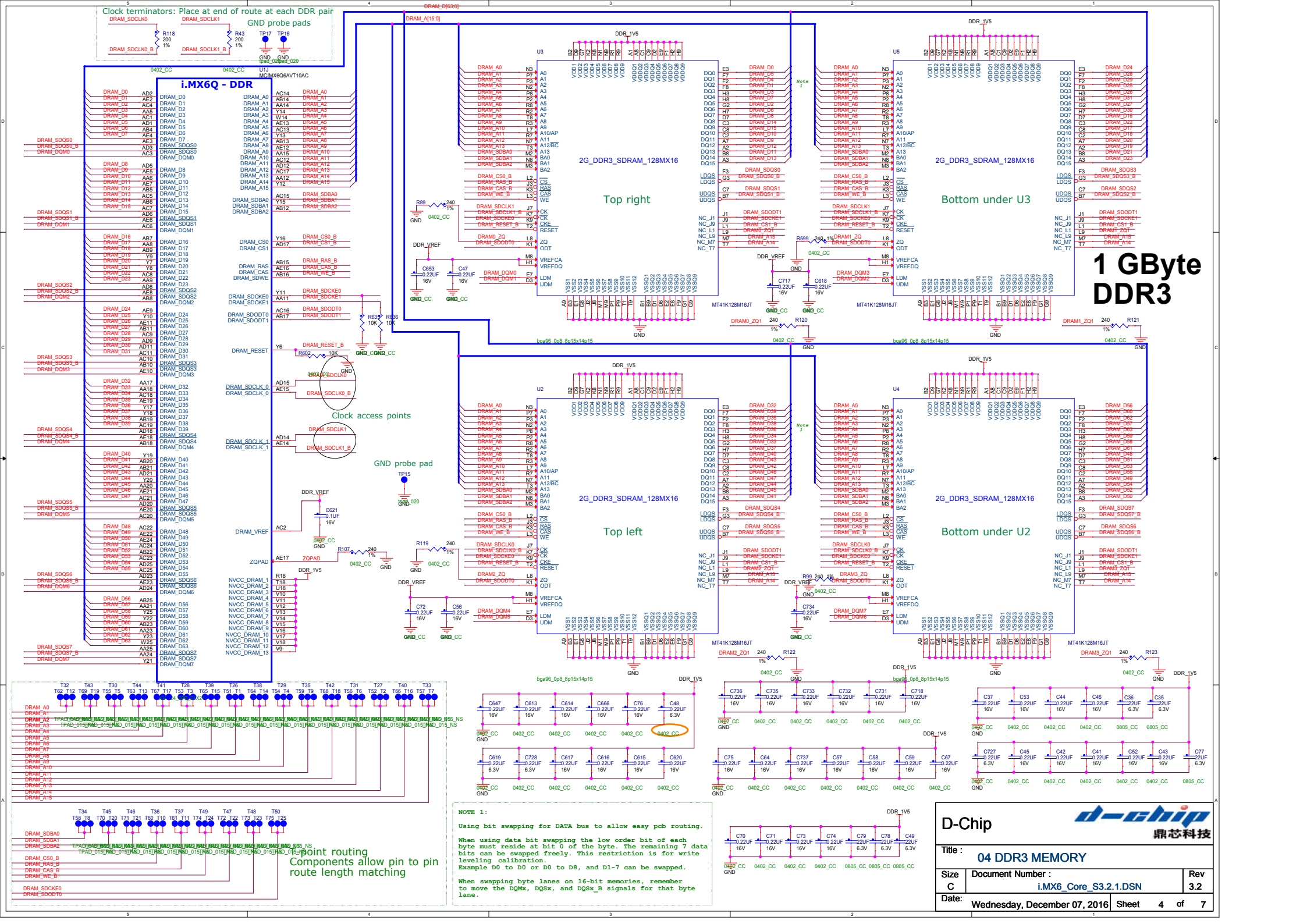
Clock terminators: Place at end of route at each DDR pair
GND probe pads
i.MX6Q - DDR
Top right
Top left
Bottom under U3
Bottom under U2
2G_DDR3_SDRAM_128MX16
MT41K128M16JT
1 GByte
DDR3
Clock access points
GND probe pad
point routing
Components allow pin to pin
route length matching
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
D-Chip
Title :
04 DDR3 MEMORY
Size
C
Document Number :
i.MX6_Core_S3.2.1.DSN
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3.2
Date:
Wednesday, December 07, 2016
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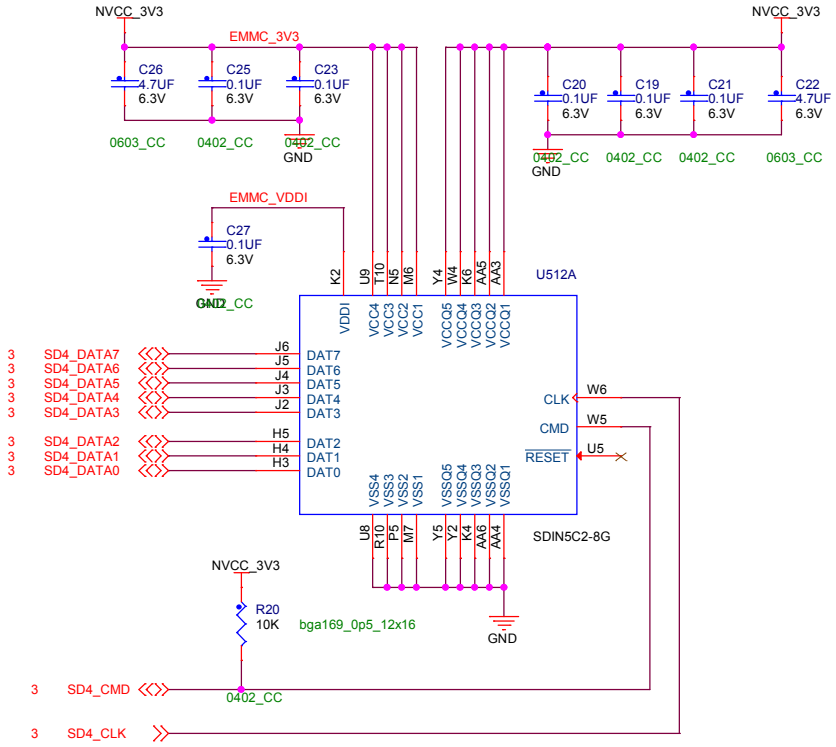
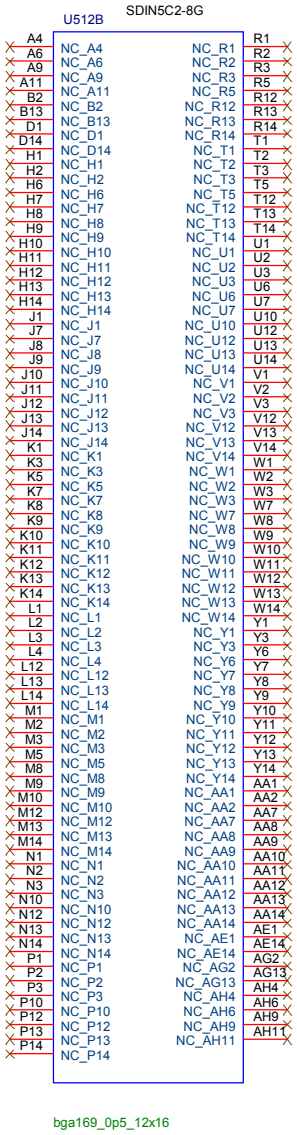
4
of
7

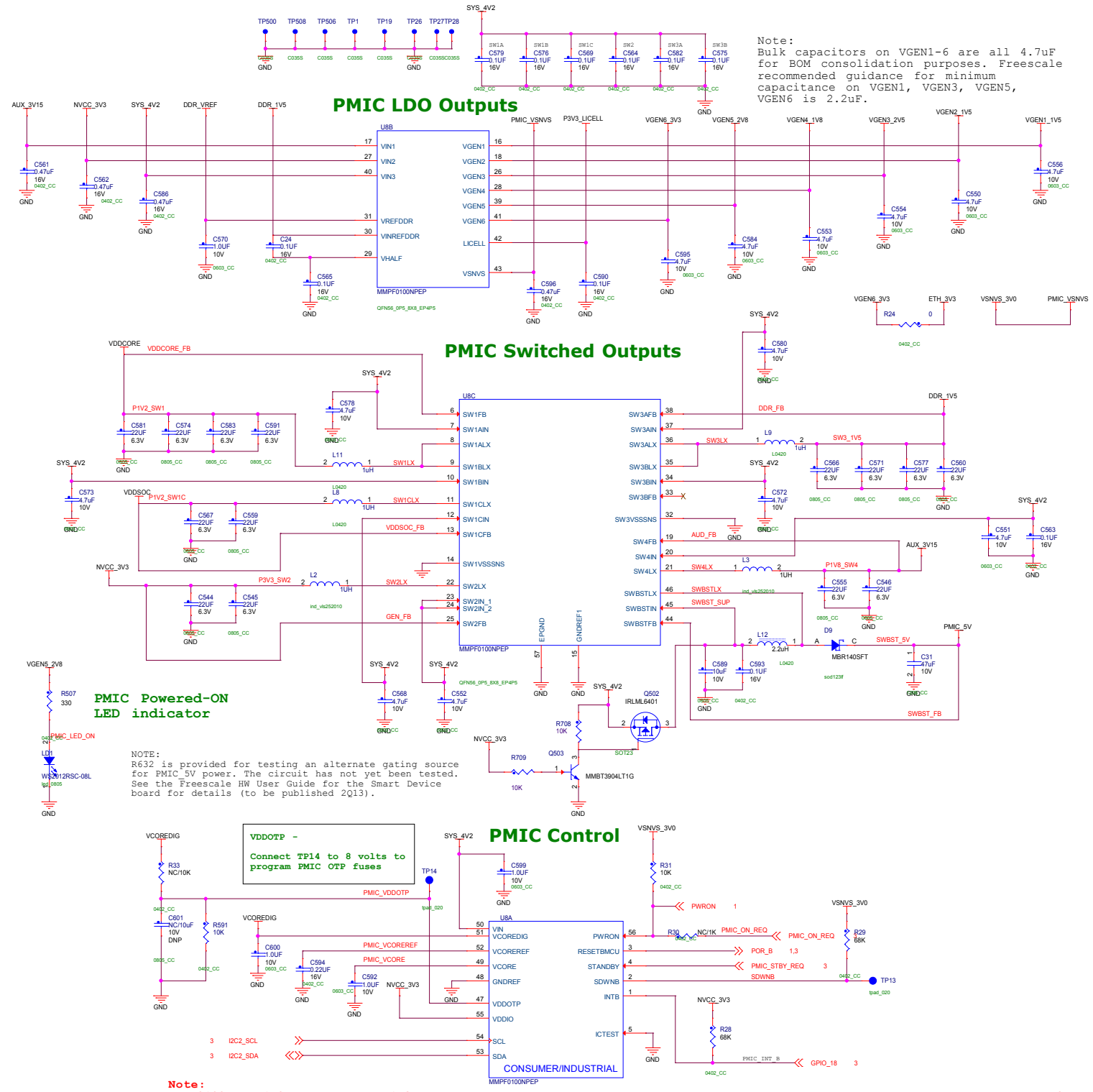
8GB eMMC MEMORY





Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

D-Chip		
Title : 05 eMMC		
Size B	Document Number : i.MX6_Core_S3.2.1.DSN	Rev 3.2
Date: Wednesday, December 07, 2016	Sheet 5 of 7	



Typical Power Requirements

	Voltage	Power Up Sequence	Current Drawn (mA)	SYS 4V2 Current (mA)	NOTES
SW1A SW1B	1.375	1	2155	1001	
SW1C	1.375	2	1590	739	
SW2	3.3	5	653	728	
SW3A SW3B	1.5	3	1500	760	
SW4	3.15	6	200	213	
SWBST	5.0	13	300	507	
VGEN1	1.5	9	100	0	Supplied from SW4
VGEN2	1.5	10	250	0	Supplied from SW4
VGEN3	2.8	11	70	66	
VGEN4	1.8	12	310	189	
VGEN5	2.8	10	75	71	See Note on Page 20
VGEN6	3.3	8	160	178	
VSNVS	3.0	0	0.2	0	
VREFDDR	0.75	3	10	3	
Total System Current Requirements:			4454		

SYSTEM POWER RAILS

Voltge	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB LVDS1 HDMI	PF0100 SWBST	600	
	AUX_5V	SATA LVDS0 CAN	MAX8815	1000	
3.3	GEN_3V3	EMMC SD3 NOR SATA LVDS HDMI MIPI mPCIe SENSORS	PF0100 SW2	2000	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_JTAG
	VGEN6_3V3	ETH	PF0100 VGEN6	200	NVCC_ENET
3.15	AUX_3V15	EXP HDR TOUCH GPS	PF0100 SW4	1000	Supplies: VGEN1 VGEN2
2.8	VDDHIGH_IN	IMX6	PF0100 VGEN5	100	
	VGEN3_2V5	CAMERA	PF0100 VGEN3	100	
2.5	GEN_2V5	SATA HDMI MIPI mPCIe	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
1.8	GEN_1V8	AUDIO CAMERA ACC	PF0100 VGEN4	350	NVCC_SD1 NVCC_CSI
1.5	VGEN2_1V5	CAMERA	PF0100VGEN2	250	
	VGEN1_1V5	GPS mPCIe	PF0100 VGEN1	100	
	DDR_1V5	DDR	PF0100 SW3A/B	2500	
1.375	VDDCORE	ARMCORE	PF0100 SW1A/B	2500	
	VDDSOC	VDDSOC	PF0100 SW1C	1750	
0.75	VREFDDR	DDR	PF0100 VREFDDR	10	

D-Chip 鼎芯科技

Title : 06 PF0100 PMIC

Size	Document Number :	Rev
C	i.MX6_Core_S3.2.1.DSN	3.2
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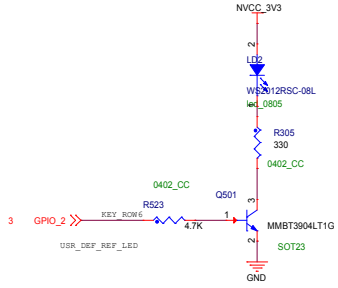
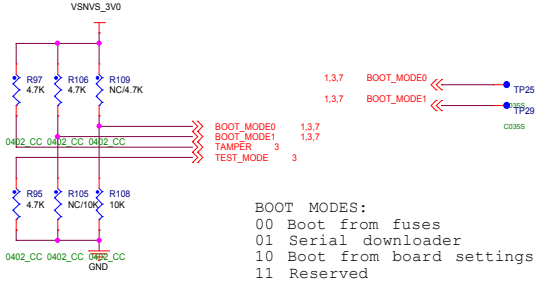
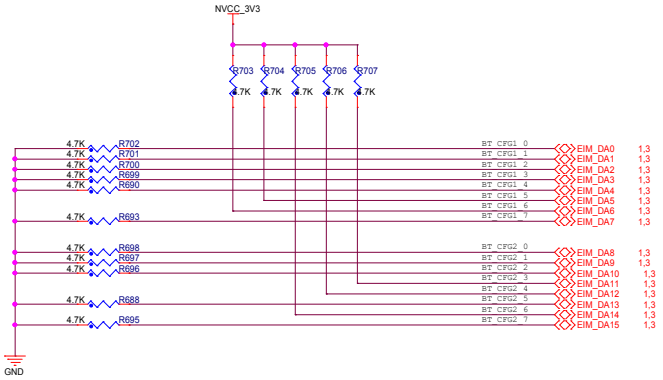




BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved



8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0

Boot Select Table

NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

D-Chip			
Title : 07 BOOT SELECT			
Size C	Document Number : i.MX6_Core_S3.2.1.DSN		Rev 3.2
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