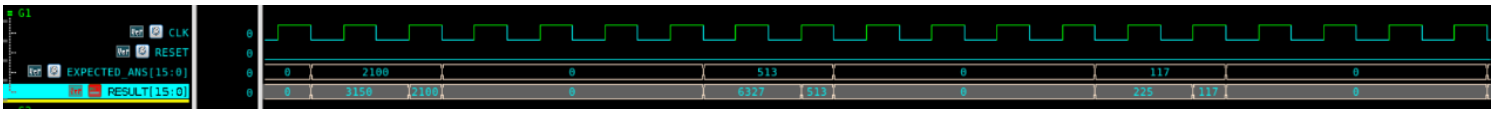
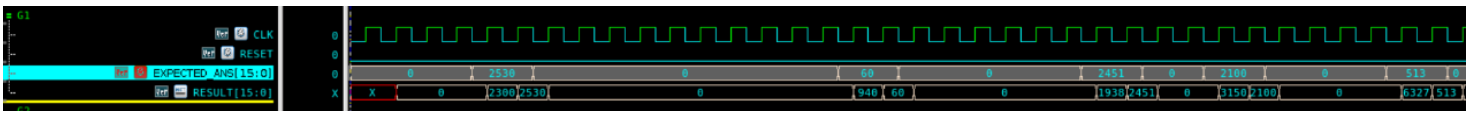
1. Pre-sim 波型:

Clock-gating:



Pipeline:

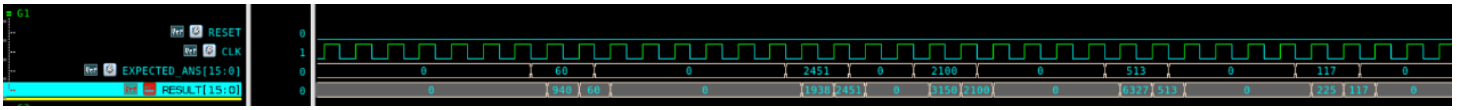


Non-pipeline:

2. Gate-level-sim 波型:

Clock-gating:

Pipeline:



Non-pipeline:

3. Design Compiler:

Clock-gating(delay-opt):

Area:

```
                                Global cell area         Local cell area
                                ------------------  ---------------------------
Hierarchical cell               Absolute   Percent  Combi-    Noncombi-  Black-
                                Total      Total    national  national   boxes   Design
------------------------------  ---------  -------  --------  ---------  ------  ----------------------------------------
hw2_pipe_clkgating               203.0054    100.0    2.0218     0.0000  0.0000  hw2_pipe_clkgating
clk_gate_C21                       0.8294      0.4    0.0000     0.8294  0.0000  SNPS_CLOCK_GATE_HIGH_hw2_pipe_clkgating
fs                                31.7261     15.6    4.1472     0.0000  0.0000  first_stage
fs/add_31                          7.9834      3.9    7.9834     0.0000  0.0000  first_stage_DW01_add_0
fs/dff8                           10.3680      5.1    0.0000     0.0000  0.0000  D_FF_8
fs/dff8/ff_gen_0__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_0
fs/dff8/ff_gen_1__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_25
fs/dff8/ff_gen_2__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_24
fs/dff8/ff_gen_3__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_23
fs/dff8/ff_gen_4__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_22
fs/dff8/ff_gen_5__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_21
fs/dff8/ff_gen_6__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_20
fs/dff8/ff_gen_7__ff_inst          1.2960      0.6    0.1555     1.1405  0.0000  D_FF_19
fs/sub_31                          9.2275      4.5    9.2275     0.0000  0.0000  first_stage_DW01_sub_0
ss                               168.4282     83.0    0.0000     0.0000  0.0000  second_stage
ss/dff16                          20.9434     10.3    0.2074     0.0000  0.0000  D_FF_16
ss/dff16/ff_gen_0__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_18
ss/dff16/ff_gen_10__ff_inst        1.2960      0.6    0.1555     1.1405  0.0000  D_FF_6
ss/dff16/ff_gen_11__ff_inst        1.2960      0.6    0.1555     1.1405  0.0000  D_FF_5
ss/dff16/ff_gen_12__ff_inst        1.2960      0.6    0.1555     1.1405  0.0000  D_FF_4
ss/dff16/ff_gen_13__ff_inst        1.2960      0.6    0.1555     1.1405  0.0000  D_FF_3
ss/dff16/ff_gen_14__ff_inst        1.2960      0.6    0.1555     1.1405  0.0000  D_FF_2
ss/dff16/ff_gen_15__ff_inst        1.2960      0.6    0.1555     1.1405  0.0000  D_FF_1
ss/dff16/ff_gen_1__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_17
ss/dff16/ff_gen_2__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_15
ss/dff16/ff_gen_3__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_14
ss/dff16/ff_gen_4__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_13
ss/dff16/ff_gen_5__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_12
ss/dff16/ff_gen_6__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_11
ss/dff16/ff_gen_7__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_10
ss/dff16/ff_gen_8__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_9
ss/dff16/ff_gen_9__ff_inst         1.2960      0.6    0.1555     1.1405  0.0000  D_FF_7
ss/mult_42                       147.4848     72.7  147.4848     0.0000  0.0000  second_stage_DW_mult_uns_2
------------------------------  ---------  -------  --------  ---------  ------  ----------------------------------------
Total                                                174.8045    28.2010  0.0000
1
```

Power:

```
Design        Wire Load Model            Library
------------------------------------------------
hw2_pipe_clkgating     ZeroWireload      N16ADFP_StdCellss0p72vm40c_ccs


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


Attributes
----------|
i - Including register clock pin internal power


  Cell Internal Power  = 629.6423 uW   (69%)
  Net Switching Power  = 286.3854 uW   (31%)
                         ---------
Total Dynamic Power    = 916.0278 uW  (100%)

Cell Leakage Power     = 179.7616 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.2498        2.1762e-02          8.0289e-03            0.2715  (  29.64%)  i
register        4.2010e-02        1.3622e-02            16.9682          5.5649e-02  (   6.07%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational      0.3379           0.2510            162.7801             0.5890  (  64.29%)
------------------------------------------------------------------------------------------------
Total              0.6296 mW        0.2864 mW         179.7564 nW          0.9162 mW
1
```

Time:

```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
hw2_pipe_clkgating ZeroWireload          N16ADFP_StdCellss0p72vm40c_ccs

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
fs/dff8/ff_gen_7__ff_inst/q_reg/CP (DFCNQD2BWP16P90LVT)
                                                        0.00       0.00 r
fs/dff8/ff_gen_7__ff_inst/q_reg/Q (DFCNQD2BWP16P90LVT)
                                                        0.05       0.05 f
fs/dff8/ff_gen_7__ff_inst/q (D_FF_19)                   0.00       0.05 f
fs/dff8/q[7] (D_FF_8)                                   0.00       0.05 f
fs/first_stage_result[7] (first_stage)                  0.00       0.05 f
ss/sum[7] (second_stage)                                0.00       0.05 f
ss/mult_42/b[7] (second_stage_DW_mult_uns_2)            0.00       0.05 f
ss/mult_42/U480/ZN (CKND2BWP16P90LVT)                   0.01       0.05 r
ss/mult_42/U331/ZN (CKND2D4BWP16P90LVT)                 0.01       0.06 f
ss/mult_42/U545/ZN (ND2D2BWP16P90LVT)                   0.01       0.07 r
ss/mult_42/U454/Z (OR2D2BWP16P90LVT)                    0.01       0.08 r
ss/mult_42/U455/ZN (ND2D4BWP16P90LVT)                   0.01       0.09 f
ss/mult_42/U338/ZN (ND2D4BWP16P90LVT)                   0.01       0.09 r
ss/mult_42/U340/ZN (ND3D4BWP16P90LVT)                   0.01       0.10 f
ss/mult_42/U343/ZN (CKND2BWP16P90LVT)                   0.01       0.11 r
ss/mult_42/U447/ZN (AOAI211D2BWP16P90LVT)               0.01       0.12 f
ss/mult_42/U539/Z (XOR2D4BWP16P90LVT)                   0.02       0.14 r
ss/mult_42/U437/Z (XOR2D2BWP16P90LVT)                   0.02       0.16 f
ss/mult_42/U547/ZN (NR2D2BWP16P90LVT)                   0.01       0.17 r
ss/mult_42/U537/ZN (OAI21D2BWP16P90LVT)                 0.01       0.19 f
ss/mult_42/U626/ZN (AOI21D1BWP16P90LVT)                 0.01       0.20 r
ss/mult_42/U520/ZN (OAI21D1BWP16P90LVT)                 0.01       0.21 f
ss/mult_42/U625/ZN (XNR2D1BWP16P90LVT)                  0.02       0.23 r
ss/mult_42/product[14] (second_stage_DW_mult_uns_2)     0.00       0.23 r
ss/dff16/d[14] (D_FF_16)                                0.00       0.23 r
ss/dff16/ff_gen_14__ff_inst/d (D_FF_2)                  0.00       0.23 r
ss/dff16/ff_gen_14__ff_inst/q_reg/D (DFCNQD2BWP16P90LVT)
                                                        0.00       0.23 r
data arrival time                                                  0.23

clock clk (rise edge)                                   0.24       0.24
clock network delay (ideal)                             0.00       0.24
ss/dff16/ff_gen_14__ff_inst/q_reg/CP (DFCNQD2BWP16P90LVT)
                                                        0.00       0.24 r
library setup time                                     -0.01       0.23
data required time                                                 0.23
-----------------------------------------------------------------------
data required time                                                 0.23
data arrival time                                                 -0.23
-----------------------------------------------------------------------
slack (VIOLATED: increase significant digits)                      0.00
```

Pipeline(delay-opt):

Area:

```
Hierarchical area distribution
------------------------------

                                Global cell area         Local cell area
                                ----------------  ---------------------------
Hierarchical cell               Absolute   Percent  Combi-    Noncombi-  Black-
                                Total      Total    national  national   boxes   Design
------------------------------  ---------  -------  --------  ---------  ------  --------------------------
hw2_pipe                         198.8064    100.0    0.0000     0.0000  0.0000  hw2_pipe
fs                                32.4000     16.3    4.1472     0.0000  0.0000  first_stage
fs/add_23                          7.9834      4.0    7.9834     0.0000  0.0000  first_stage_DW01_add_0
fs/dff8                           11.0419      5.6    0.2074     0.0000  0.0000  D_FF_8
fs/dff8/ff_gen_0_ff_inst           1.2960      0.7    0.1555     1.1405  0.0000  D_FF_0
fs/dff8/ff_gen_1_ff_inst           1.2960      0.7    0.1555     1.1405  0.0000  D_FF_25
fs/dff8/ff_gen_2_ff_inst           1.2960      0.7    0.1555     1.1405  0.0000  D_FF_24
fs/dff8/ff_gen_3_ff_inst           1.7626      0.9    0.4666     1.2960  0.0000  D_FF_23
fs/dff8/ff_gen_4_ff_inst           1.2960      0.7    0.1555     1.1405  0.0000  D_FF_22
fs/dff8/ff_gen_5_ff_inst           1.2960      0.7    0.1555     1.1405  0.0000  D_FF_21
fs/dff8/ff_gen_6_ff_inst           1.2960      0.7    0.1555     1.1405  0.0000  D_FF_20
fs/dff8/ff_gen_7_ff_inst           1.2960      0.7    0.1555     1.1405  0.0000  D_FF_19
fs/sub_23                          9.2275      4.6    9.2275     0.0000  0.0000  first_stage_DW01_sub_0
ss                               166.4064     83.7    0.0000     0.0000  0.0000  second_stage
ss/dff16                          21.1507     10.6    0.4147     0.0000  0.0000  D_FF_16
ss/dff16/ff_gen_0_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_18
ss/dff16/ff_gen_10_ff_inst         1.2960      0.7    0.1555     1.1405  0.0000  D_FF_6
ss/dff16/ff_gen_11_ff_inst         1.2960      0.7    0.1555     1.1405  0.0000  D_FF_5
ss/dff16/ff_gen_12_ff_inst         1.2960      0.7    0.1555     1.1405  0.0000  D_FF_4
ss/dff16/ff_gen_13_ff_inst         1.2960      0.7    0.1555     1.1405  0.0000  D_FF_3
ss/dff16/ff_gen_14_ff_inst         1.2960      0.7    0.1555     1.1405  0.0000  D_FF_2
ss/dff16/ff_gen_15_ff_inst         1.2960      0.7    0.1555     1.1405  0.0000  D_FF_1
ss/dff16/ff_gen_1_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_17
ss/dff16/ff_gen_2_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_15
ss/dff16/ff_gen_3_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_14
ss/dff16/ff_gen_4_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_13
ss/dff16/ff_gen_5_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_12
ss/dff16/ff_gen_6_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_11
ss/dff16/ff_gen_7_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_10
ss/dff16/ff_gen_8_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_9
ss/dff16/ff_gen_9_ff_inst          1.2960      0.7    0.1555     1.1405  0.0000  D_FF_7
ss/mult_34                       145.2557     73.1  145.2557     0.0000  0.0000  second_stage_DW_mult_uns_2
------------------------------  ---------  -------  --------  ---------  ------  --------------------------
Total                                                171.2794    27.5270  0.0000
```

Power:

```
Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  = 626.7470 uW   (71%)
  Net Switching Power  = 259.8201 uW   (29%)
                         ---------
Total Dynamic Power    = 886.5671 uW  (100%)

Cell Leakage Power     = 177.5667 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.2432           0.0000              0.0000             0.2432  (  27.43%)  i
register       4.1751e-02       1.0478e-02            16.9884         5.2246e-02  (   5.89%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational      0.3418           0.2493            160.5764             0.5913  (  66.68%)
--------------------------------------------------------------------------------------------------
Total              0.6267 mW        0.2598 mW       177.5648 nW          0.8867 mW
1
```

Time:

```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
hw2 pipe           ZeroWireload          N16ADFP StdCellss0p72vm40c ccs

Point                                                    Incr       Path
-----------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.00       0.00
fs/dff8/ff_gen_3__ff_inst/q_reg/CP (DFCNQND2BWP16P90LVT)
                                                         0.00       0.00 r
fs/dff8/ff_gen_3__ff_inst/q_reg/QN (DFCNQND2BWP16P90LVT)
                                                         0.04       0.04 r
fs/dff8/ff_gen_3__ff_inst/U3/ZN (INVD4BWP16P90LVT)       0.01       0.05 f
fs/dff8/ff_gen_3__ff_inst/q (D_FF_23)                    0.00       0.05 f
fs/dff8/q[3] (D_FF_8)                                    0.00       0.05 f
fs/first_stage_result[3] (first_stage)                   0.00       0.05 f
ss/sum[3] (second_stage)                                 0.00       0.05 f
ss/mult_34/b[3] (second_stage_DW_mult_uns_2)             0.00       0.05 f
ss/mult_34/U310/ZN (XNR2D8BWP16P90LVT)                   0.02       0.07 r
ss/mult_34/U472/ZN (OAI22D4BWP16P90LVT)                  0.01       0.08 f
ss/mult_34/U471/Z (XOR2D4BWP16P90LVT)                    0.02       0.10 r
ss/mult_34/U157/S (FA1D1BWP16P90LVT)                     0.03       0.13 f
ss/mult_34/U386/ZN (CKND2BWP16P90LVT)                    0.01       0.14 r
ss/mult_34/U385/ZN (ND2D2BWP16P90LVT)                    0.01       0.15 f
ss/mult_34/U409/ZN (IOA21D4BWP16P90LVT)                  0.02       0.16 f
ss/mult_34/U515/ZN (AOI21D4BWP16P90LVT)                  0.01       0.17 r
ss/mult_34/U483/ZN (OAI21D4BWP16P90LVT)                  0.01       0.18 f
ss/mult_34/U481/ZN (AOI21D1BWP16P90LVT)                  0.01       0.20 r
ss/mult_34/U609/ZN (OAI21D1BWP16P90LVT)                  0.01       0.21 f
ss/mult_34/U608/ZN (XNR2D1BWP16P90LVT)                   0.02       0.23 r
ss/mult_34/product[14] (second_stage_DW_mult_uns_2)      0.00       0.23 r
ss/dff16/d[14] (D_FF_16)                                 0.00       0.23 r
ss/dff16/ff_gen_14__ff_inst/d (D_FF_2)                   0.00       0.23 r
ss/dff16/ff_gen_14__ff_inst/q_reg/D (DFCNQD2BWP16P90LVT)
                                                         0.00       0.23 r
data arrival time                                                   0.23

clock clk (rise edge)                                    0.24       0.24
clock network delay (ideal)                              0.00       0.24
ss/dff16/ff_gen_14__ff_inst/q_reg/CP (DFCNQD2BWP16P90LVT)
                                                         0.00       0.24 r
library setup time                                      -0.01       0.23
data required time                                                  0.23
-----------------------------------------------------------------------
data required time                                                  0.23
data arrival time                                                  -0.23
-----------------------------------------------------------------------
slack (VIOLATED: increase significant digits)                       0.00
```

Non-pipeline(delay-opt):

Area:

```
Hierarchical area distribution
------------------------------

                              Global cell area          Local cell area
                              ------------------  ----------------------------
Hierarchical cell             Absolute   Percent  Combi-    Noncombi-  Black-
                              Total      Total    national  national   boxes   Design
------------------------------ ---------  -------  --------  ---------  ------  --------------------------
hw2_nonpipe                    411.9725    100.0    8.7610     0.0000  0.0000  hw2_nonpipe
add_10                          41.4202     10.1   41.4202     0.0000  0.0000  hw2_nonpipe_DW01_add_2
mult_10                        141.7306     34.4  141.7306     0.0000  0.0000  hw2_nonpipe_DW_mult_uns_7
mult_12                        160.9114     39.1  160.9114     0.0000  0.0000  hw2_nonpipe_DW_mult_uns_6
sub_12                          59.1494     14.4   59.1494     0.0000  0.0000  hw2_nonpipe_DW01_sub_2
------------------------------ ---------  -------  --------  ---------  ------  --------------------------
Total                                                411.9725     0.0000  0.0000
```

Power:

```
Design        Wire Load Model            Library
------------------------------------------------
hw2 nonpipe            ZeroWireload      N16ADFP StdCellss0p72vm40c ccs


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.0662 mW   (58%)
  Net Switching Power  = 780.8401 uW   (42%)
                         ---------
Total Dynamic Power    =   1.8471 mW  (100%)

Cell Leakage Power     = 494.0578 nW

Information: report power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io pad              0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory              0.0000            0.0000            0.0000            0.0000  (   0.00%)
black box           0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock network       0.0000            0.0000            0.0000            0.0000  (   0.00%)  i
register            0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential          0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational       1.0663            0.7808          494.0559            1.8476  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total               1.0663 mW         0.7808 mW       494.0559 nW         1.8476 mW
1
```

Time:

```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
hw2 nonpipe        ZeroWireload          N16ADFP StdCellss0p72vm40c ccs

Point                                                   Incr       Path
-----------------------------------------------------------------------
input external delay                                    0.00       0.00 r
b[1] (in)                                               0.00       0.00 r
sub 12/B[1] (hw2 nonpipe_DW01_sub_2)                    0.00       0.00 r
sub 12/U150/ZN (CKND16BWP16P90LVT)                      0.00       0.00 f
sub 12/U125/ZN (NR2D8BWP16P90LVT)                       0.01       0.01 r
sub 12/U99/ZN (OAI21D4BWP16P90LVT)                      0.01       0.02 f
sub 12/U170/ZN (AOI21D4BWP16P90LVT)                     0.01       0.03 r
sub 12/U139/ZN (OAI21D1BWP16P90LVT)                     0.01       0.04 f
sub 12/U133/ZN (ND2D1BWP16P90LVT)                       0.01       0.05 r
sub 12/U135/ZN (ND2D4BWP16P90LVT)                       0.01       0.06 f
sub 12/DIFF[7] (hw2 nonpipe_DW01_sub_2)                 0.00       0.06 f
mult 12/a[7] (hw2 nonpipe_DW_mult_uns_6)                0.00       0.06 f
mult 12/U316/Z (XOR2D4BWP16P90LVT)                      0.02       0.09 r
mult 12/U521/ZN (OAI22D4BWP16P90LVT)                    0.01       0.09 f
mult 12/U304/ZN (CKND2BWP16P90LVT)                      0.01       0.10 r
mult 12/U318/ZN (IND2D2BWP16P90LVT)                     0.01       0.11 f
mult 12/U312/ZN (CKND2D2BWP16P90LVT)                    0.01       0.11 r
mult 12/U519/Z (XOR2D4BWP16P90LVT)                      0.02       0.14 f
mult 12/U425/Z (XOR2D4BWP16P90LVT)                      0.02       0.16 f
mult 12/U374/Z (XOR2D2BWP16P90LVT)                      0.02       0.17 r
mult 12/U373/ZN (ND2D2BWP16P90LVT)                      0.01       0.18 f
mult 12/U503/ZN (CKND2BWP16P90LVT)                      0.01       0.19 r
mult 12/U531/ZN (AOI21D2BWP16P90LVT)                    0.01       0.19 f
mult 12/U562/ZN (OAI21D2BWP16P90LVT)                    0.01       0.20 r
mult 12/U388/ZN (AOI21D2BWP16P90LVT)                    0.01       0.21 f
mult 12/U579/ZN (OAI21D1BWP16P90LVT)                    0.01       0.22 r
mult 12/U632/ZN (XNR2D1BWP16P90LVT)                     0.02       0.24 f
mult 12/product[15] (hw2 nonpipe_DW_mult_uns_6)         0.00       0.24 f
U20/ZN (ND2D1BWP16P90LVT)                               0.01       0.24 r
U22/ZN (ND2D1BWP16P90LVT)                               0.01       0.25 f
result[15] (out)                                        0.00       0.25 f
data arrival time                                                  0.25

max_delay                                               0.25       0.25
output external delay                                   0.00       0.25
data required time                                                 0.25
-----------------------------------------------------------------------
data required time                                                 0.25
data arrival time                                                 -0.25
-----------------------------------------------------------------------
slack (VIOLATED: increase significant digits)                      0.00
```

4. 部分驗證截圖:

Clock-gating:

```
------RESET=0 CLK=0 | A= 17 B=  4 C=  9 S=0 Got=    0 # Expected=  117
------RESET=0 CLK=1 | A= 17 B=  4 C=  9 S=0 Got=    0 # Expected=  117
------RESET=0 CLK=1 | A= 17 B=  4 C=  9 S=0 Got=  225 # Expected=  117
------RESET=0 CLK=0 | A= 17 B=  4 C=  9 S=0 Got=  225 # Expected=  117
------RESET=0 CLK=1 | A= 17 B=  4 C=  9 S=0 Got=  225 # Expected=  117
------RESET=0 CLK=1 | A= 17 B=  4 C=  9 S=0 Got=  245 # Expected=  117
------RESET=0 CLK=1 | A= 17 B=  4 C=  9 S=0 Got=  117 # Expected=  117
------RESET=0 CLK=0 | A= 55 B= 18 C=  0 S=1 Got=  117 # Expected=    0
------RESET=0 CLK=0 | A= 55 B= 18 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 55 B= 18 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 55 B= 18 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 55 B= 18 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A=  5 B=  3 C= 64 S=0 Got=    0 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got=    0 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got= 4864 # Expected=  128
------RESET=0 CLK=0 | A=  5 B=  3 C= 64 S=0 Got= 4864 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got= 4864 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got= 4992 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got=  128 # Expected=  128
------RESET=0 CLK=0 | A= 42 B= 28 C=  0 S=0 Got=  128 # Expected=    0
------RESET=0 CLK=0 | A= 42 B= 28 C=  0 S=0 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 42 B= 28 C=  0 S=0 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 42 B= 28 C=  0 S=0 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 42 B= 28 C=  0 S=0 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=0 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=1 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=0 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=1 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=0 | A= 35 B= 51 C=  0 S=1 Got=    0 # Expected=    0
```

Pipeline:

```
------RESET=0 CLK=1 | A= 17 B=  4 C=  9 S=0 Got=  245 # Expected=  117
------RESET=0 CLK=1 | A= 17 B=  4 C=  9 S=0 Got=  117 # Expected=  117
------RESET=0 CLK=0 | A= 55 B= 18 C=  0 S=1 Got=  117 # Expected=    0
------RESET=0 CLK=1 | A= 55 B= 18 C=  0 S=1 Got=  117 # Expected=    0
------RESET=0 CLK=1 | A= 55 B= 18 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 55 B= 18 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 55 B= 18 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 45 B= 31 C=  0 S=1 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A=  5 B=  3 C= 64 S=0 Got=    0 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got=    0 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got= 4864 # Expected=  128
------RESET=0 CLK=0 | A=  5 B=  3 C= 64 S=0 Got= 4864 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got= 4864 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got= 4992 # Expected=  128
------RESET=0 CLK=1 | A=  5 B=  3 C= 64 S=0 Got=  128 # Expected=  128
------RESET=0 CLK=0 | A= 42 B= 28 C=  0 S=0 Got=  128 # Expected=    0
------RESET=0 CLK=1 | A= 42 B= 28 C=  0 S=0 Got=  128 # Expected=    0
------RESET=0 CLK=1 | A= 42 B= 28 C=  0 S=0 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 42 B= 28 C=  0 S=0 Got=    0 # Expected=    0
------RESET=0 CLK=1 | A= 42 B= 28 C=  0 S=0 Got=    0 # Expected=    0
------RESET=0 CLK=0 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=0 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=1 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
------RESET=1 CLK=0 | A= 28 B= 18 C=  0 S=0 Got=    0 # Expected=    0
```

Non-pipeline:

```
300------A=  4 B=  2 C=  0 S=0 Got=    0 # Expected=    0
310------A= 14 B=  4 C=  0 S=0 Got=    0 # Expected=    0
320------A=  3 B=  0 C=  0 S=0 Got=    0 # Expected=    0
330------A= 10 B=  4 C=  0 S=0 Got=    0 # Expected=    0
340------A= 56 B= 43 C=  0 S=0 Got=    0 # Expected=    0
350------A= 25 B= 13 C=  0 S=1 Got=    0 # Expected=    0
360------A= 45 B=  0 C= 22 S=0 Got=    0 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=    2 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=    6 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=   14 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=   78 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=   94 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=  222 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=  478 # Expected=  990
360------A= 45 B=  0 C= 22 S=0 Got=  990 # Expected=  990
370------A=  6 B=  5 C=  0 S=0 Got=  990 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=  982 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=  980 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=  976 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=  960 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=  832 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=  768 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=  256 # Expected=    0
370------A=  6 B=  5 C=  0 S=0 Got=    0 # Expected=    0
380------A= 52 B= 32 C=  0 S=0 Got=    0 # Expected=    0
390------A=  7 B=  2 C= 62 S=0 Got=    0 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=    2 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=    6 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=   22 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=   86 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=  214 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got= 1238 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got= 1270 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got= 1142 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=  118 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=   54 # Expected=  310
390------A=  7 B=  2 C= 62 S=0 Got=  310 # Expected=  310
400------A= 41 B= 33 C=  0 S=0 Got=  310 # Expected=    0
400------A= 41 B= 33 C=  0 S=0 Got=  318 # Expected=    0
400------A= 41 B= 33 C=  0 S=0 Got=  316 # Expected=    0
400------A= 41 B= 33 C=  0 S=0 Got=  296 # Expected=    0
400------A= 41 B= 33 C=  0 S=0 Got=  288 # Expected=    0
400------A= 41 B= 33 C=  0 S=0 Got=  352 # Expected=    0
```

5. Primetime power 測量截圖:

Clock-gating:

```
****************************************
Report : Averaged Power
         -hierarchy
Design : hw2_pipe_clkgating
Version: V-2023.12
Date   : Thu Oct 17 20:56:03 2024
****************************************


                                    Int      Switch   Leak     Total
Hierarchy                           Power    Power    Power    Power    %
------------------------------------------------------------------------------
hw2_pipe_clkgating                  1.30e-05 6.39e-06 1.75e-07 1.95e-05 100.0
  ss (second_stage)                 9.31e-06 5.17e-06 1.52e-07 1.46e-05  74.9
    mult_42_(second_stage_DW_mult_uns 2)
                                    6.62e-06 4.99e-06 1.40e-07 1.18e-05  60.1
    dff16 (D_FF_16)                 2.69e-06 1.76e-07 1.27e-08 2.88e-06  14.7
      ff_gen_13_ff_inst (D_FF_3)    1.46e-07 7.07e-09 7.25e-10 1.54e-07   0.8
      ff_gen_9_ff_inst (D_FF_7)     1.90e-07 7.07e-09 7.93e-10 1.97e-07   1.0
      ff_gen_12_ff_inst (D_FF_4)    1.41e-07 7.07e-09 7.34e-10 1.49e-07   0.8
      ff_gen_8_ff_inst (D_FF_9)     1.84e-07 7.07e-09 7.89e-10 1.91e-07   1.0
      ff_gen_11_ff_inst (D_FF_5)    1.65e-07 7.07e-09 7.58e-10 1.73e-07   0.9
      ff_gen_7_ff_inst (D_FF_10)    1.89e-07 7.07e-09 8.07e-10 1.96e-07   1.0
      ff_gen_10_ff_inst (D_FF_6)    1.70e-07 7.07e-09 7.80e-10 1.78e-07   0.9
      ff_gen_6_ff_inst (D_FF_11)    1.82e-07 7.07e-09 8.08e-10 1.90e-07   1.0
      ff_gen_5_ff_inst (D_FF_12)    1.95e-07 7.07e-09 8.15e-10 2.03e-07   1.0
      ff_gen_1_ff_inst (D_FF_17)    1.71e-07 7.07e-09 7.95e-10 1.79e-07   0.9
      ff_gen_4_ff_inst (D_FF_13)    1.91e-07 7.07e-09 8.02e-10 1.99e-07   1.0
      ff_gen_0_ff_inst (D_FF_18)    1.49e-07 7.07e-09 7.78e-10 1.57e-07   0.8
      ff_gen_3_ff_inst (D_FF_14)    1.82e-07 7.07e-09 8.11e-10 1.90e-07   1.0
      ff_gen_2_ff_inst (D_FF_15)    1.74e-07 7.07e-09 8.11e-10 1.82e-07   0.9
      ff_gen_15_ff_inst (D_FF_1)    1.24e-07 7.07e-09 7.25e-10 1.32e-07   0.7
      ff_gen_14_ff_inst (D_FF_2)    1.32e-07 7.07e-09 7.25e-10 1.40e-07   0.7
  clk_gate_C21 (SNPS_CLOCK_GATE_HIGH_hw2_pipe_clkgating)
                                    1.69e-07 2.62e-07 7.50e-12 4.31e-07   2.2
  fs (first_stage)                  3.46e-06 9.26e-07 2.11e-08 4.40e-06  22.5
    sub_31_(first_stage_DW01_sub_0) 5.04e-07 2.76e-07 5.90e-09 7.86e-07   4.0
    add_31_(first_stage_DW01_add_0) 4.31e-07 1.57e-07 5.20e-09 5.93e-07   3.0
    dff8 (D_FF_8)                   2.24e-06 3.56e-07 7.27e-09 2.60e-06  13.3
      ff_gen_1_ff_inst (D_FF_25)    2.86e-07 4.84e-08 9.56e-10 3.35e-07   1.7
      ff_gen_0_ff_inst (D_FF_0)     2.79e-07 8.51e-08 9.57e-10 3.65e-07   1.9
      ff_gen_7_ff_inst (D_FF_19)    2.32e-07 6.82e-10 7.55e-10 2.33e-07   1.2
      ff_gen_6_ff_inst (D_FF_20)    2.73e-07 2.80e-08 8.63e-10 3.02e-07   1.5
      ff_gen_5_ff_inst (D_FF_21)    2.95e-07 5.46e-08 9.26e-10 3.50e-07   1.8
      ff_gen_4_ff_inst (D_FF_22)    2.90e-07 4.03e-08 9.09e-10 3.31e-07   1.7
      ff_gen_3_ff_inst (D_FF_23)    2.92e-07 4.84e-08 9.53e-10 3.41e-07   1.7
      ff_gen_2_ff_inst (D_FF_24)    2.93e-07 5.04e-08 9.53e-10 3.45e-07   1.8
1
```

Pipeline:

```
****************************************
Report : Averaged Power
         -hierarchy
Design : hw2_pipe
Version: V-2023.12
Date   : Thu Oct 17 20:49:42 2024
****************************************


                                    Int      Switch   Leak     Total
Hierarchy                           Power    Power    Power    Power    %
------------------------------------------------------------------------------
hw2_pipe                            1.45e-05 5.83e-06 1.74e-07 2.05e-05 100.0
  fs (first_stage)                  3.48e-06 8.99e-07 2.19e-08 4.40e-06  21.5
    sub_23_(first_stage_DW01_sub_0) 5.04e-07 2.76e-07 5.90e-09 7.86e-07   3.8
    add_23_(first_stage_DW01_add_0) 4.31e-07 1.57e-07 5.20e-09 5.93e-07   2.9
    dff8 (D_FF_8)                   2.26e-06 3.29e-07 8.06e-09 2.60e-06  12.7
      ff_gen_7_ff_inst (D_FF_19)    2.32e-07 6.26e-10 7.55e-10 2.33e-07   1.1
      ff_gen_6_ff_inst (D_FF_20)    2.73e-07 3.39e-08 8.63e-10 3.08e-07   1.5
      ff_gen_5_ff_inst (D_FF_21)    2.95e-07 5.17e-08 9.26e-10 3.47e-07   1.7
      ff_gen_1_ff_inst (D_FF_25)    2.86e-07 4.79e-08 9.56e-10 3.35e-07   1.6
      ff_gen_4_ff_inst (D_FF_22)    2.90e-07 4.62e-08 9.09e-10 3.37e-07   1.6
      ff_gen_0_ff_inst (D_FF_0)     2.79e-07 1.44e-08 9.57e-10 2.94e-07   1.4
      ff_gen_3_ff_inst (D_FF_23)    3.17e-07 8.52e-08 1.49e-09 4.03e-07   2.0
      ff_gen_2_ff_inst (D_FF_24)    2.93e-07 4.68e-08 9.53e-10 3.41e-07   1.7
  ss (second_stage)                 1.10e-05 4.94e-06 1.52e-07 1.61e-05  78.5
    mult_34_(second_stage_DW_mult_uns 2)
                                    6.70e-06 4.93e-06 1.38e-07 1.18e-05  57.4
    dff16 (D_FF_16)                 4.32e-06 1.05e-08 1.37e-08 4.34e-06  21.2
      ff_gen_14_ff_inst (D_FF_2)    2.37e-07 4.22e-10 7.55e-10 2.38e-07   1.2
      ff_gen_7_ff_inst (D_FF_10)    2.93e-07 4.22e-10 8.57e-10 2.94e-07   1.4
      ff_gen_1_ff_inst (D_FF_17)    2.76e-07 4.22e-10 8.42e-10 2.77e-07   1.4
      ff_gen_9_ff_inst (D_FF_7)     2.88e-07 4.22e-10 8.42e-10 2.89e-07   1.4
      ff_gen_2_ff_inst (D_FF_15)    2.74e-07 4.22e-10 8.61e-10 2.75e-07   1.3
      ff_gen_11_ff_inst (D_FF_5)    2.67e-07 4.22e-10 7.97e-10 2.68e-07   1.3
      ff_gen_4_ff_inst (D_FF_13)    2.95e-07 4.22e-10 8.54e-10 2.97e-07   1.4
      ff_gen_13_ff_inst (D_FF_3)    2.48e-07 4.22e-10 7.55e-10 2.49e-07   1.2
      ff_gen_6_ff_inst (D_FF_11)    2.83e-07 4.22e-10 8.59e-10 2.84e-07   1.4
      ff_gen_15_ff_inst (D_FF_1)    2.35e-07 4.22e-10 7.55e-10 2.36e-07   1.2
      ff_gen_0_ff_inst (D_FF_18)    2.53e-07 4.22e-10 8.22e-10 2.55e-07   1.2
      ff_gen_8_ff_inst (D_FF_9)     2.83e-07 4.22e-10 8.35e-10 2.84e-07   1.4
      ff_gen_10_ff_inst (D_FF_6)    2.67e-07 4.22e-10 8.23e-10 2.68e-07   1.3
      ff_gen_3_ff_inst (D_FF_14)    2.81e-07 4.22e-10 8.63e-10 2.82e-07   1.4
      ff_gen_12_ff_inst (D_FF_4)    2.45e-07 4.22e-10 7.67e-10 2.46e-07   1.2
      ff_gen_5_ff_inst (D_FF_12)    2.95e-07 4.22e-10 8.69e-10 2.96e-07   1.4
1
```

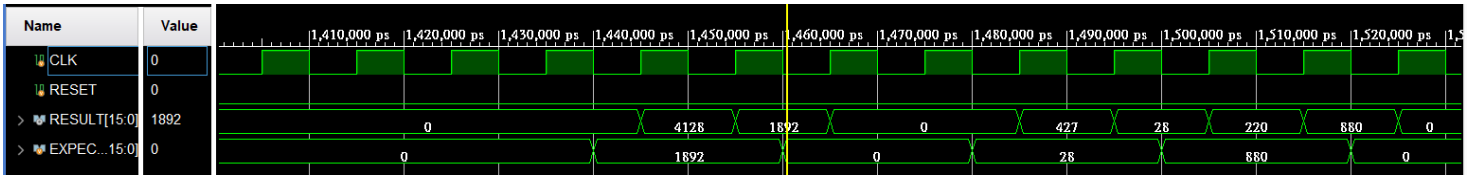
Non-pipeline:

```
****************************************
Report : Averaged Power
         -hierarchy
Design : hw2_nonpipe
Version: V-2023.12
Date   : Thu Oct 17 20:44:40 2024
****************************************


                                    Int      Switch   Leak     Total
Hierarchy                           Power    Power    Power    Power    %
------------------------------------------------------------------------------------
hw2_nonpipe                         3.85e-05 2.79e-05 4.88e-07 6.68e-05 100.0
  mult_10 (hw2_nonpipe_DW_mult_uns_7) 1.33e-05 9.33e-06 1.41e-07 2.27e-05  34.0
  mult_12 (hw2_nonpipe_DW_mult_uns_6) 1.55e-05 1.07e-05 1.75e-07 2.64e-05  39.5
  sub_12 (hw2_nonpipe_DW01_sub_2)   5.10e-06 4.86e-06 1.01e-07 1.01e-05  15.1
  add_10 (hw2_nonpipe_DW01_add_2)   3.54e-06 2.87e-06 6.26e-08 6.48e-06   9.7
1
```

6. Vivado:

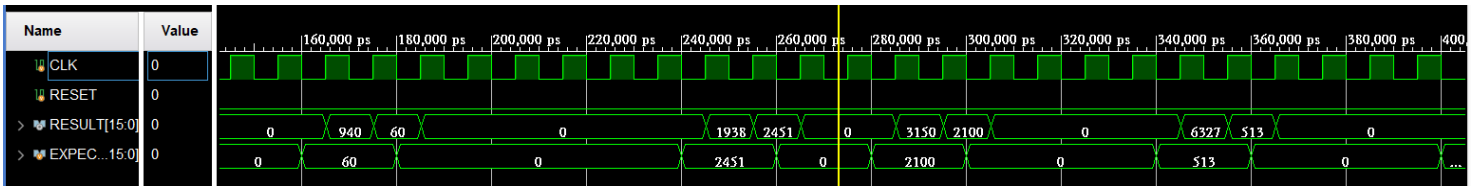
Behavior 波型:



解釋:

結果符合預期

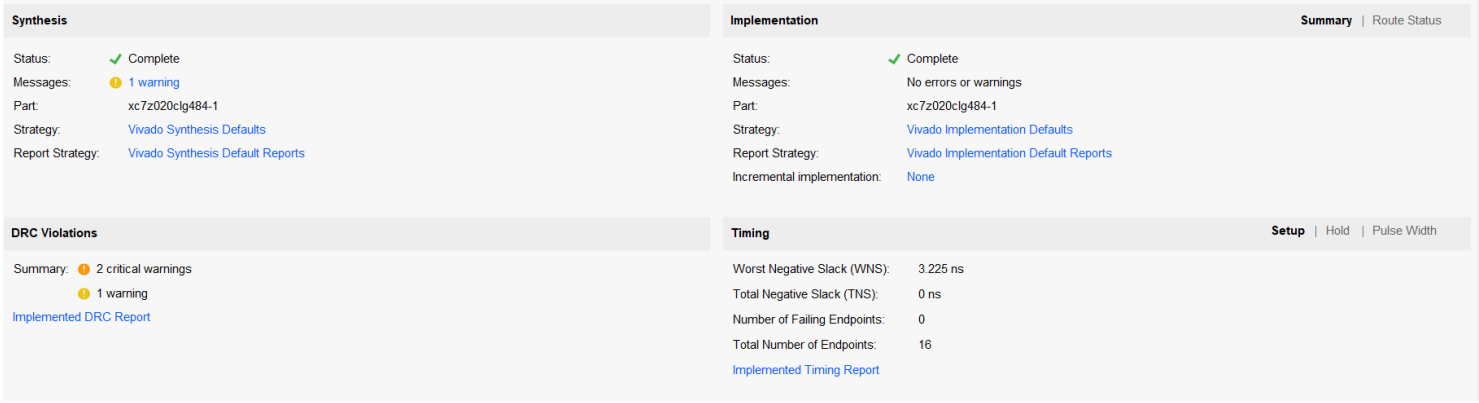
post-implement 波型:

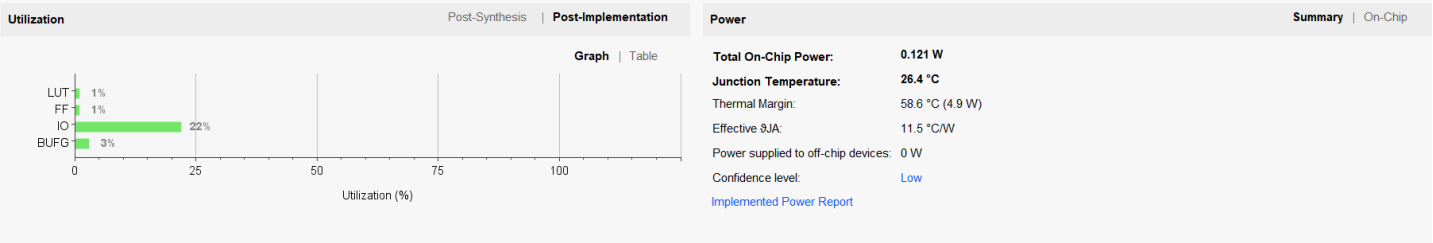


解釋:

結果符合預期

Vivado Summary Overview:





7. 數據表格:

	Area(um^2)			Timing(ns)			Power(mW)		
	CL	SL	Total	Arrival Time	Required time	Slack (MET)	Dynamic	Leakage	Total
Non-pipelined (DC)	411.972486	0.000000	411.972486	0.25	0.25	0	1.8471	494.0559 nW	1.8476
Non-pipelined (PrimeTime)							66.4	0.488	66.88
Pipelined (DC)	171.279364	27.527041	198.806405	0.23	0.23	0	886.5671 uW	177.5667 nW	0.8867
Pipelined (PrimeTime)							20.33	0.17	20.5
Clock-gated (DC)	174.804484	28.200961	203.005445	0.23	0.23	0	916.0278 uW	179.7616 nW	0.9162
Clock-gated (PrimeTime)							19.39	0.17	19.5

8. 心得

這次作業重點在於 Clock gating 省 power，用 Primetime 可以看出。再應用於 FPGA，利用 vivado。流程比第一次作業多了不少，但雖然過程耗時，依然學到了不少 verilog coding、結果分析以及應用於 FPGA 的實用技巧與經驗。