DSLab. 05 Digital Logic Gates & Karnaugh Map

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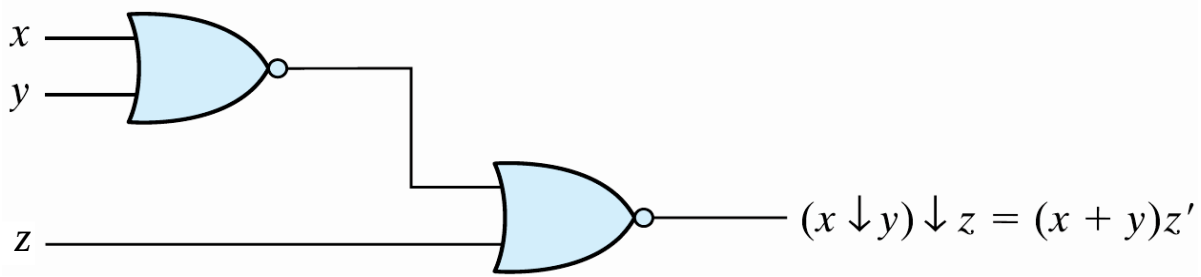
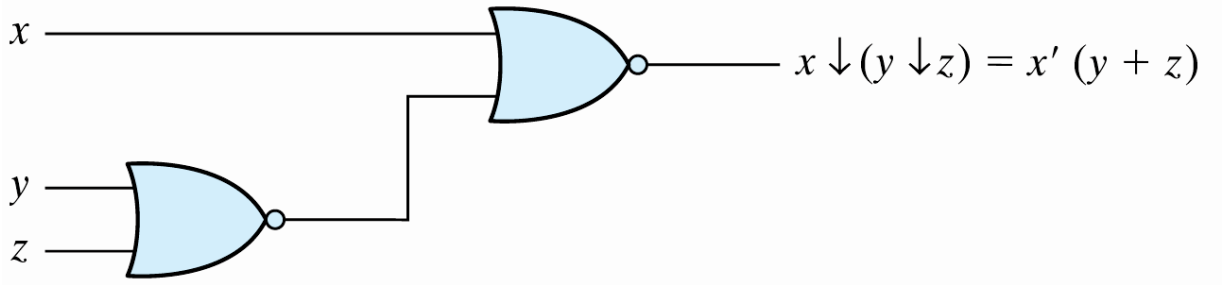
- Design and verify the following circuits using Verilog HDL and Schematic
- Verilog
  - Behavioral level modeling
  - Dataflow modeling
  - Structural level modeling
- Schematic
- Please write and upload the lab report (Lab05) -- Due on 2022/10/07 23:59

Exercise 1

- Derive $(x \downarrow y) \downarrow z = (x + y)z'$, $z \downarrow (y \downarrow x) = z'(y + x)$ and $x \downarrow (y \downarrow z) = x'(y + z)$ (applying DeMorgan's theorem)
- Verify $(x \downarrow y) \downarrow z = z \downarrow (y \downarrow x)$ (using Structural level modeling)
- Verify $(x \downarrow y) \downarrow z \neq x \downarrow (y \downarrow z)$ (using Structural level modeling)





Exercise 2

- XOR is an odd function
- Complete the truth table of four-variable XOR function

  $F(w, x, y, z)$
- $F1 = (w \oplus x) \oplus (y \oplus z)$

  $F2 = w \oplus (x \oplus (y \oplus z))$

  $F3 = w \oplus x \oplus y \oplus z$
- Verify $F1 = F2 = F3$

  (using Structural level modeling)

w	*x*	*y*	*z*	*F*
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Exercise 3

- $F(w, x, y, z) = w'yz' + w'xy + wxz + xyz + wx'y'$
- Draw the Karnaugh map and find all the simplest sum-of-products of *F*
- If the simplest sum-of-products of *F* are *F4*, *F5* and *F6*, verify *F4* = *F5* = *F6* (using Verilog Dataflow modeling)