

## Lab04

實驗主題: Canonical and Standard Forms

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實驗內容: Design and verify circuits using Verilog

### Exercise1

$$F1 = (x+z)(y'z'+yz)$$

F2 = the complement of F1 (using demorgan's law)

Verify  $F1' = F2$  (using dataflow modeling)

推導:  $F1' = [(x+z)(y'z'+yz)]'$

$$F2 = [(x+z)(y'z'+yz)]' = (x+z)' + (y'z'+yz)' = (x'z') + (y+z)(y'+z')$$

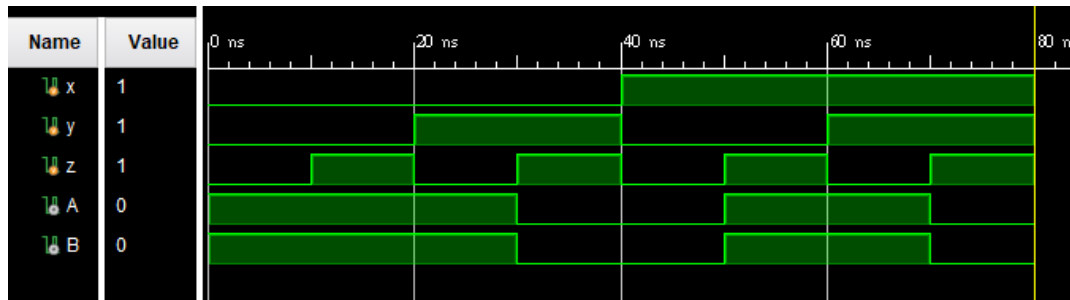
程式碼 for exercise1 (dataflow modeling):

```
module exercise1(A,B,x,y,z);  
    output A,B;  
    input x,y,z;  
  
    assign A = ~( (x|z)&((~y&~z)|(y&z)) );  
    assign B = (~x&~z)|((y|z)&(~y|~z));  
endmodule
```

Testbench for exercise1:

```
module tb;  
    reg x;  
    reg y;  
    reg z;  
    wire A;  
    wire B;  
    exercise1 uut(.x(x),.y(y),.z(z),.A(A),.B(B));  
    initial begin  
        x=1'b0; y=1'b0; z=1'b0;#10  
        x=1'b0; y=1'b0; z=1'b1;#10  
        x=1'b0; y=1'b1; z=1'b0;#10  
        x=1'b0; y=1'b1; z=1'b1;#10  
        x=1'b1; y=1'b0; z=1'b0;#10  
        x=1'b1; y=1'b0; z=1'b1;#10  
        x=1'b1; y=1'b1; z=1'b0;#10  
        x=1'b1; y=1'b1; z=1'b1;#10  
        $finish;  
    end  
endmodule
```

波形圖(結果):



Exercise1 實驗結果與分析:

F1 & F2 的波型相同

Exercise2

Find and show the sum of minterms (F3) of the following truth table

Find and show the product of maxterms (F4) of the following truth table

Truth table:

w	x	y	z	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Verify F3=F4(using structural level modeling)

推導:

$$F3 = w'x'y'z + w'x'yz' + w'xyz + wx'y'z + wxy'z' + wxyz' + wxyz$$

$$F4 = (w+x+y+z)(w+x'+y+z)(w+x'+y+z')(w+x'+y'+z')(w'+x+y+z)(w'+x+y+z')(w'+x+y'+z)(w'+x'+y+z')$$

程式碼 for exercise2:

```

module exercise_2(A,B,w,x,y,z);
    output A,B;
    input w,x,y,z;
    wire n1,n2,n3,n4,n5,n6,n7,n8,n9,n10,n11,n12,n13,n14,n15,n16,n17,n18,n19,n20;

    not(n1,w);
    not(n2,x);
    not(n3,y);
    not(n4,z);

    and(n5,n1,n2,n3,z);
    and(n6,n1,n2,y,n4);
    and(n7,n1,n2,y,z);
    and(n8,n1,x,y,n4);
    and(n9,w,n2,y,z);
    and(n10,w,x,n3,n4);
    and(n11,w,x,y,n4);
    and(n12,w,x,y,z);
    or(A,n5,n6,n7,n8,n9,n10,n11,n12);

    or(n13,w,x,y,z);
    or(n14,w,n2,y,z);
    or(n15,w,n2,y,n4);
    or(n16,w,n2,n3,n4);
    or(n17,n1,x,y,z);
    or(n18,n1,x,y,n4);
    or(n19,n1,x,n3,z);
    or(n20,n1,n2,y,n4);
    and(B,n13,n14,n15,n16,n17,n18,n19,n20);

endmodule

```

## Testbench for exercise2:

```

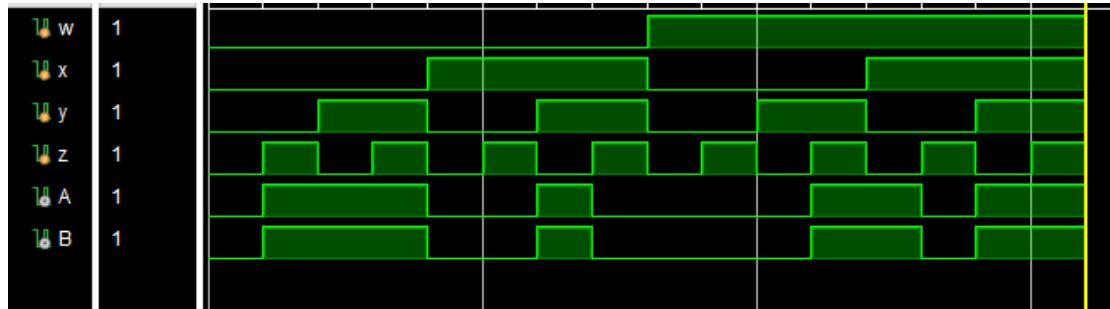
module testbench;
    reg w;
    reg x;
    reg y;
    reg z;
    wire A;
    wire B;
    exercise_2 uut(.w(w),.x(x),.y(y),.z(z),.A(A),.B(B));
    initial begin

        w=1'b0; x=1'b0; y=1'b0; z=1'b0;#10
        w=1'b0; x=1'b0; y=1'b0; z=1'b1;#10
        w=1'b0; x=1'b0; y=1'b1; z=1'b0;#10
        w=1'b0; x=1'b0; y=1'b1; z=1'b1;#10
        w=1'b0; x=1'b1; y=1'b0; z=1'b0;#10
        w=1'b0; x=1'b1; y=1'b0; z=1'b1;#10
        w=1'b0; x=1'b1; y=1'b1; z=1'b0;#10
        w=1'b0; x=1'b1; y=1'b1; z=1'b1;#10
        w=1'b1; x=1'b0; y=1'b0; z=1'b0;#10
        w=1'b1; x=1'b0; y=1'b0; z=1'b1;#10
        w=1'b1; x=1'b0; y=1'b1; z=1'b0;#10
        w=1'b1; x=1'b0; y=1'b1; z=1'b1;#10
        w=1'b1; x=1'b1; y=1'b0; z=1'b0;#10
        w=1'b1; x=1'b1; y=1'b0; z=1'b1;#10
        w=1'b1; x=1'b1; y=1'b1; z=1'b0;#10
        w=1'b1; x=1'b1; y=1'b1; z=1'b1;#10

    $finish;
    end
endmodule

```

波形圖:



Exercise2 實驗結果與分析:

F3 & F4 的波型相同

Exercise3

$$F5(x, y, z) = x + z'$$

Find and show the canonical forms of F5, i.e., the sum of minterms (F6) and the product of maxterms (F7)

Verify  $F5 = F6 = F7$  (using structural level modeling)

推導:

$$F5 = x + z'$$

$$F6 = x(y + y')(z + z') + (x + x')(y + y')z' = xyz + xyz' + xy'z + xy'z' + x'yz + x'yz' + x'y'z + x'y'z'$$

$$F7 = (x + z') + yy' = [(x + z') + y][(x + z') + y'] = (x + y + z')(x + y' + z')$$

程式碼 for exercise3:

```
module e3(A,B,C,x,y,z);
    output A,B,C;
    input x,y,z;
    wire n1,n2,n3,n4,n5,n6,n7,n8,n9,n10,n11,n12,n13;
    not(n1,x);
    not(n2,y);
    not(n3,z);
    or(A,x,n3);

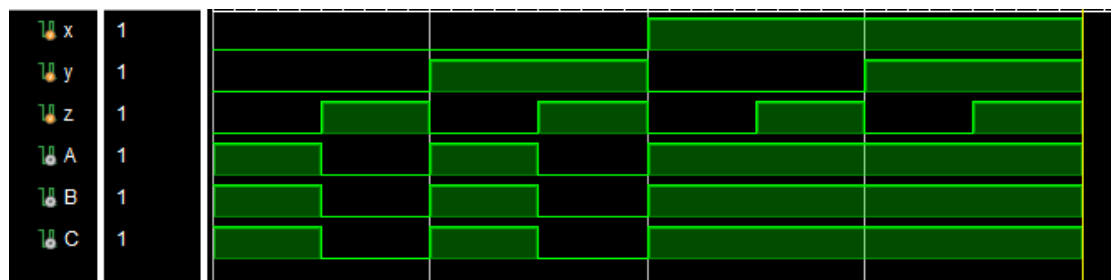
    and(n4,x,y,z);
    and(n5,x,y,n3);
    and(n6,x,n2,z);
    and(n7,x,n2,n3);
    and(n8,x,y,n3);
    and(n9,n1,y,n3);
    and(n10,x,n2,n3);
    and(n11,n1,n2,n3);
    or(B,n4,n5,n6,n7,n8,n9,n10,n11);

    or(n12,x,y,n3);
    or(n13,x,n2,n3);
    and(C,n12,n13);
endmodule
```

Testbench for exercise3:

```
module tb;
    reg x;
    reg y;
    reg z;
    wire A;
    wire B;
    wire C;
    e3 UUT(.x(x),.y(y),.z(z),.A(A),.B(B),.C(C));
    initial begin
        x=1'b0; y=1'b0; z=1'b0;#10
        x=1'b0; y=1'b0; z=1'b1;#10
        x=1'b0; y=1'b1; z=1'b0;#10
        x=1'b0; y=1'b1; z=1'b1;#10
        x=1'b1; y=1'b0; z=1'b0;#10
        x=1'b1; y=1'b0; z=1'b1;#10
        x=1'b1; y=1'b1; z=1'b0;#10
        x=1'b1; y=1'b1; z=1'b1;#10
    $finish;
    end
endmodule
```

波形圖:



Exercise3 實驗結果與分析:

F5 & F6 & F7 的波型相同

### 實驗心得

這次實驗比上次順利許多。上次因為還不熟悉 verilog 跟 vivado，所以常常出現操作順序搞錯或是程式碼跟 testbench 東錯西錯的情形。相較於上次，這次的習題出現了一些比較需要先自己推導 minterm 或 maxterm 及 SOP 或 POS 表示法的練習，在實作過程中我對於這些表示法又更熟悉了一些。雖說這次實作過程比上次順利許多，但其中還是發生了一點小失誤，可以做為實作經驗。像是 testbench 中在設定每個不同輸入的排列組合之間，要記得加上#10 的指令，讓每種組合之間有間隔時間，才不會導致波形圖中都只有 testbench 中最後一個輸入組合的波型。