DSLab. 09 Adders

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- Design and Verify the following circuits using Verilog HDL and Schematic
- Verilog
  - Behavioral level modeling
  - Dataflow modeling
  - Structural level (Gate-level) modeling
- Schematic
- Please write and upload the lab report (Lab09) -- Due on 2022/11/04 23:59

Behavioral level Description of 4-bit Adder

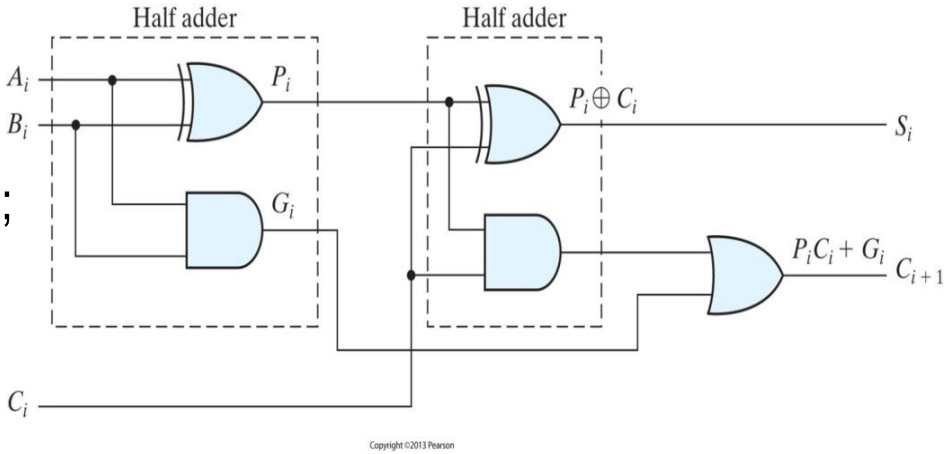
```
// Behavioral level description of 4-bit adder
module r_4_bit_bl (C_out, Sum, A, B, C_in);
   output  C_out;
   output [3:0]  Sum;
   input [3:0]  A, B;
   input  C_in;
   reg C_out;
   reg [3:0]  Sum;

   always @(A or B or C_in)
       {C_out, Sum} = A + B + C_in;

endmodule
```

Dataflow Description of 4-bit Adder

```
// Dataflow description of 4-bit adder
module adder_4_bit_df (
    output [3:0]        Sum,
    output              C_out,
    input [3: 0]        A, B,
    input C_in
    );
     assign {C_out, Sum} = A + B + C_in;
endmodule
```

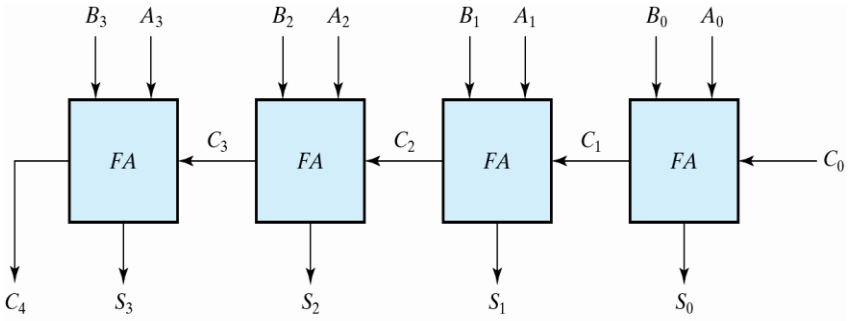
Gate-level Description of 4-bit Ripple-Carry Adder

```
module half_adder (output S, C, input x, y);
   xor (S, x, y);
   and (C, x, y);
endmodule
```



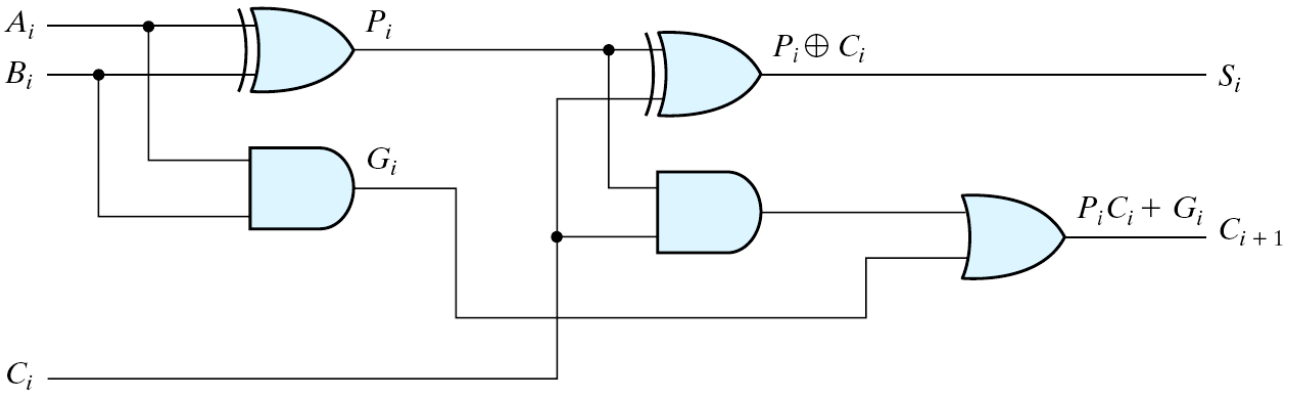

```
module full_adder (output S, C, input x, y, z);
   wire     S1, C1, C2;
   half_adder HA1 (S1, C1, x, y);
   half_adder HA2 (S, C2, S1, z);
   or G1 (C, C2, C1);
endmodule
```

```
module ripple_carry_4_bit_adder ( output [3: 0] Sum, output C4, input [3:0]  A, B, input C0);
    wire          C1, C2, C3;      // Intermediate carries

    full_adder    FA0 (Sum[0], C1, A[0], B[0], C0),
                  FA1 (Sum[1], C2, A[1], B[1], C1),
                  FA2 (Sum[2], C3, A[2], B[2], C2),
                  FA3 (Sum[3], C4, A[3], B[3], C3);
endmodule
```



Exercise 1: 8-bit Carry-look Ahead Adder (1/3)

- Design and verify the 8-bit carry-look ahead adder composed of two 4-bit carry-look ahead adders (using Verilog Structural level modeling)
  - carry propagate: $P_i = A_i \oplus B_i$, carry generate: $G_i = A_i B_i$
  - sum: $S_i = P_i \oplus C_i$, carry: $C_{i+1} = G_i + P_i C_i$
  - $C_1 = G_0 + P_0 C_0$
  - $C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0$
  - $C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$
  - $C_4 = G_3 + P_3 C_3 = \ldots$



Exercise 1: 8-bit Carry-look Ahead Adder (2/3)

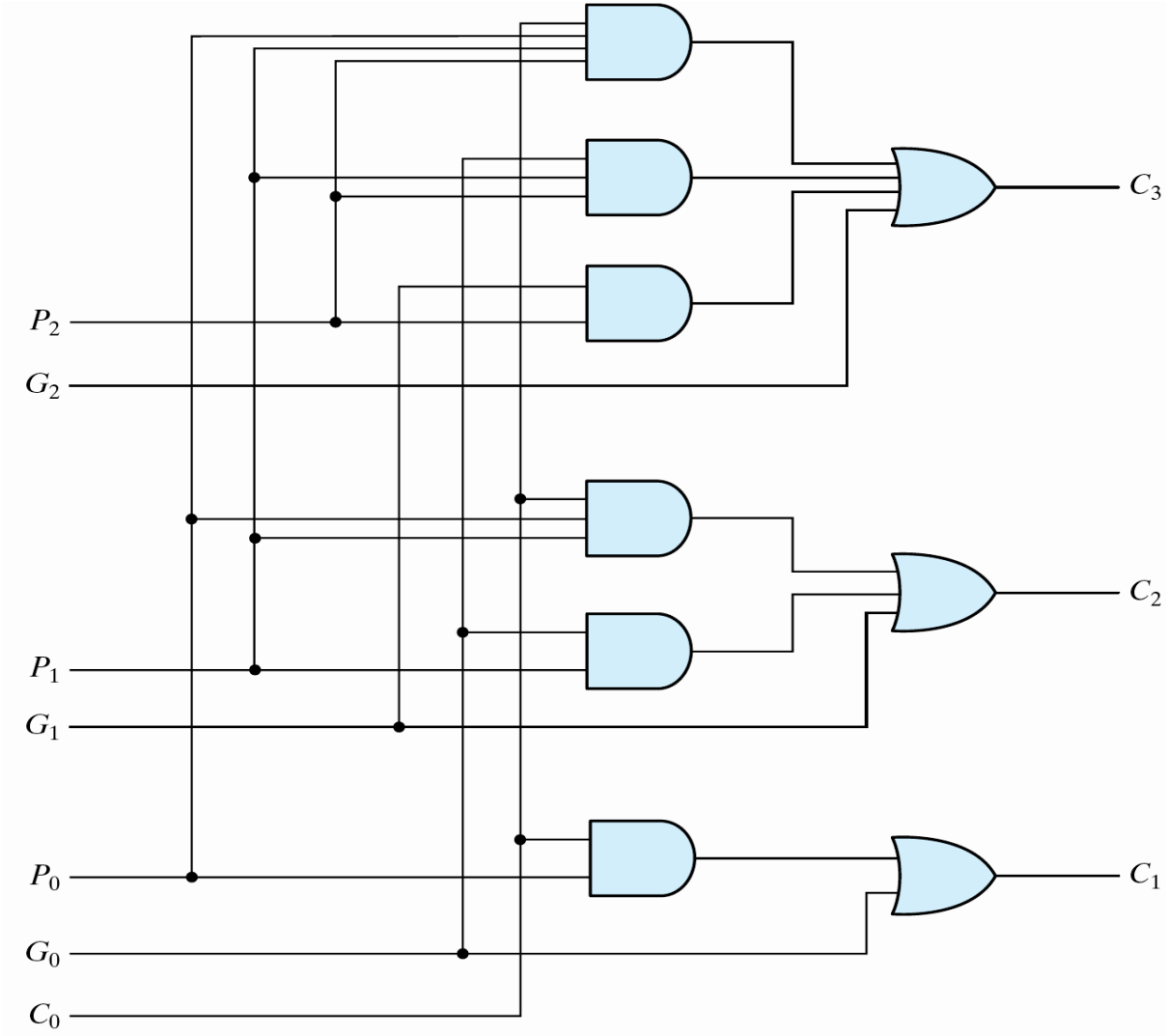
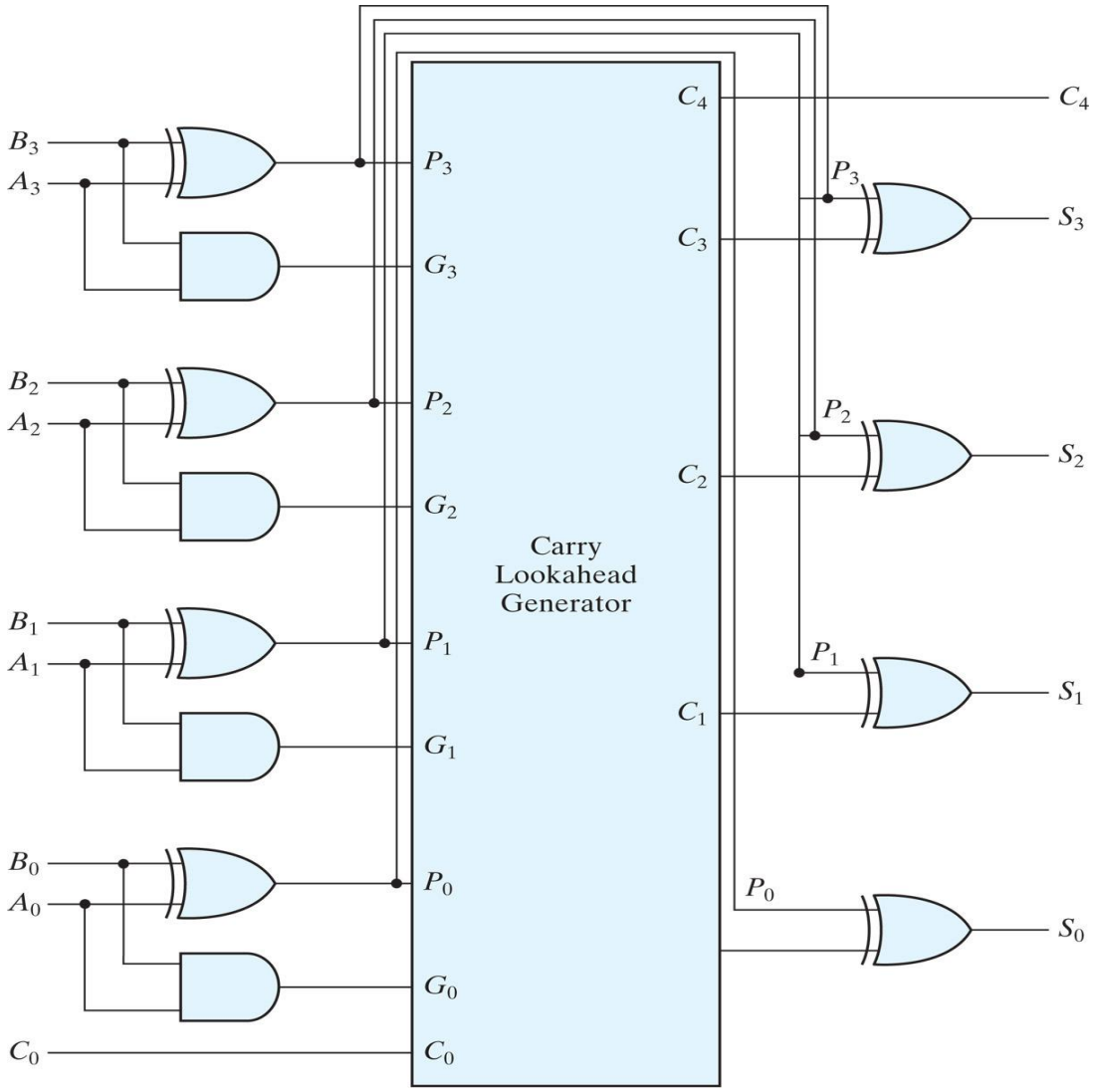


Fig. 4-11 Logic Diagram of Carry Lookahead Generator

Exercise 1: 8-bit Carry-look Ahead Adder (3/3)



Exercise 2: Decimal Adder (1/2)

- Design and verify the 2-digit decimal adder

32 + 41 = 073
25 + 57 = 082
86 + 79 = 165

$C = K + Z_8Z_4 + Z_8Z_2$

$C = 1 \Rightarrow +6$

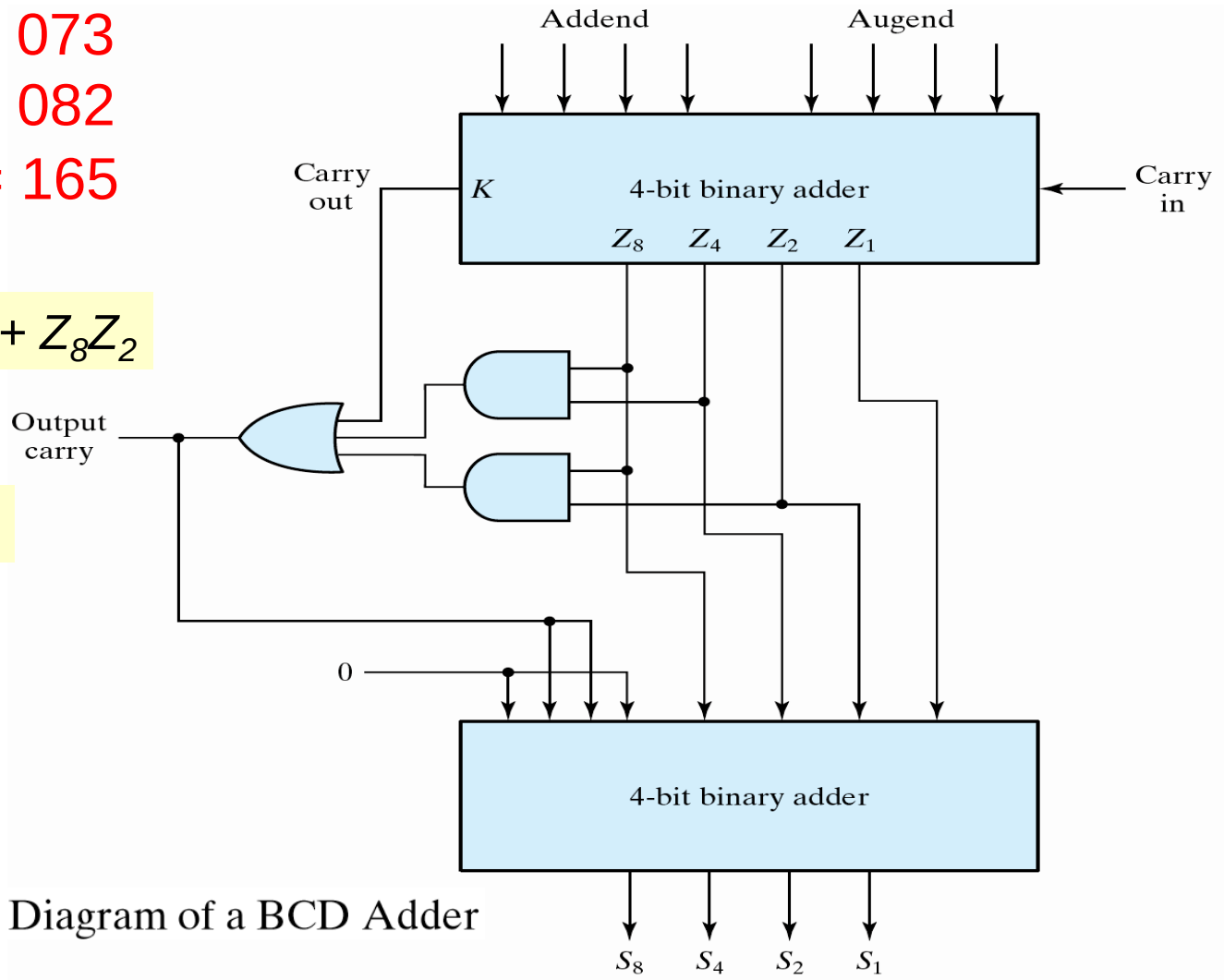


Fig. 4-14 Block Diagram of a BCD Adder

Exercise 2: Decimal Adder (2/2)

Table 4.5
Derivation of BCD Adder

Binary Sum						BCD Sum					Decimal
K	Z_8	Z_4	Z_2	Z_1		C	S_8	S_4	S_2	S_1	
0	0	0	0	0		0	0	0	0	0	0
0	0	0	0	1		0	0	0	0	1	1
0	0	0	1	0		0	0	0	1	0	2
0	0	0	1	1		0	0	0	1	1	3
0	0	1	0	0		0	0	1	0	0	4
0	0	1	0	1		0	0	1	0	1	5
0	0	1	1	0		0	0	1	1	0	6
0	0	1	1	1		0	0	1	1	1	7
0	1	0	0	0		0	1	0	0	0	8
0	1	0	0	1		0	1	0	0	1	9
0	1	0	1	0		1	0	0	0	0	10
0	1	0	1	1		1	0	0	0	1	11
0	1	1	0	0		1	0	0	1	0	12
0	1	1	0	1	+6	1	0	0	1	1	13
0	1	1	1	0	⇒	1	0	1	0	0	14
0	1	1	1	1		1	0	1	0	1	15
1	0	0	0	0		1	0	1	1	0	16
1	0	0	0	1		1	0	1	1	1	17
1	0	0	1	0		1	1	0	0	0	18
1	0	0	1	1		1	1	0	0	1	19