Lab13

實驗主題: Design of Synchronous Sequential Logic

實驗日期:2022/11/28

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實驗內容: Design and Verify the following circuits using Verilog HDL

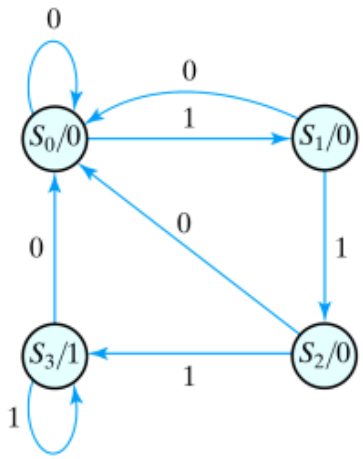


Table 5.11
State Table for Sequence Detector

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Exercise1:

Design a sequence detector to detect a sequence of three or more consecutive 1's in a string of bits coming through an input line (with D F/Fs)

Code:

Behavioral model

```
module ex1_beh(
    output y,
    input x,clock,reset
);
    reg[1:0] state;
    parameter S0 = 2'b00,S1=2'b01,S2=2'b10,S3=2'b11;
    always @(posedge clock,negedge reset)
        if(reset==0)    state<=S0;
        else case(state)
            S0:if(x)    state<=S1; else state<=S0;
            S1:if(x)    state<=S2; else state<=S0;
            S2:if(x)    state<=S3; else state<=S0;
            S3:if(x)    state<=S3;  else state<=S0;
            endcase
   assign y = (state==S3);
endmodule
```

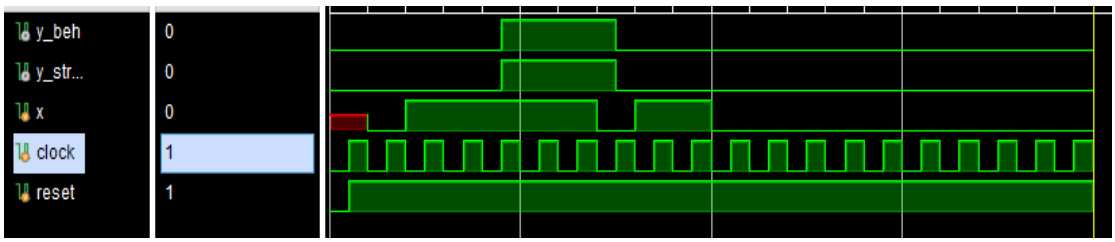
Structural model

```
module DFF(Q,Q_b,D,Clk,reset);
    output Q,Q_b;
    input D,Clk,reset;
    wire n1,n2,n3,n4;
    nand(n1,n4,n2);
    nand(n2,Clk,n1,reset);
    nand(n3,n2,Clk,n4);
    nand(n4,n3,D,reset);
    nand(Q,n2,Q_b);
    nand(Q_b,n3,Q,reset);
endmodule
module e1_struc(
    output y,
    input x,clock,reset
);
    wire A,B,A_b,B_b,n1,n2,n3,n4,DA,DB;
    and(n1,x,B);
    and(n2,x,A);
    and(n3,x,B_b);
    and(n4,x,A);
    or(DA,n1,n2);
    or(DB,n3,n4);
    DFF one(A,A_b,DA,clock,reset);
    DFF two(B,B_b,DB,clock,reset);
    and(y,A,B);
endmodule
```

Testbench:

```
module tb;
wire y_beh, y_struc;
reg x, clock, reset;
e1_beh U0 (.y(y_beh), .x(x), .clock(clock), .reset(reset));
e1_struc UUT (.y(y_struc), .x(x), .clock(clock), .reset(reset));
initial #200 $finish;
initial begin clock=0;forever#5 clock=~clock;end
initial fork
reset = 0;
clock = 0;
#5  reset=1;
#10 x=0;
#20 x=1;
#30 x=1;
#40 x=1;
#50 x=1;
#60 x=1;
#70 x=0;
#80 x=1;
#90 x=1;
#100 x=0;
join
endmodule
```

波形圖:



Exercise1 實驗結果與分析:

功能正確，且兩種寫法輸出相同。

Exercise2:

Design a sequence detector to detect a sequence of three or more consecutive 1's in a string of bits coming through an input line(with T F/Fs)

Code:

Behavioral model

```
module e2_beh(
    output y,
    input x,clock,reset
);
    reg[1:0] state;
    parameter S0 = 2'b00,S1=2'b01,S2=2'b10,S3=2'b11;
    always @(posedge clock,negedge reset)
        if(reset==0)    state<=S0;
        else case(state)
            S0:if(x)    state<=S1; else state<=S0;
            S1:if(x)    state<=S2; else state<=S0;
            S2:if(x)    state<=S3; else state<=S0;
            S3:if(x)    state<=S3;  else state<=S0;
            endcase
   assign y = (state==S3);
endmodule
```

Structural model

```
module DFF(Q,Q_b,D,Clk,reset);
    output Q,Q_b;
    input D,Clk,reset;
    wire n1,n2,n3,n4;
    nand(n1,n4,n2);
    nand(n2,Clk,n1,reset);
    nand(n3,n2,Clk,n4);
    nand(n4,n3,D,reset);
    nand(Q,n2,Q_b);
    nand(Q_b,n3,Q,reset);
endmodule
module TFF(Q,Q_b,T,Clk,reset);
    output Q,Q_b;
    input T,Clk,reset;
    wire n1;
    xor(n1,T,Q);
    DFF one(Q,Q_b,n1,Clk,reset);
endmodule
```

```
module e2_struc(
    output y,
    input x,clock,reset
);
    wire A,B,A_b,B_b,x_b,n1,n2,n3,n4,n5,TA,TB;
    not(x_b,x);
    and(n1,x_b,A);
    and(n2,x,A_b,B);
    and(n3,x_b,B);
    and(n4,x,A_b);
    and(n5,x,B_b);
    or(TA,n1,n2);
    or(TB,n3,n4,n5);
    TFF one(A,A_b,TA,clock,reset);
    TFF two(B,B_b,TB,clock,reset);
    and(y,A,B);
endmodule
```

Testbench:

```
module tb;
wire y_beh, y_struc;
reg x, clock, reset;
e2_beh U0 (.y(y_beh), .x(x), .clock(clock), .reset(reset));
e2_struc UUT (.y(y_struc), .x(x), .clock(clock), .reset(reset));
initial #200 $finish;
initial begin clock=0;forever#5 clock=~clock;end
initial fork
reset = 0;
clock = 0;
#5  reset=1;
#10 x=0;
#20 x=1;
#30 x=1;
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#50 x=1;
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#70 x=0;
#80 x=1;
#90 x=1;
#100 x=0;
join
endmodule
```
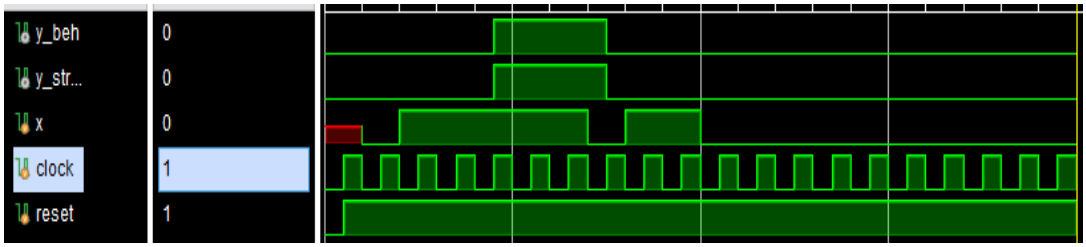

波形圖:



Exercise2 實驗結果與分析:

功能正確，且兩種寫法輸出相同。

實驗心得

這次的實驗跟上周很類似，但這次 structural 的電路要自己依照 F/F 的特性畫出來，除此之外都跟上周一樣。