DSLab. 11 D Latch and D Flip-Flops

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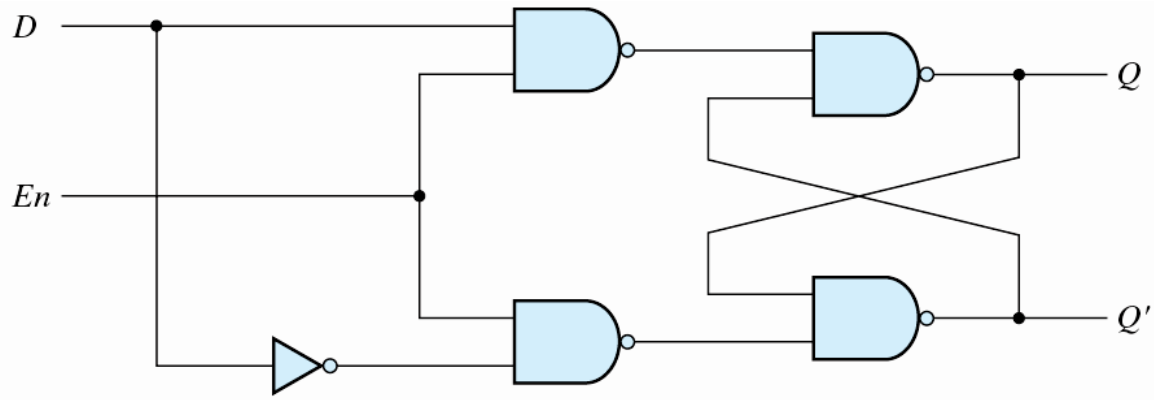
- Design and Verify the following circuits using Verilog HDL
  - D Latch
  - D Flip-Flops
- Verilog
  - Behavioral level modeling
  - Dataflow modeling
  - Structural level (Gate-level) modeling
- Please write and upload the lab report (Lab11) -- Due on 2022/11/18 23:59

Behavioral Description of D Latch

```
module D_latch (Q, D, En);
   output   Q;
   input    D, En;
   reg      Q;

  always @ (En, D)
     if (En) Q <= D;          // Alternative: if (En == 1) Q <= D;
endmodule
```



(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	*Q* = 0; reset state
1	1	*Q* = 1; set state

(b) Function table

Fig. 5.6 *D* latch

Behavioral Description of D Flip-Flop

```
module D_flip_flop (Q, D, Clk);
   output    Q;
   input     D, Clk;
   reg       Q;

  always @ (negedge Clk)
      Q <= D;
endmodule
```

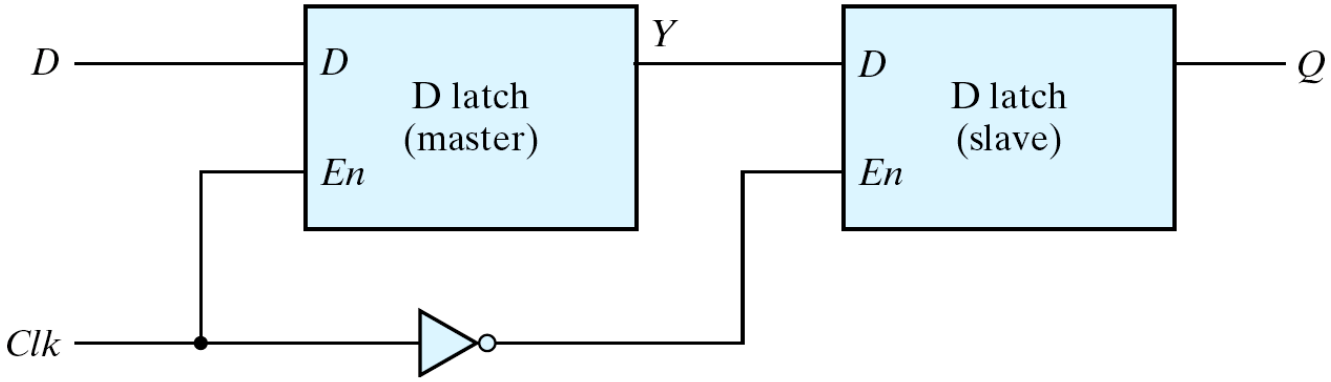


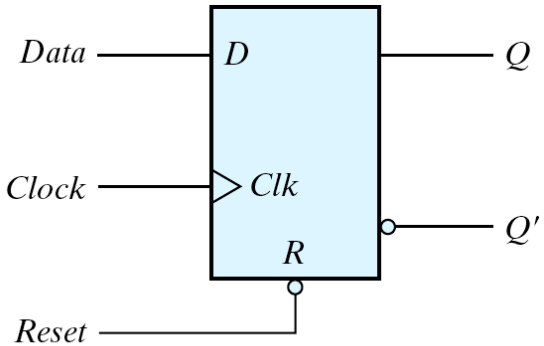
Fig. 5.9 Master-slave *D* flip-flop

D Flip-Flop with asynchronous reset (1/2)

Behavioral Description of D Flip-Flop with asynchronous reset

```
module D_flip_flop_AR_b (Q, Q_b, D, Clk, rst);
   output  Q, Q_b;
   input    D, Clk, rst;
   reg      Q;

   assign   Q_b = ~Q;
   always @ (posedge Clk, negedge rst)
      if (rst == 0) Q <= 1'b0;
      else Q <= D;
endmodule
```



(b) Graphic symbol

R	Clk	D	Q	Q′
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

D Flip-Flop with asynchronous reset (2/2)

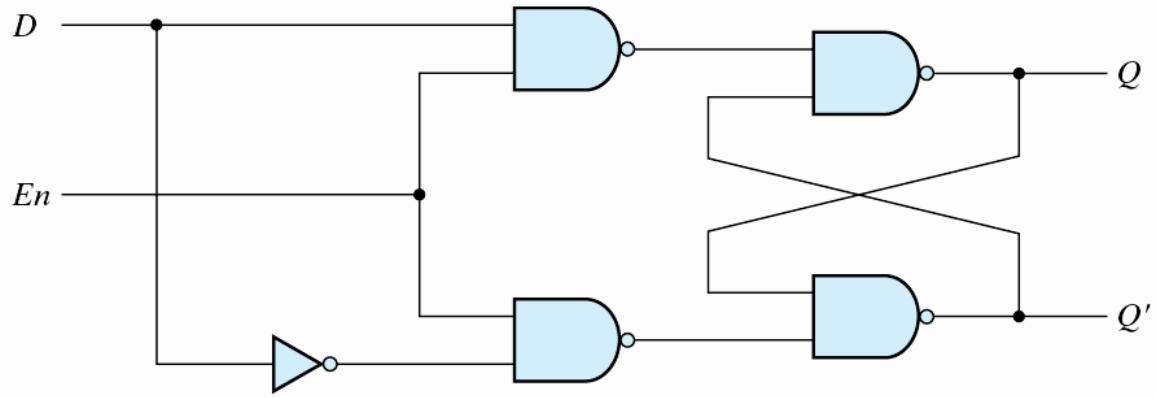
```
module t_D_flip_flops;
    wire  Q, Q_b;
    reg   D, Clk, rst;

    D_flip_flop_AR_b M0 (Q, Q_b, D, Clk, rst);

    initial #100 $finish;
    initial begin Clk = 0; forever #5 Clk = ~Clk; end
    initial fork
      D = 1;
      rst = 1;
      #20 D = 0;
      #40 D = 1;
      #50 D = 0;
      #60 D = 1;
      #70 D = 0;
      #90 D = 1;
      #42 rst = 0;
      #72 rst = 1;
    join
endmodule
```

Exercise 1: D Latch

- Design and verify the D latch using Verilog HDL
  - Structural level (Gate-level) modeling



(a) Logic diagram

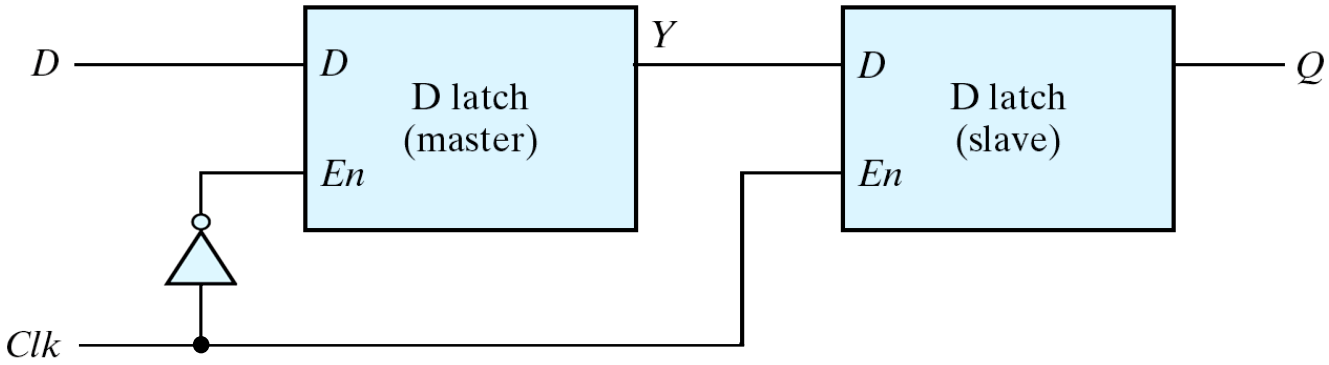
En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

Fig. 5.6 *D* latch

Exercise 2: Master-slave D Flip-Flop

- Design and verify the positive-edge-triggered master-slave D flip-flop using Verilog HDL
  - Structural level (Gate-level) modeling



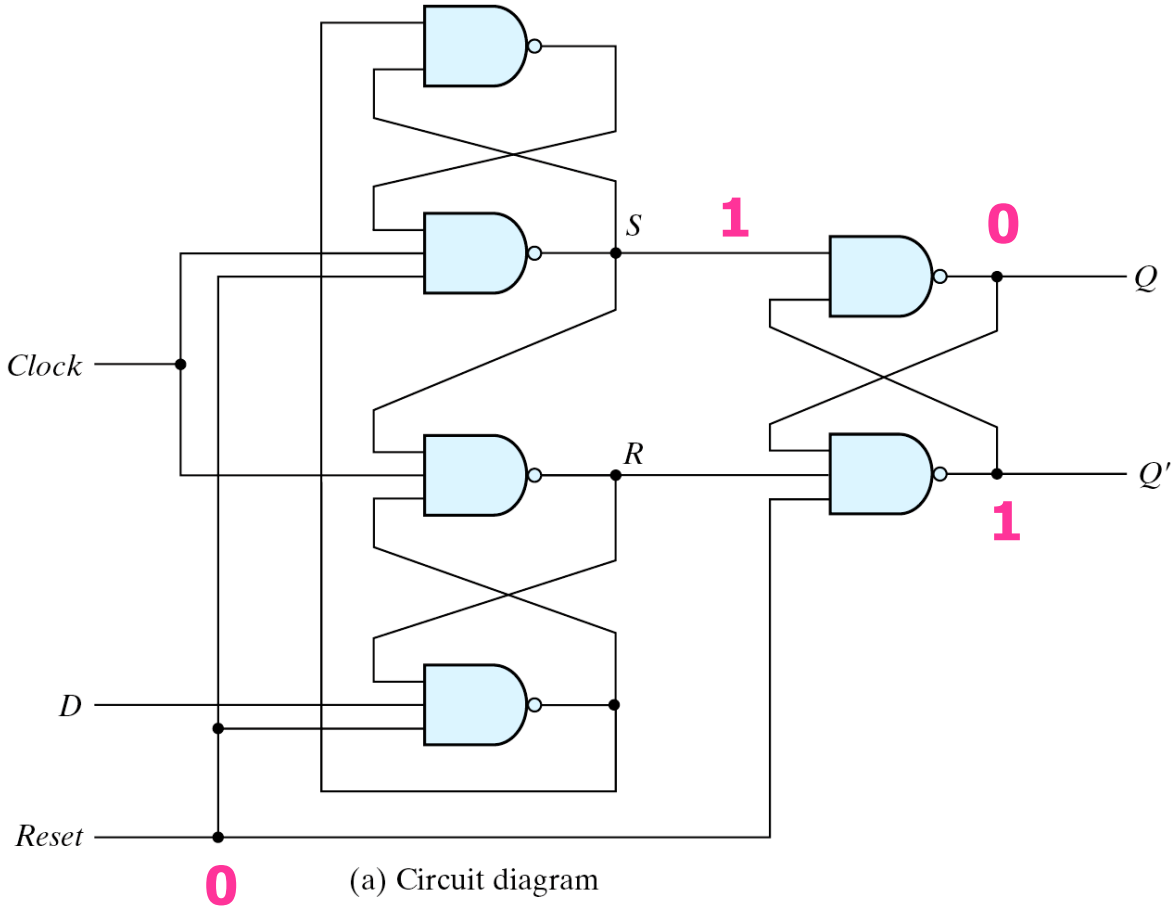
Clk	*D*	*Q*	*Q'*
↑	0	0	1
↑	1	1	0

(b) Function table

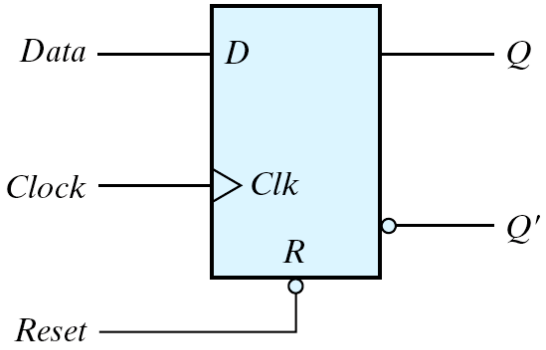
Fig. Positive-edge-triggered master-slave *D* flip-flop

Exercise 3: D flip-flop with asynchronous reset

- Design and verify the *D* flip-flop with asynchronous reset shown in Fig. 5.14 using Verilog HDL (Gate-level modeling)



(a) Circuit diagram



(b) Graphic symbol

R	*Clk*	*D*	*Q*	*Q'*
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Fig. 5.14 *D* flip-flop with asynchronous reset