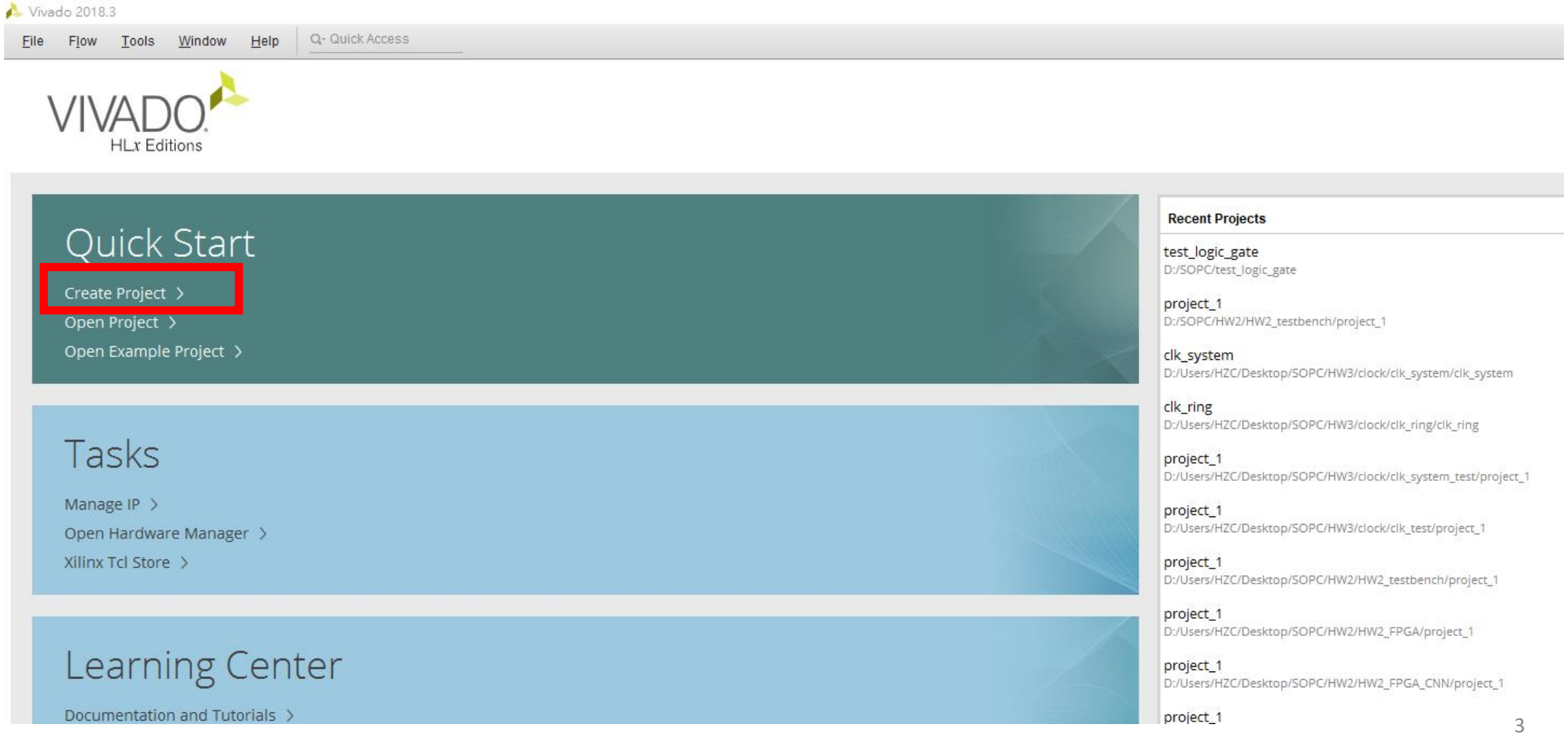
Introduction of Vivado

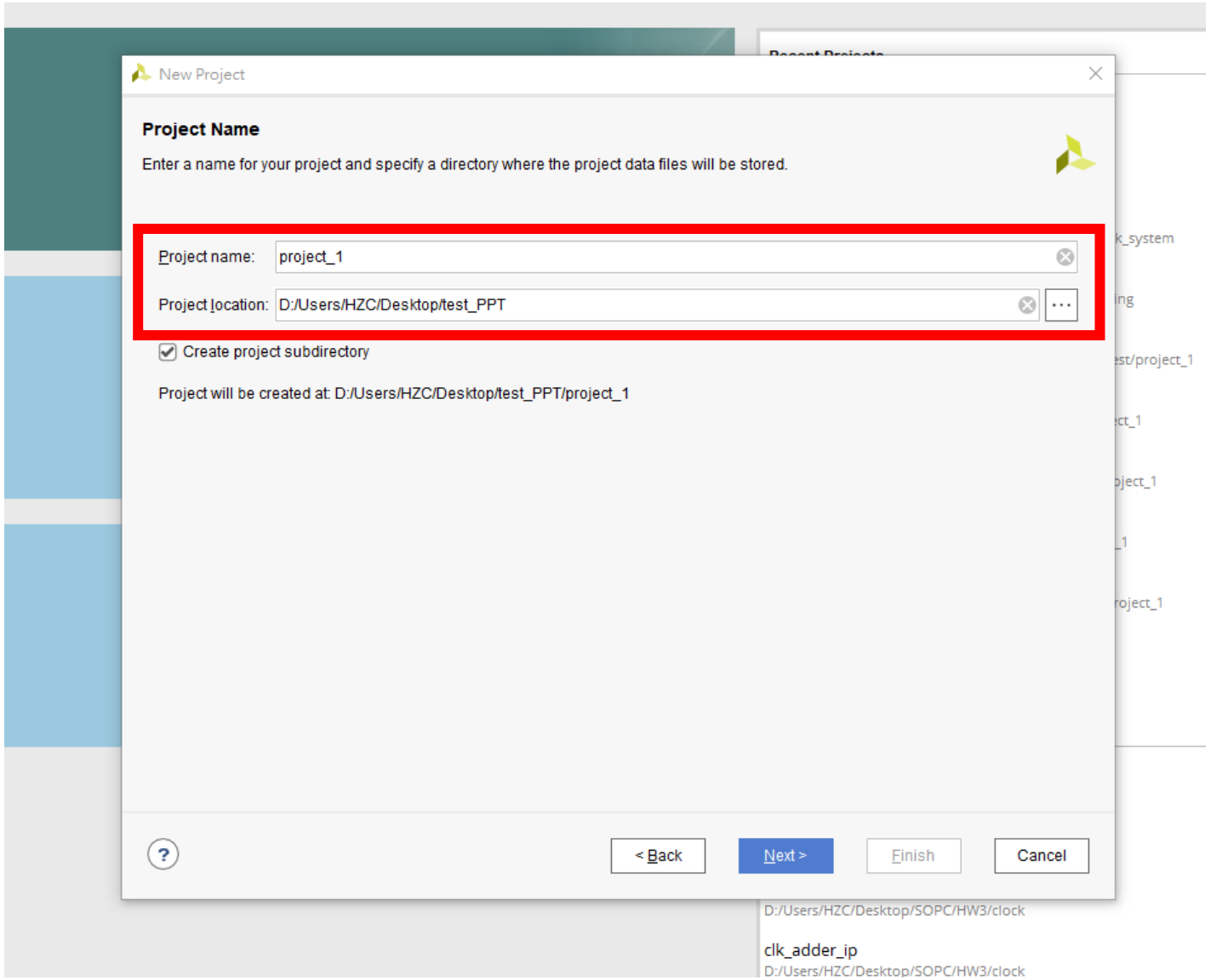
Open Vivado


中山資工署修
新生基本資料.xlsx
國立中山大學學生出差申...
ML.rar
SOPC
Vivado 2018.3
GeForce Experience
test_qt
noise2nois...
Noise2N...
Toeic
IOT智慧大平台

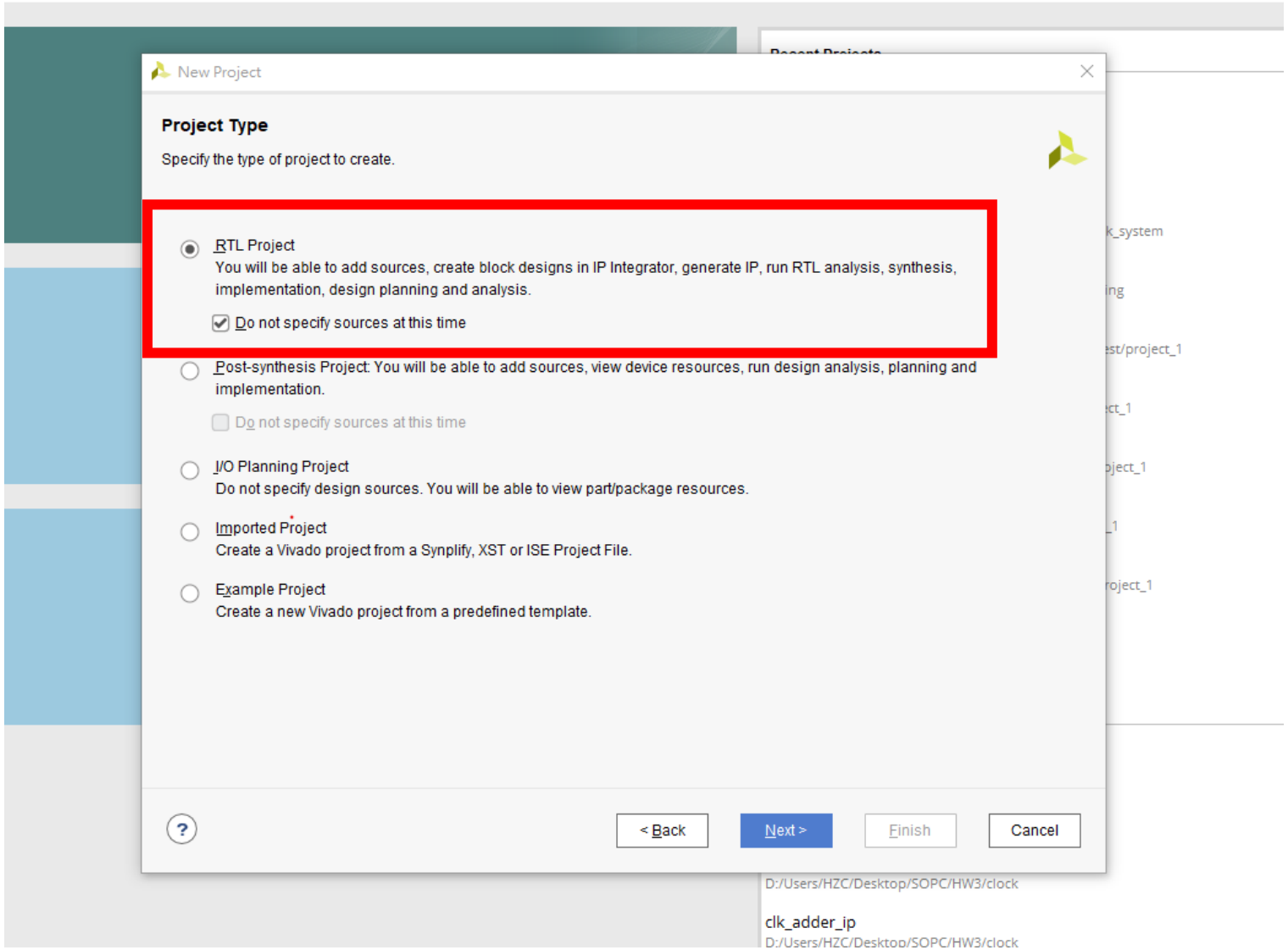
1-1、Create a new project



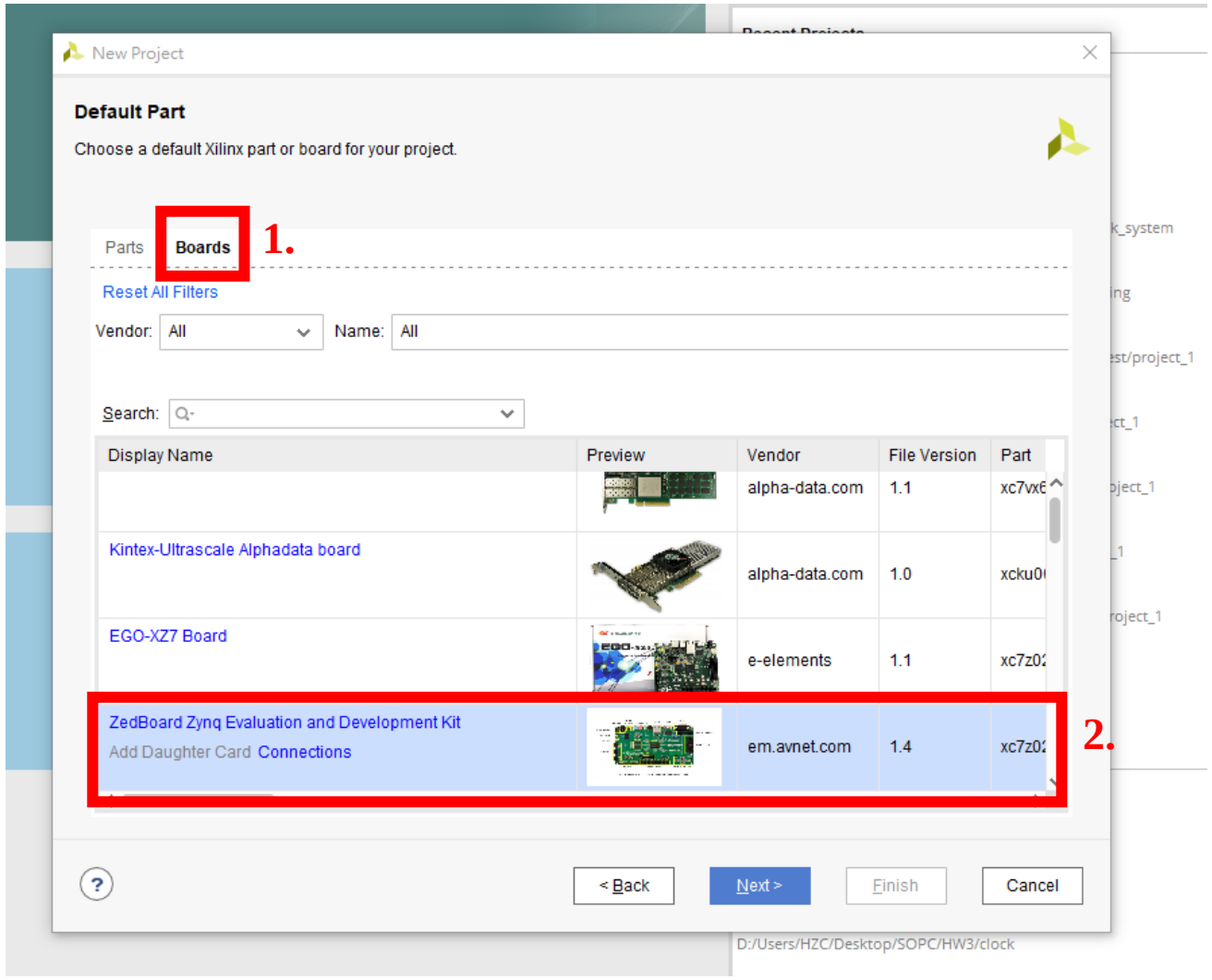
1-2、Create a new project



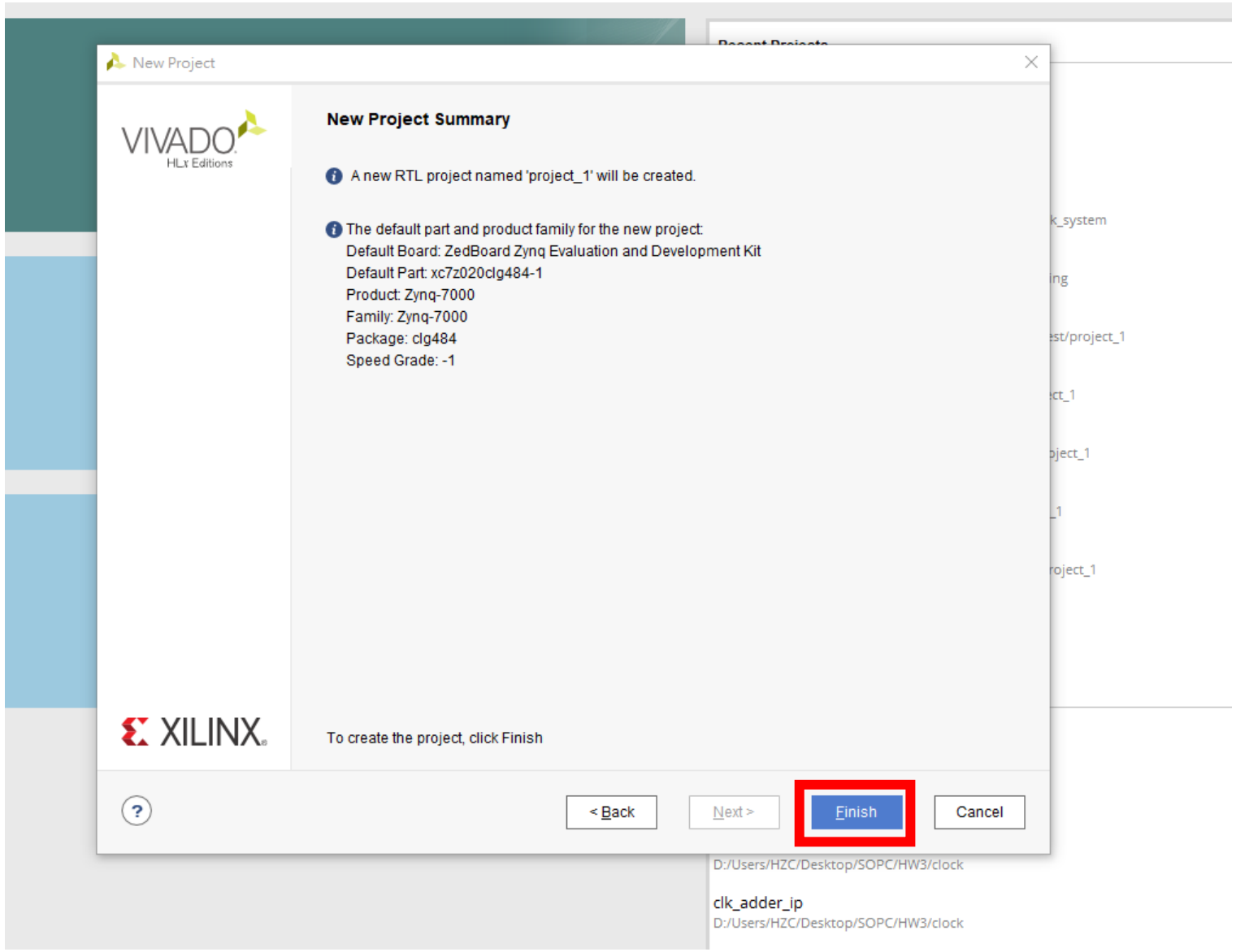
1-3、Create a new project



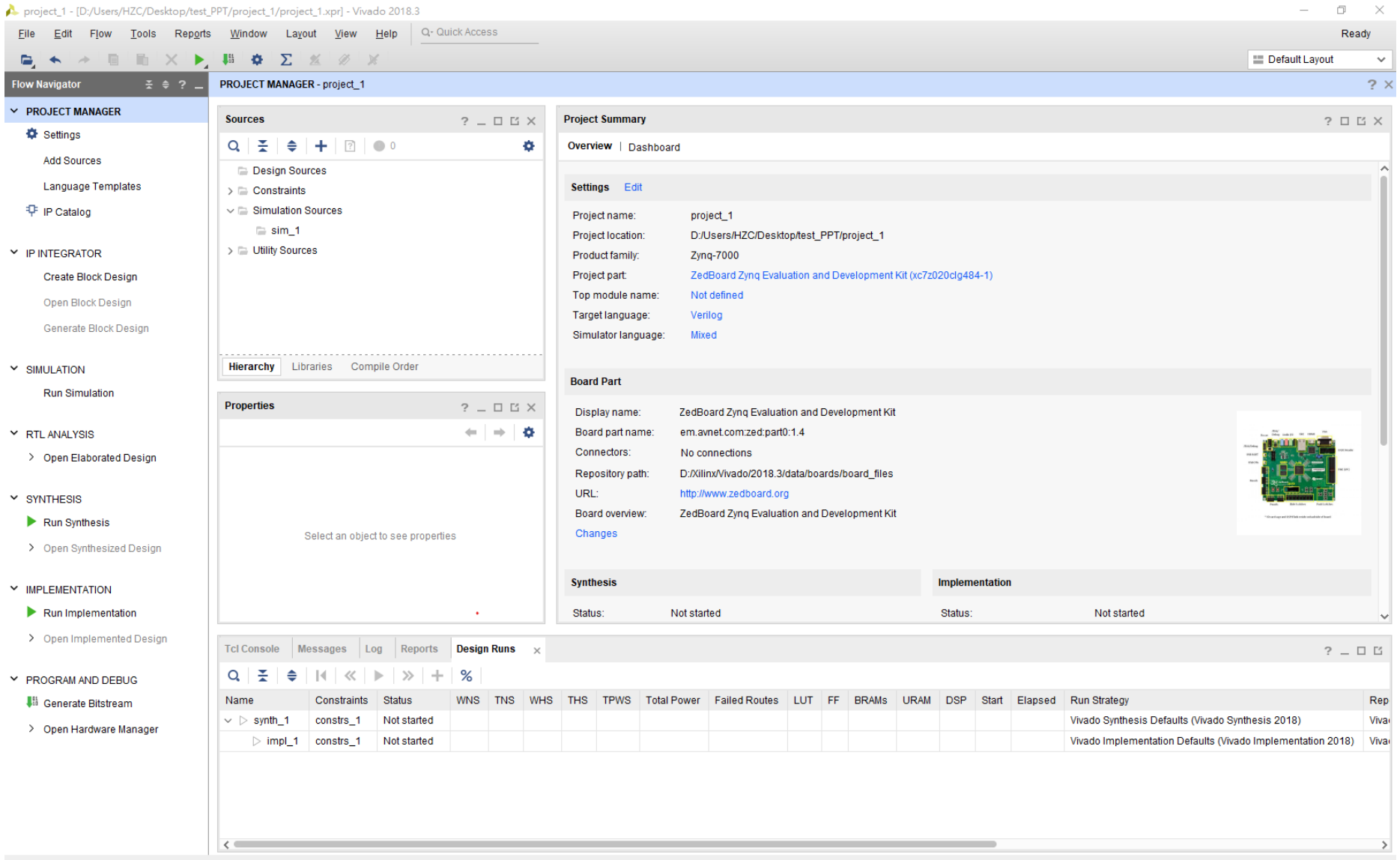
1-4、Create a new project

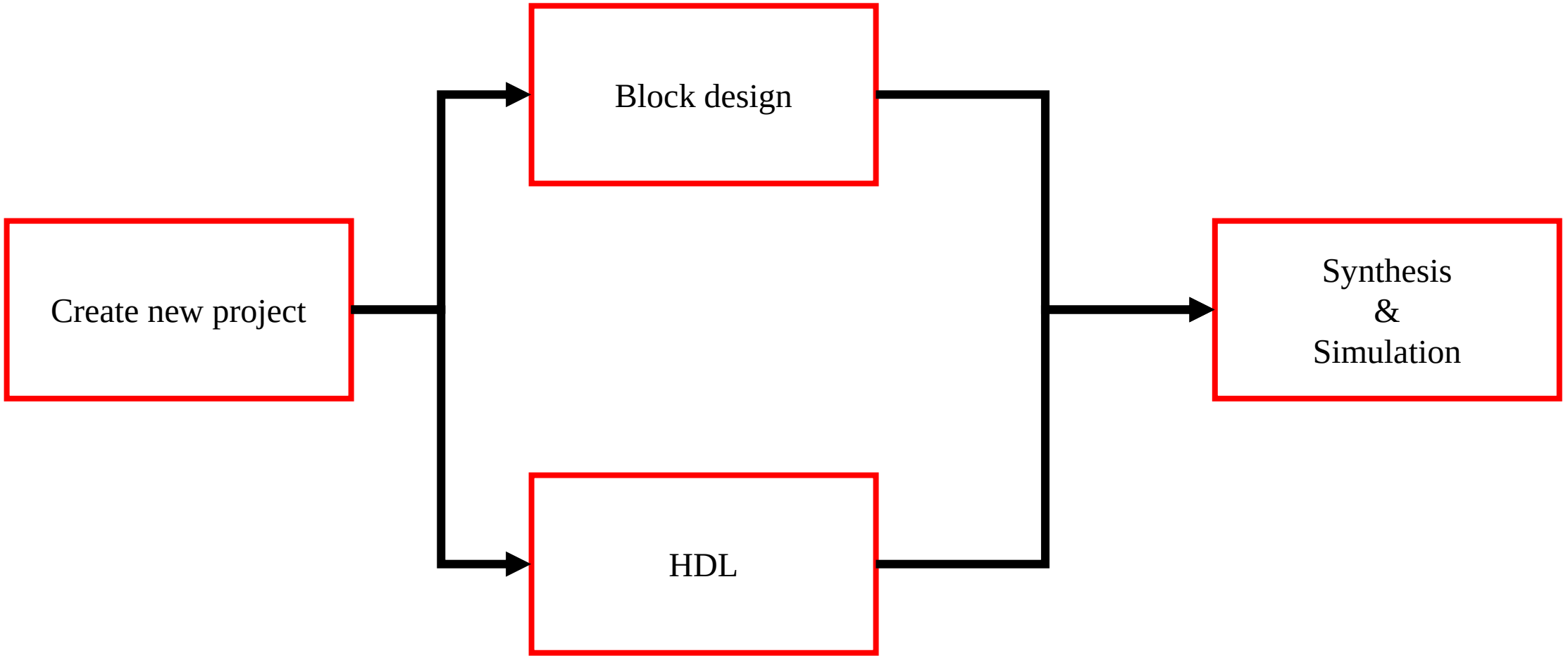


1-5、Create a new project

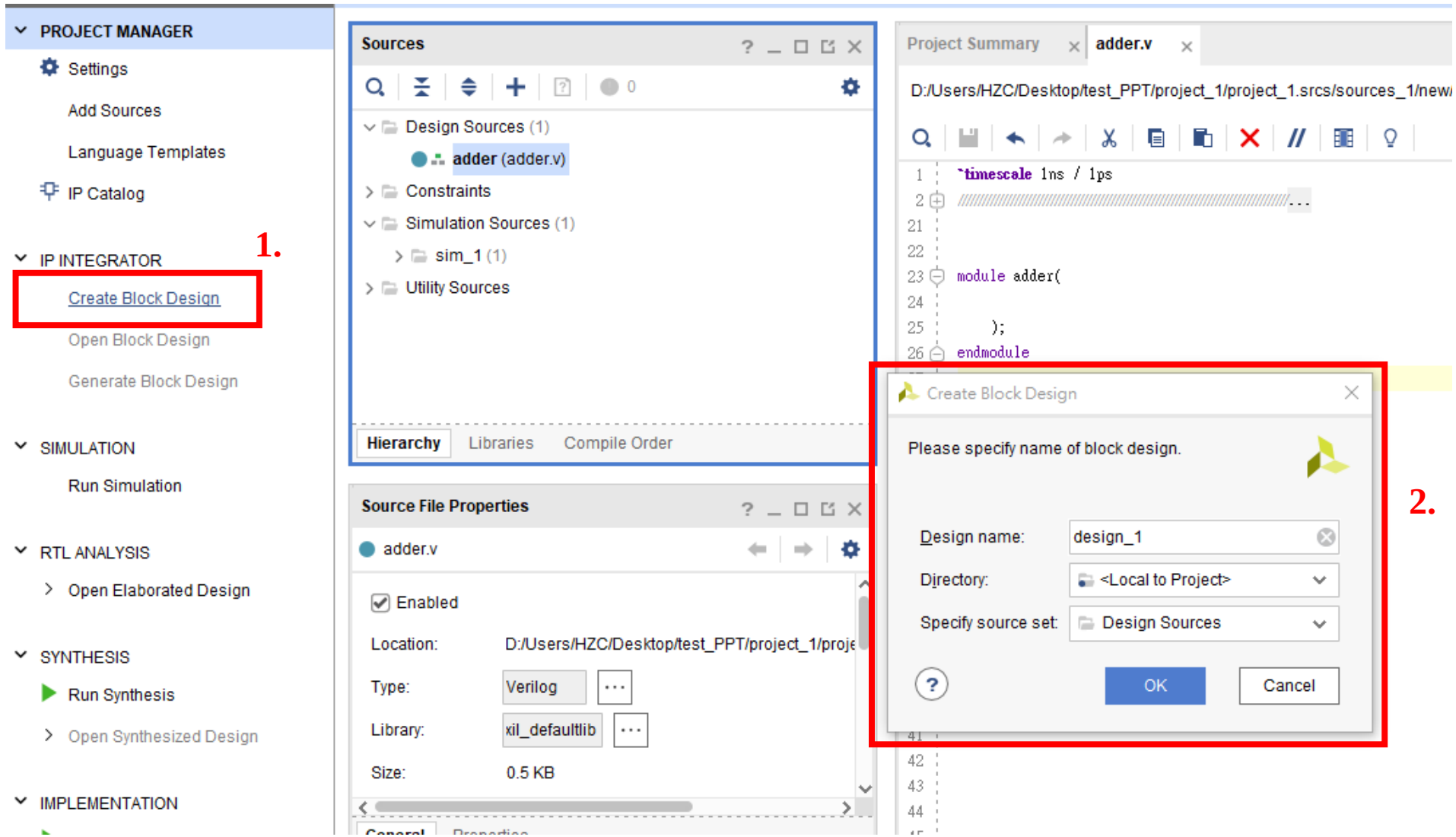


1-6、Create a new project

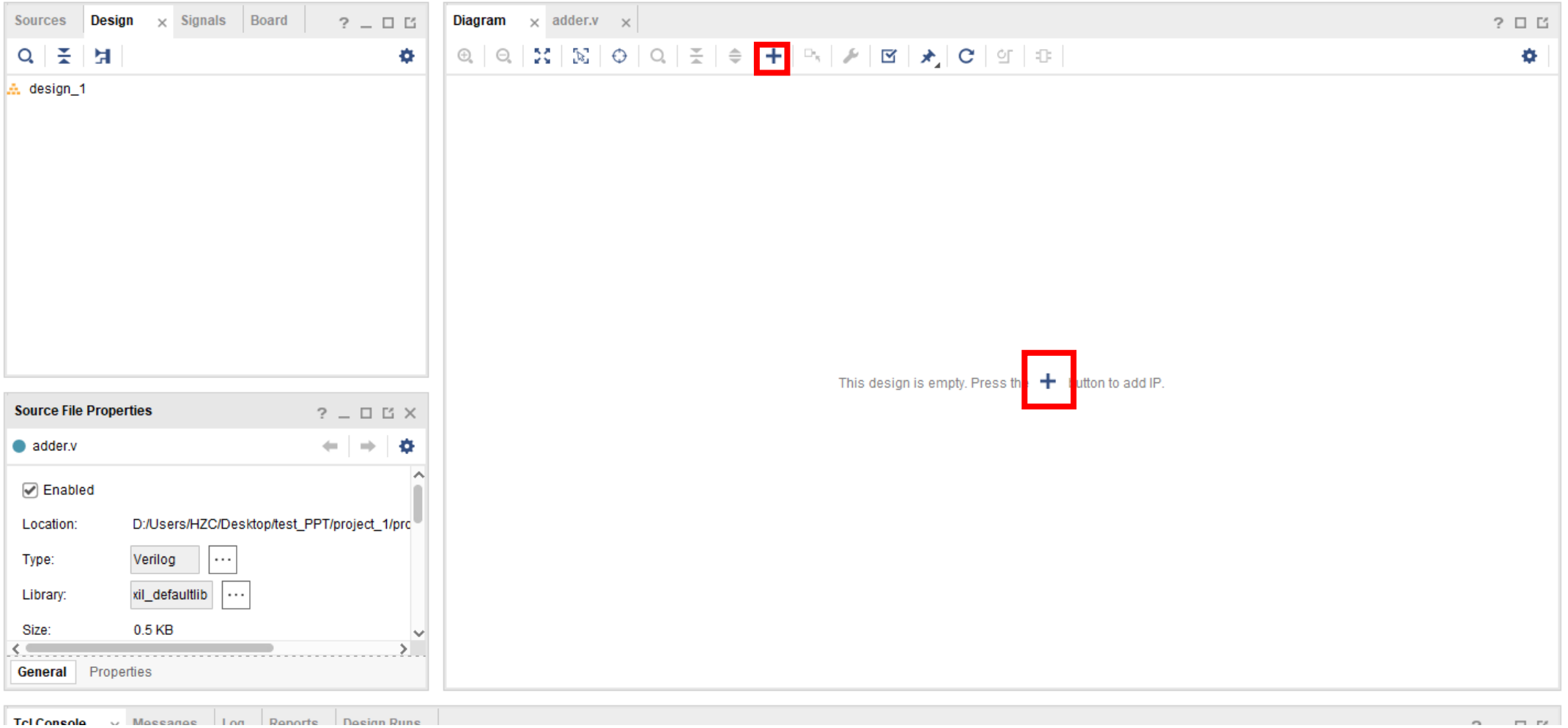



Block design
Create new project
Synthesis
&
Simulation
HDL

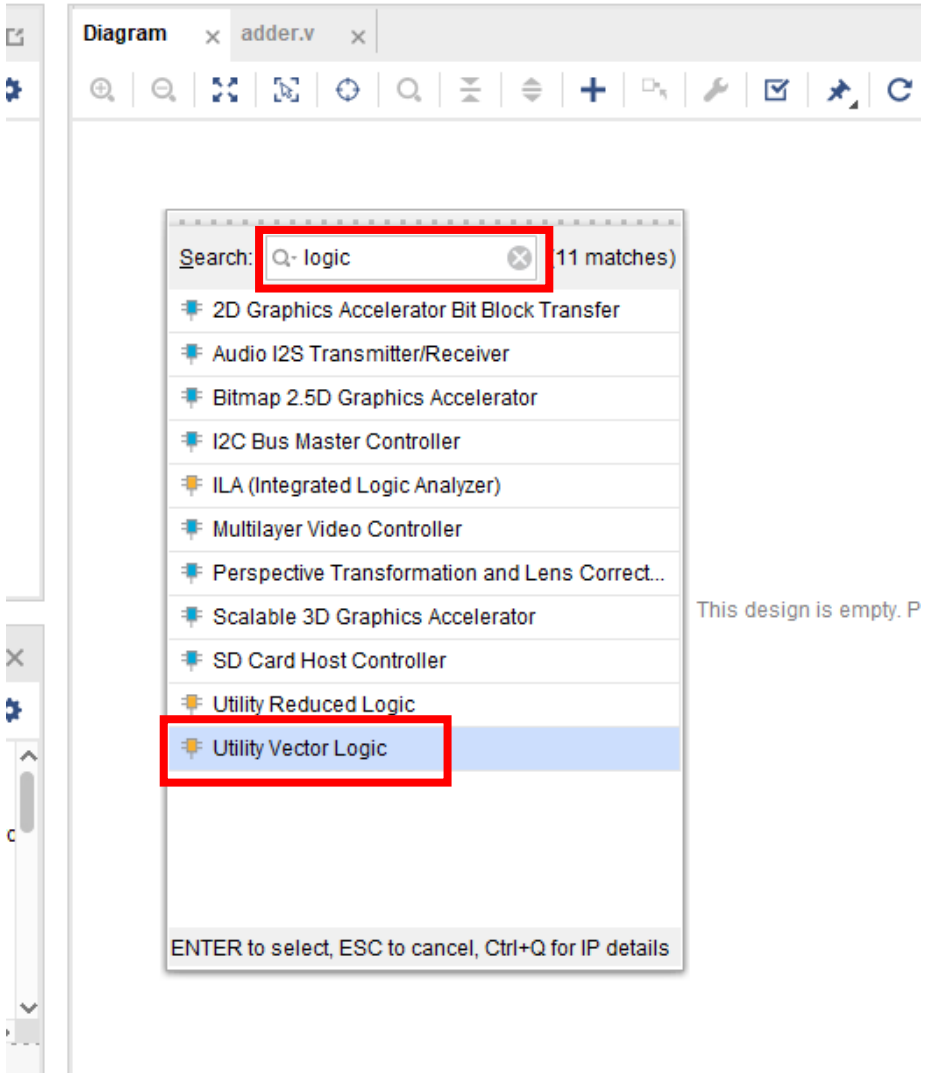
2-1、Block design



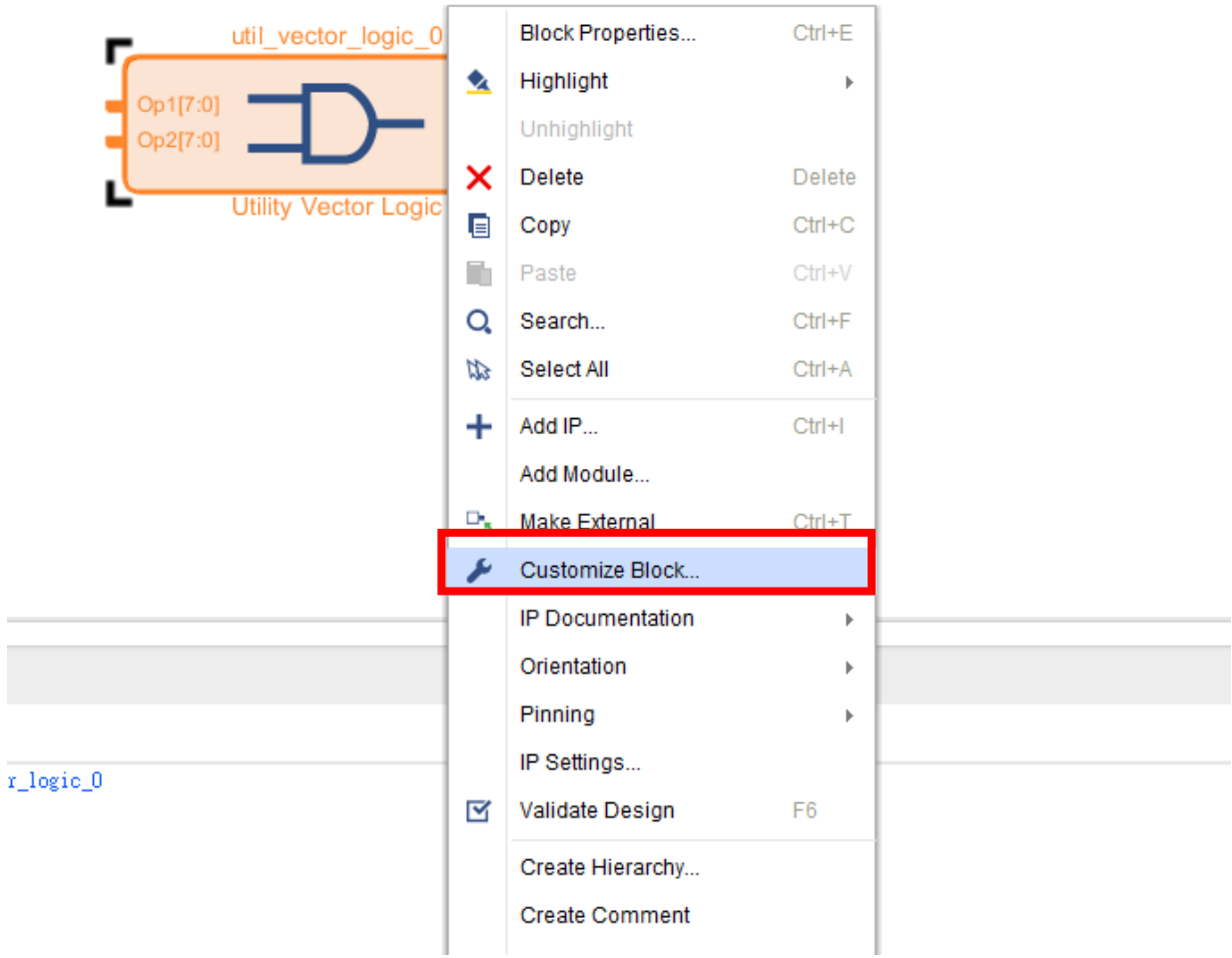
2-2、 Block design



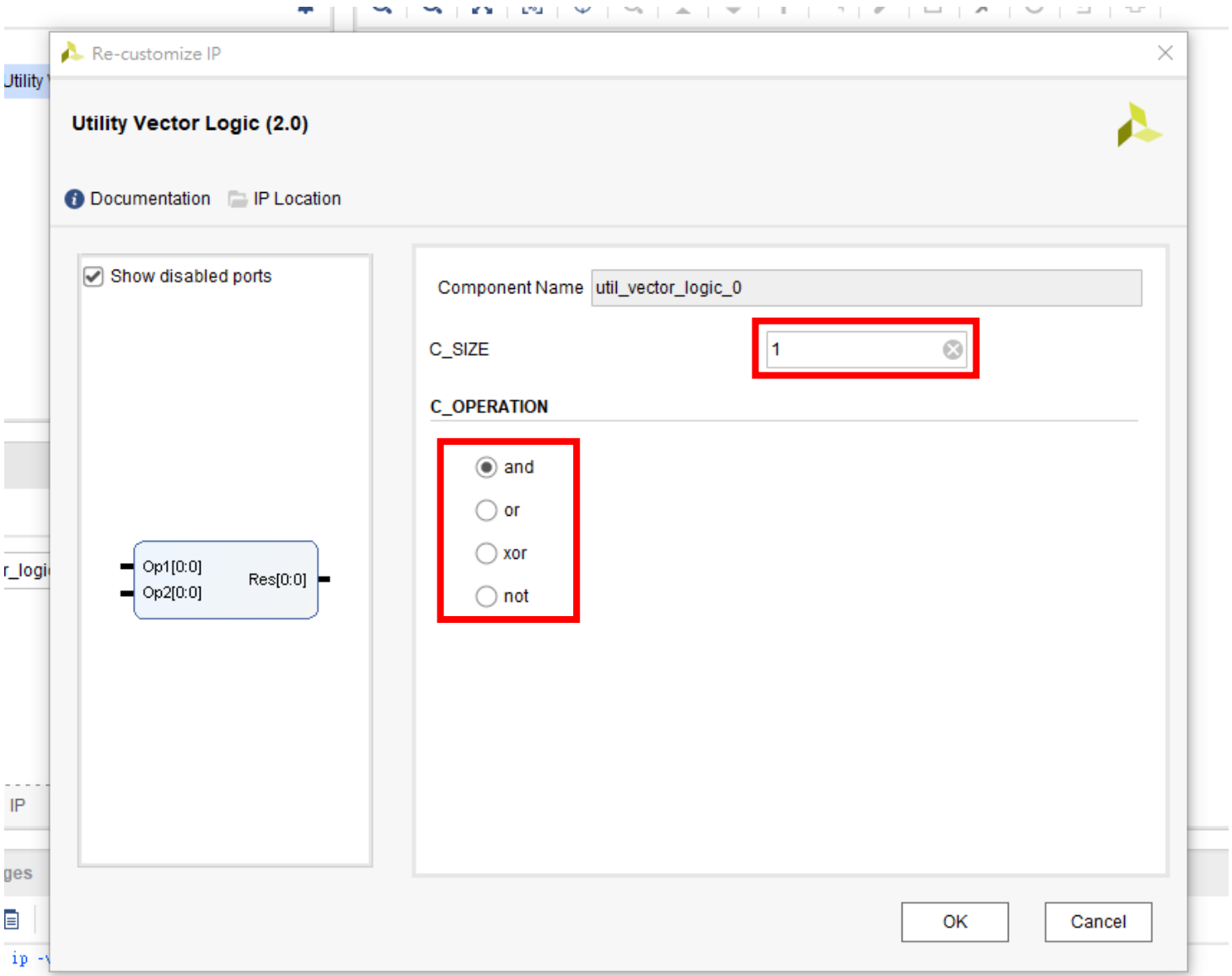
2-3、 Block design



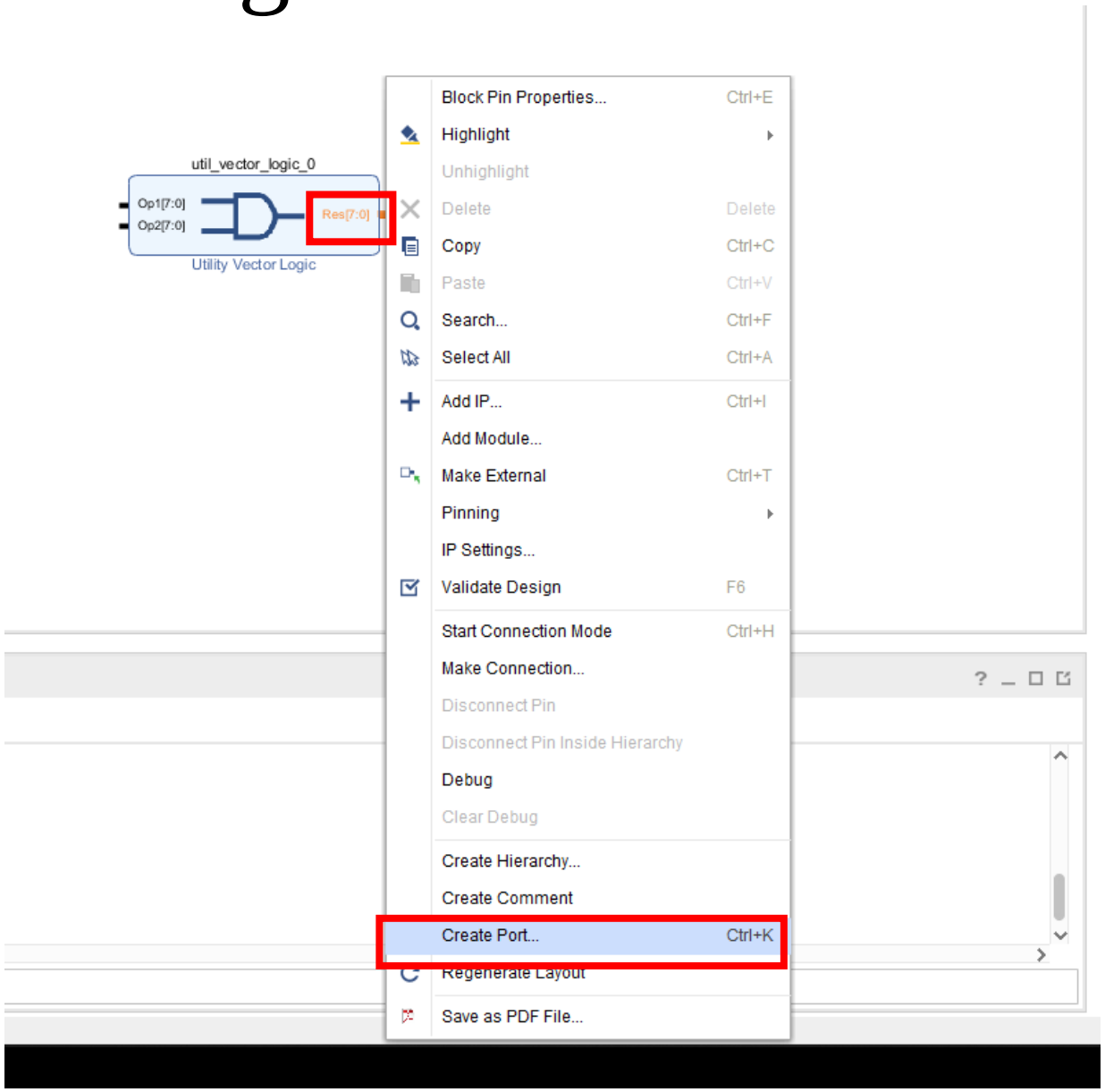
2-4、 Block design



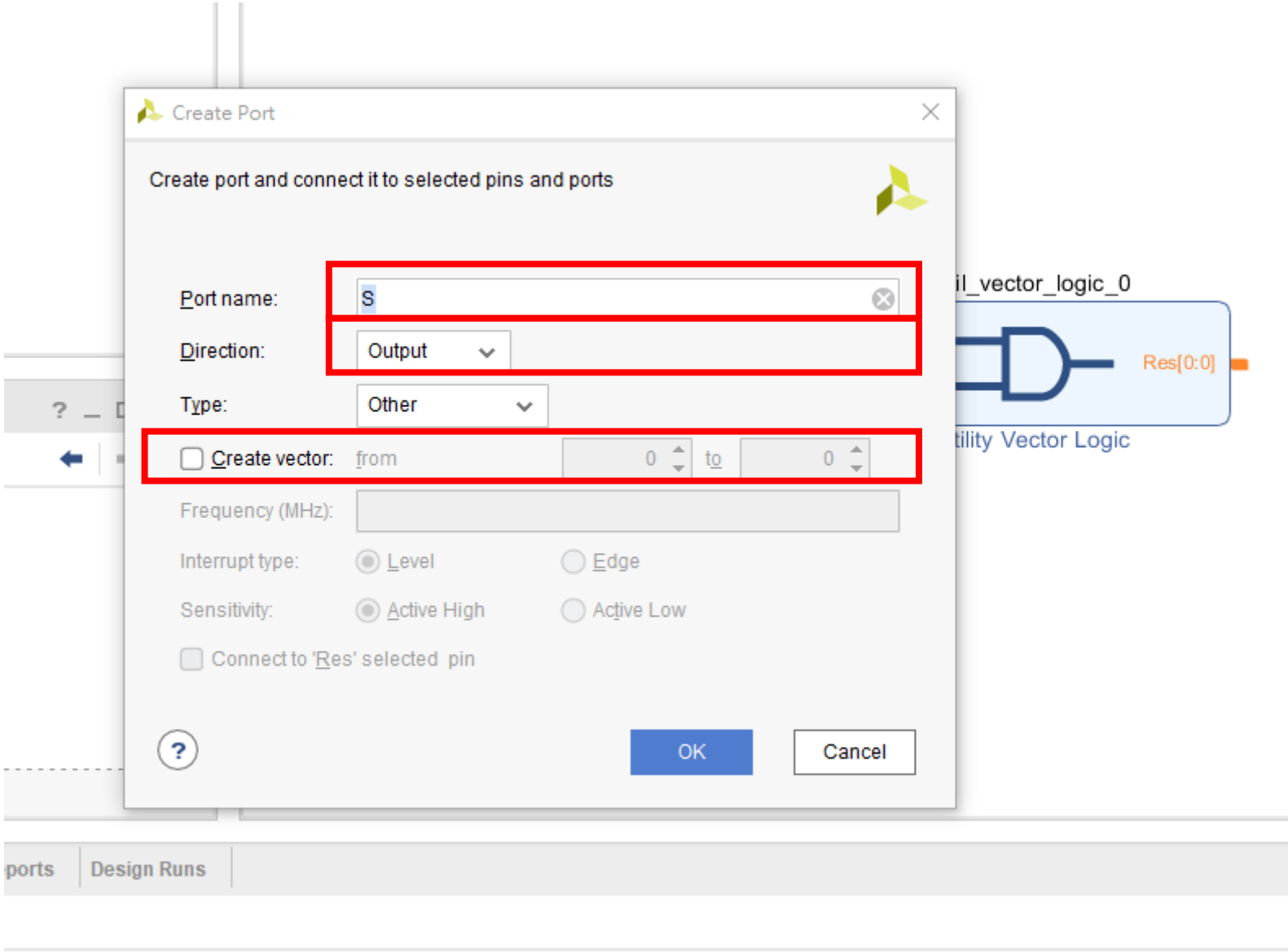
2-5、 Block design



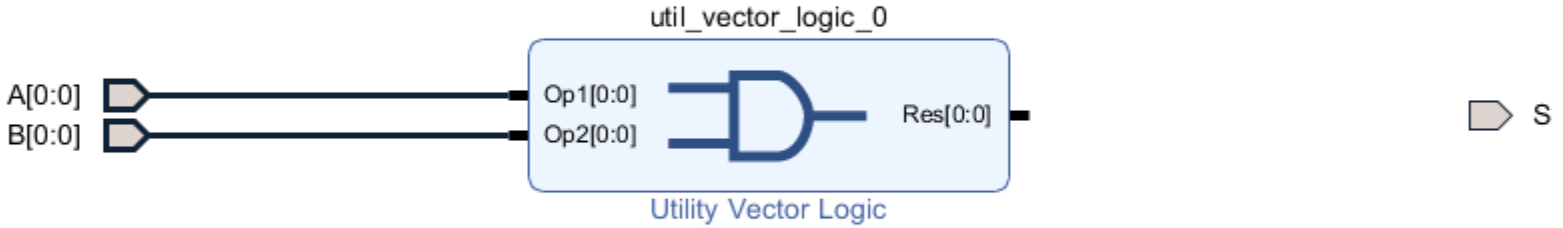
2-6、 Block design



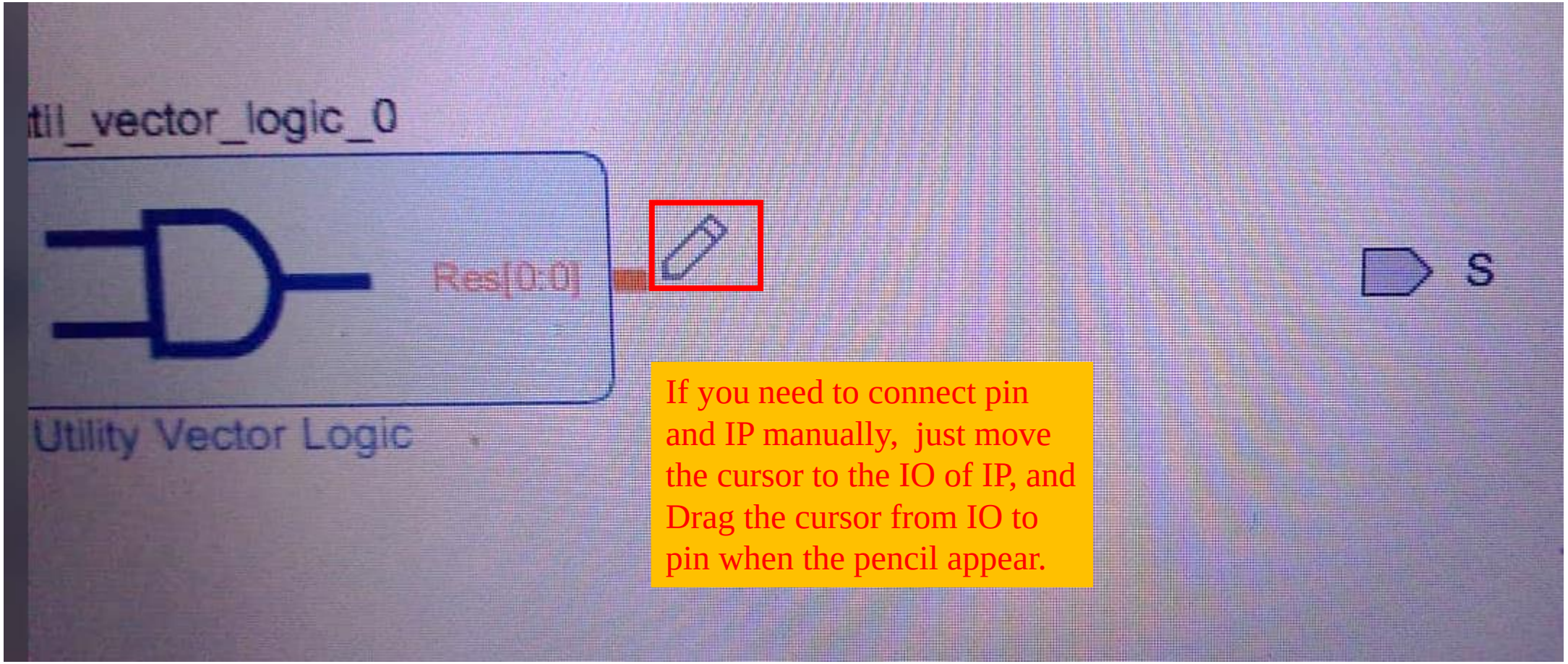
2-7、 Block design



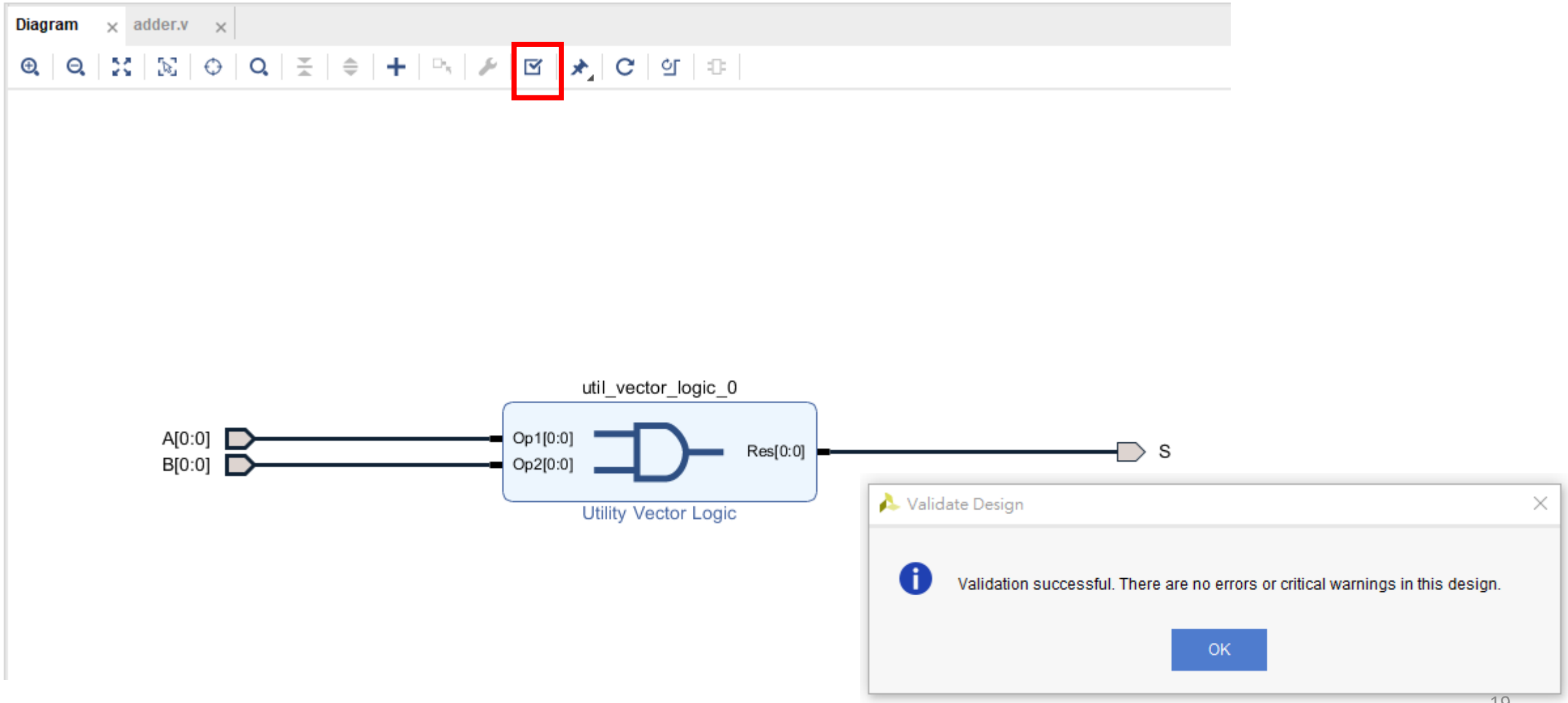
2-8、 Block design



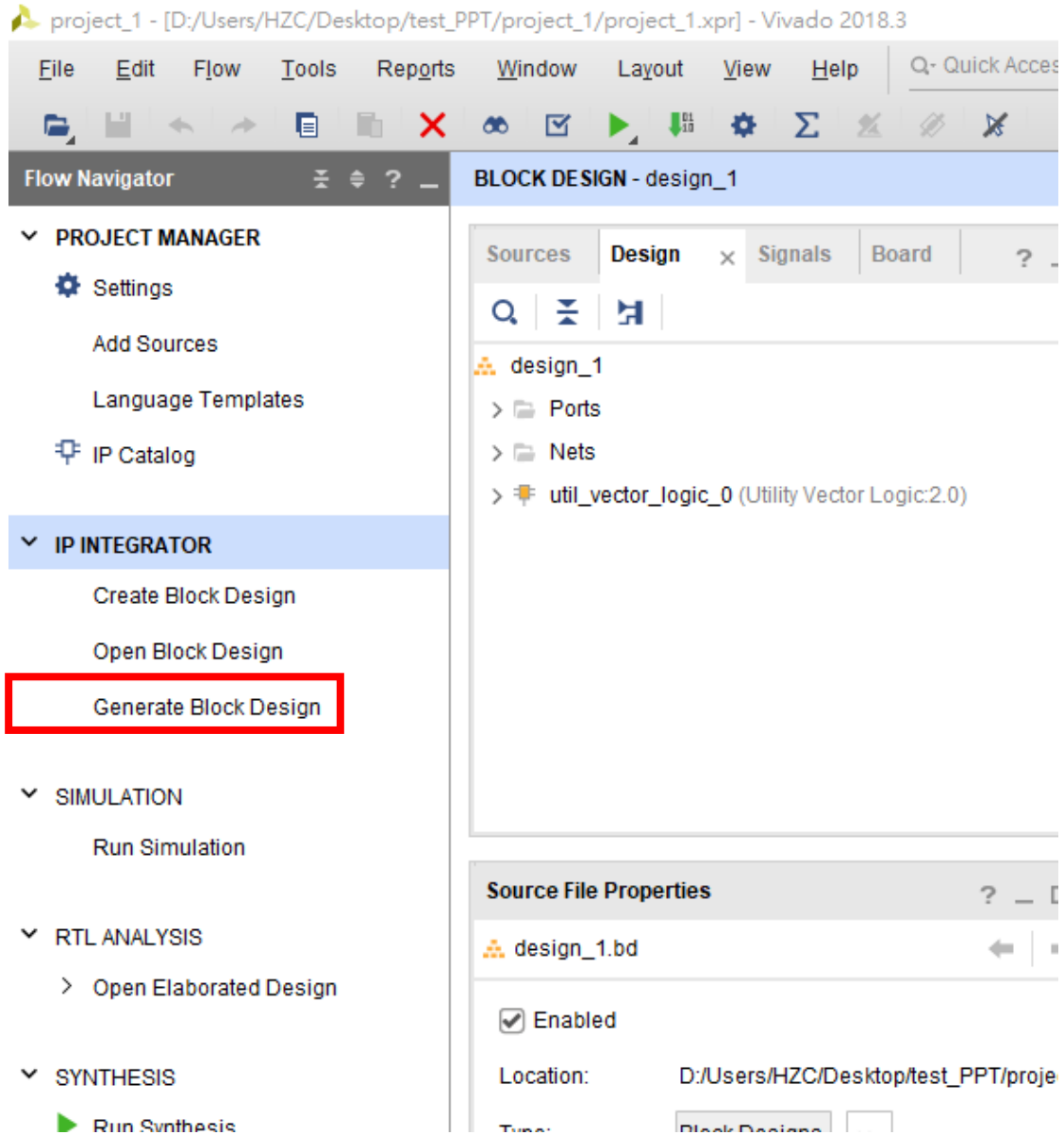
2-9、 Block design

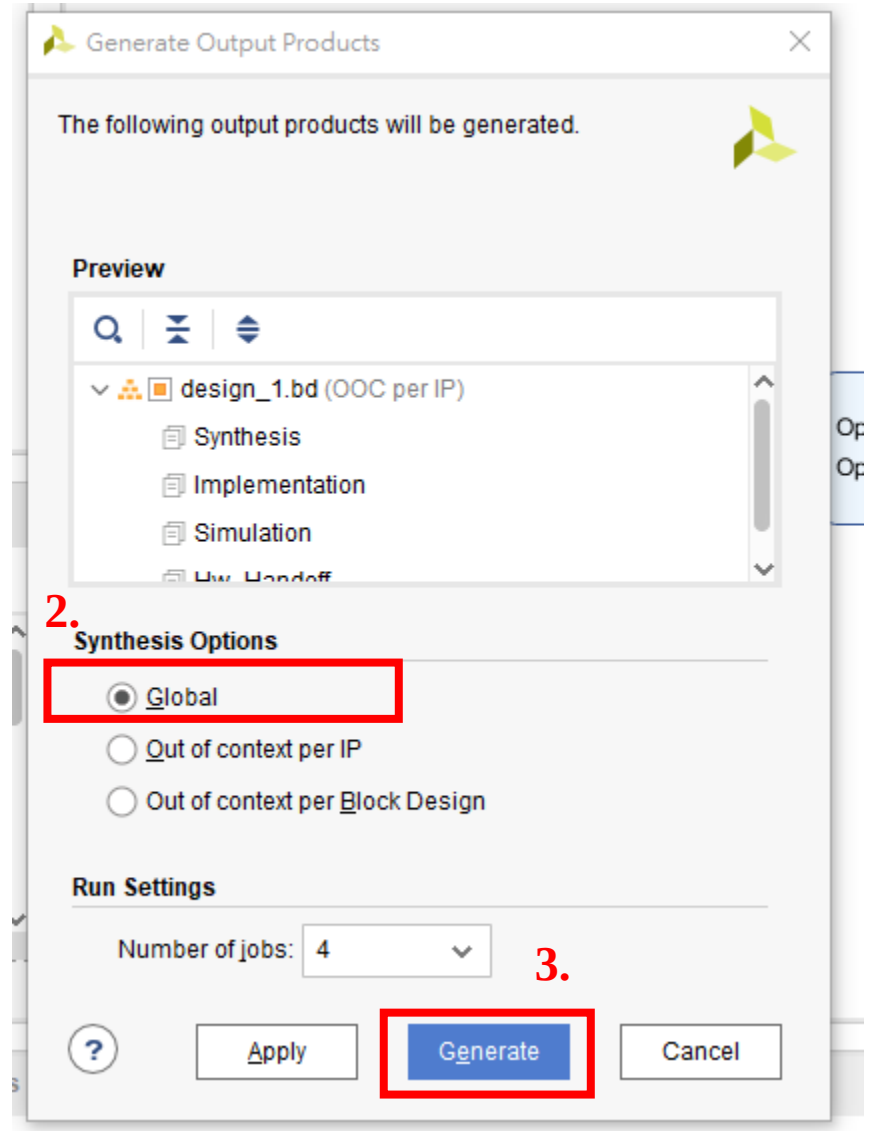


2-10、 Block design

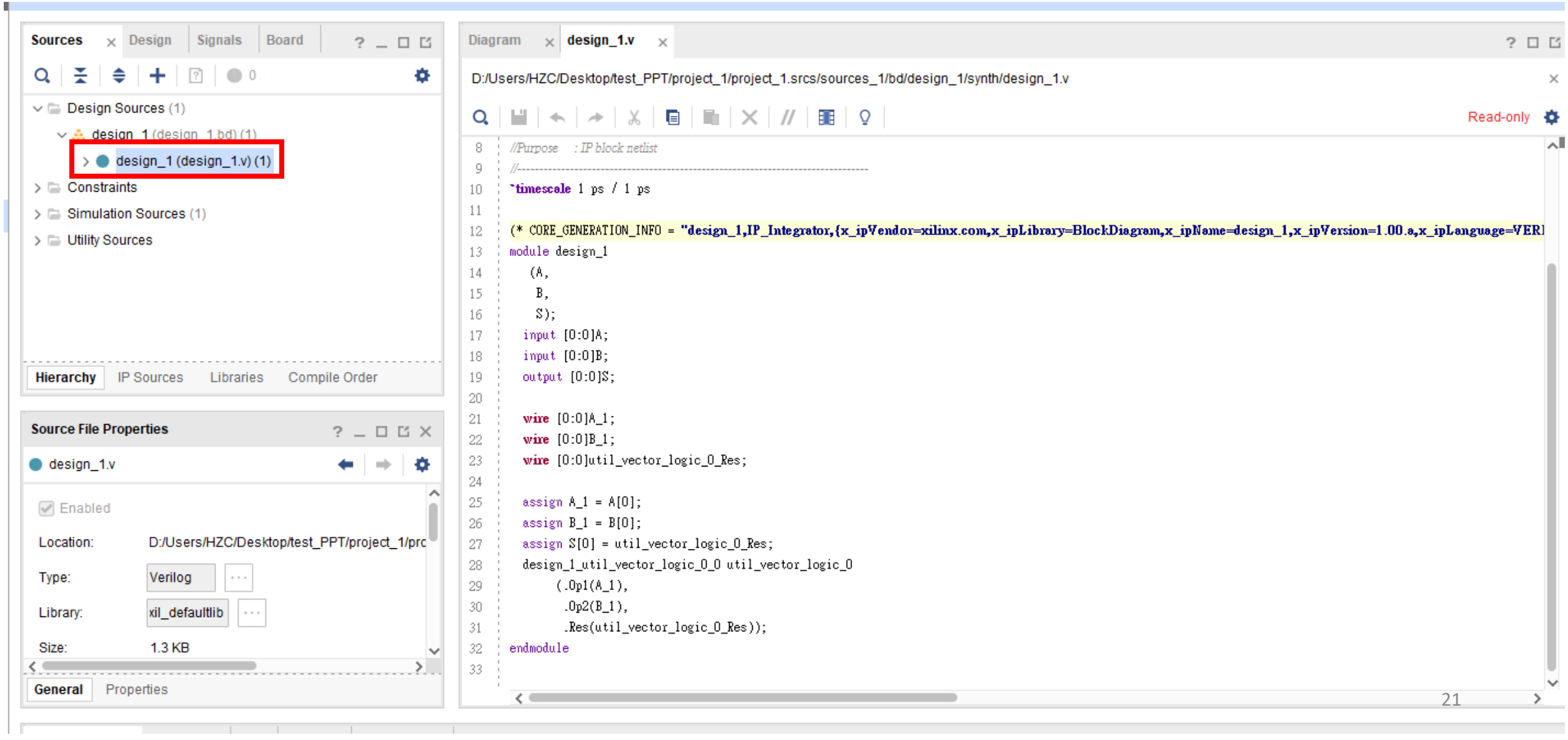


2-11、 Block design

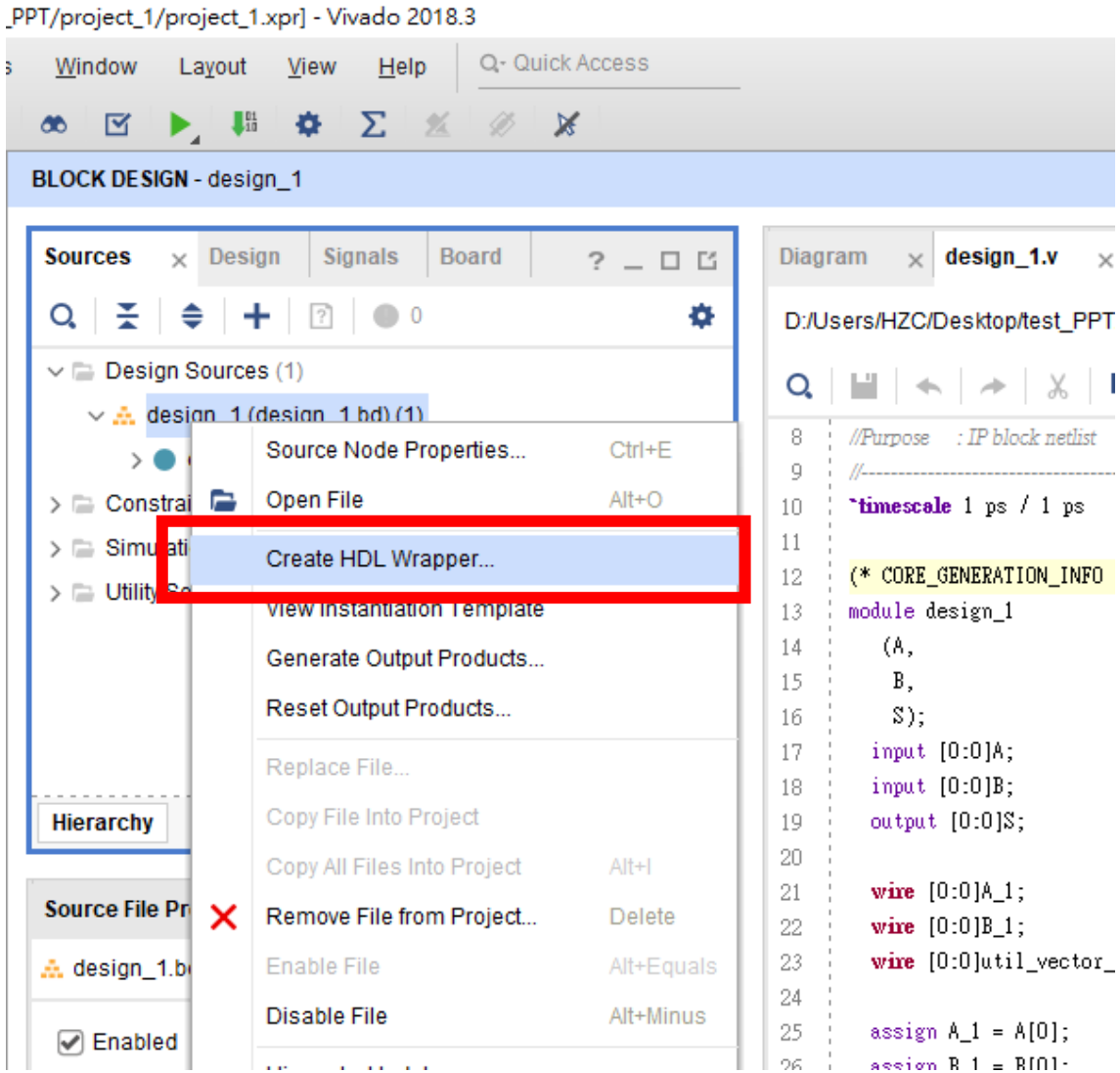


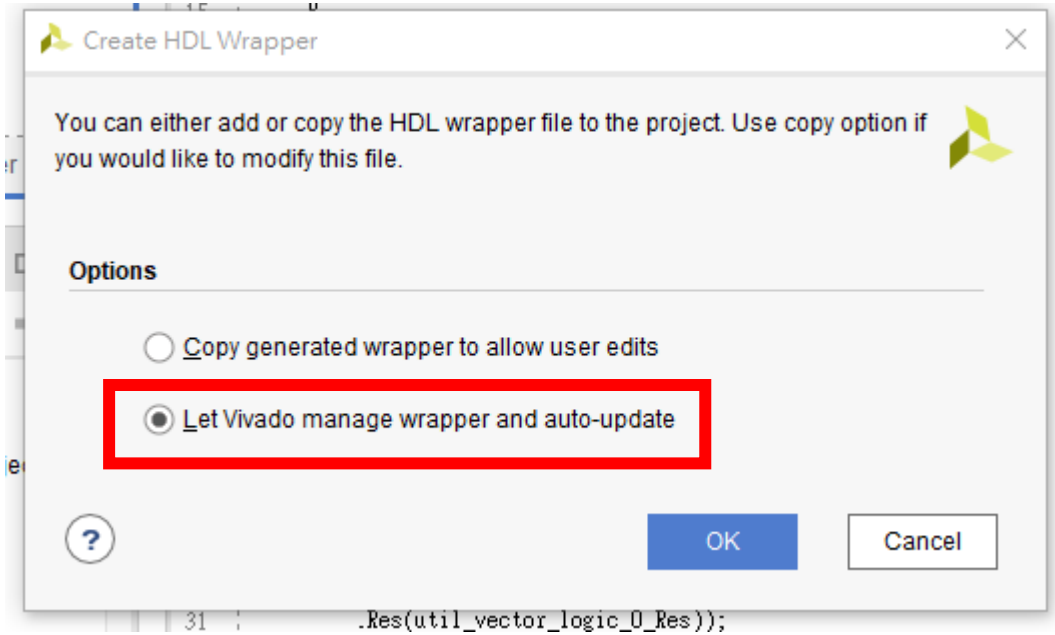


2-12、 Block design

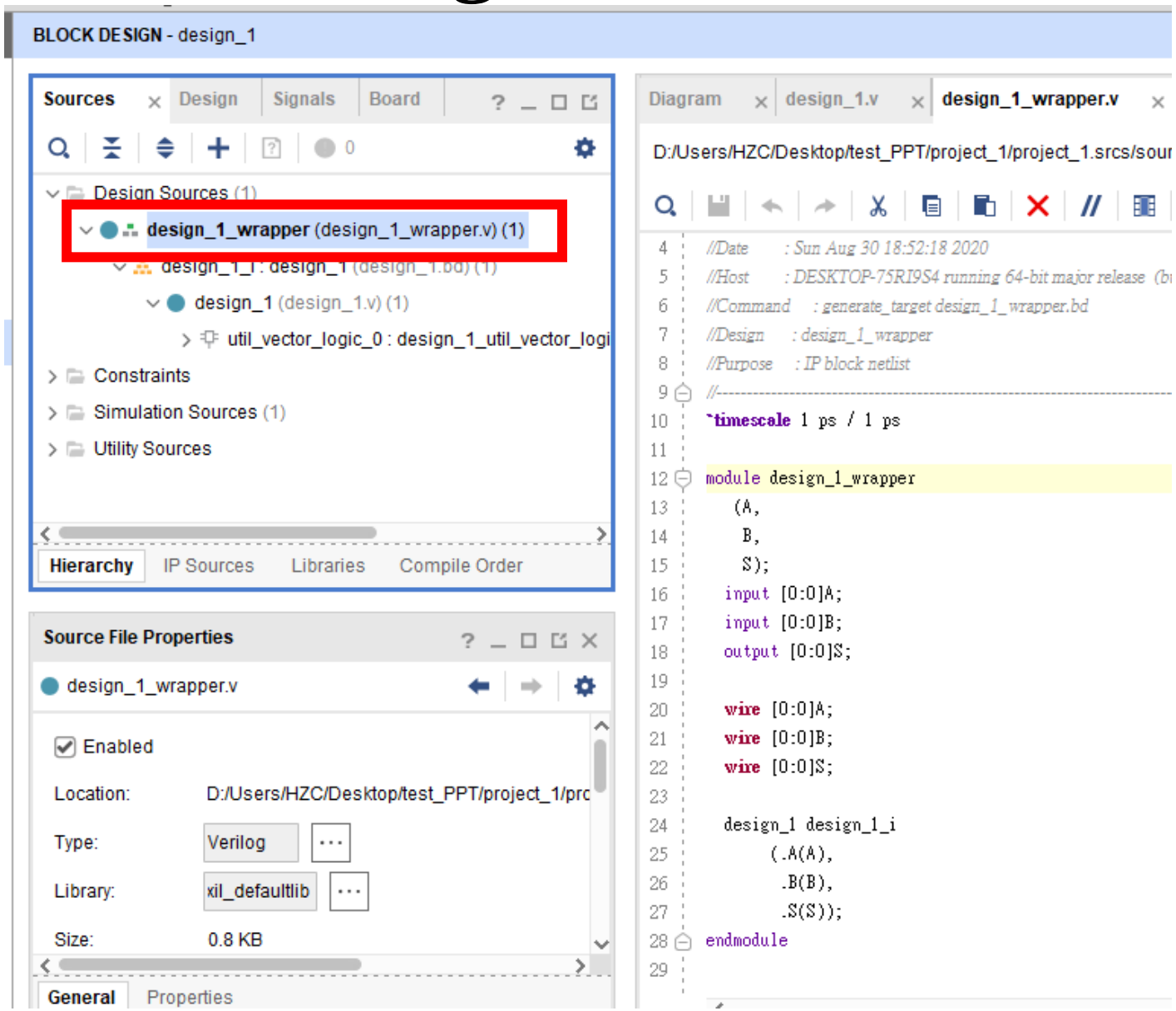


2-13、 Block design

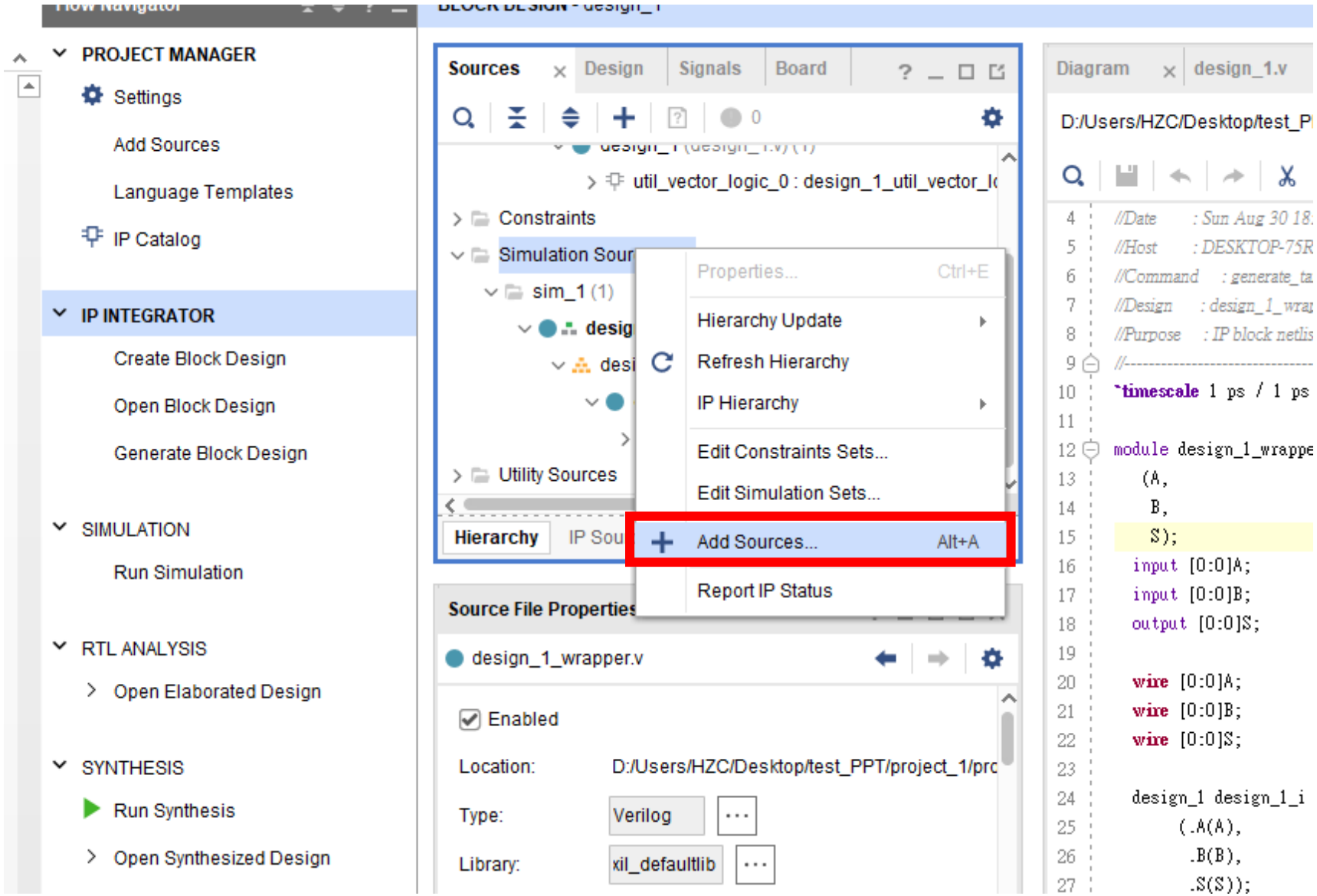




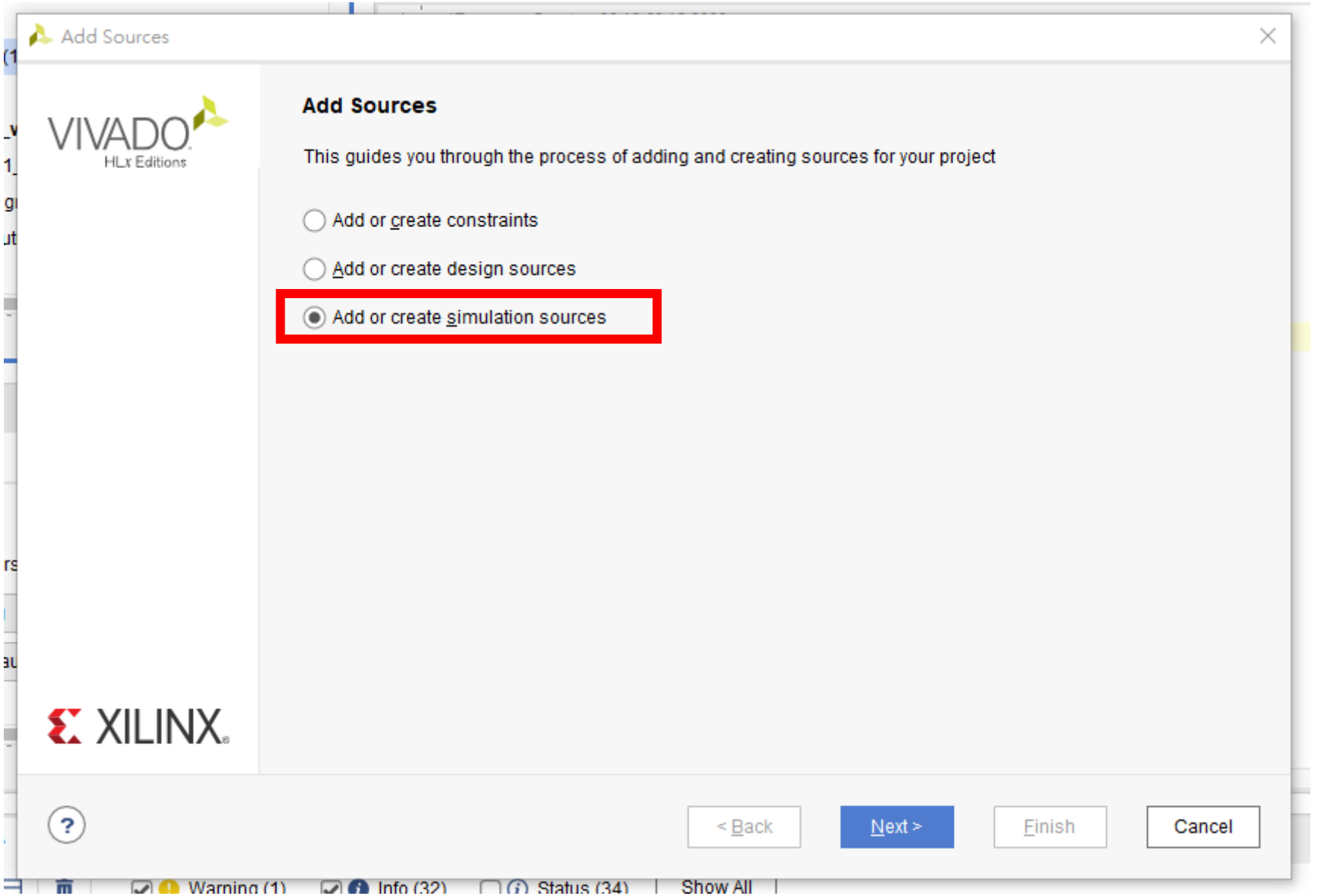
2-14、 Block design



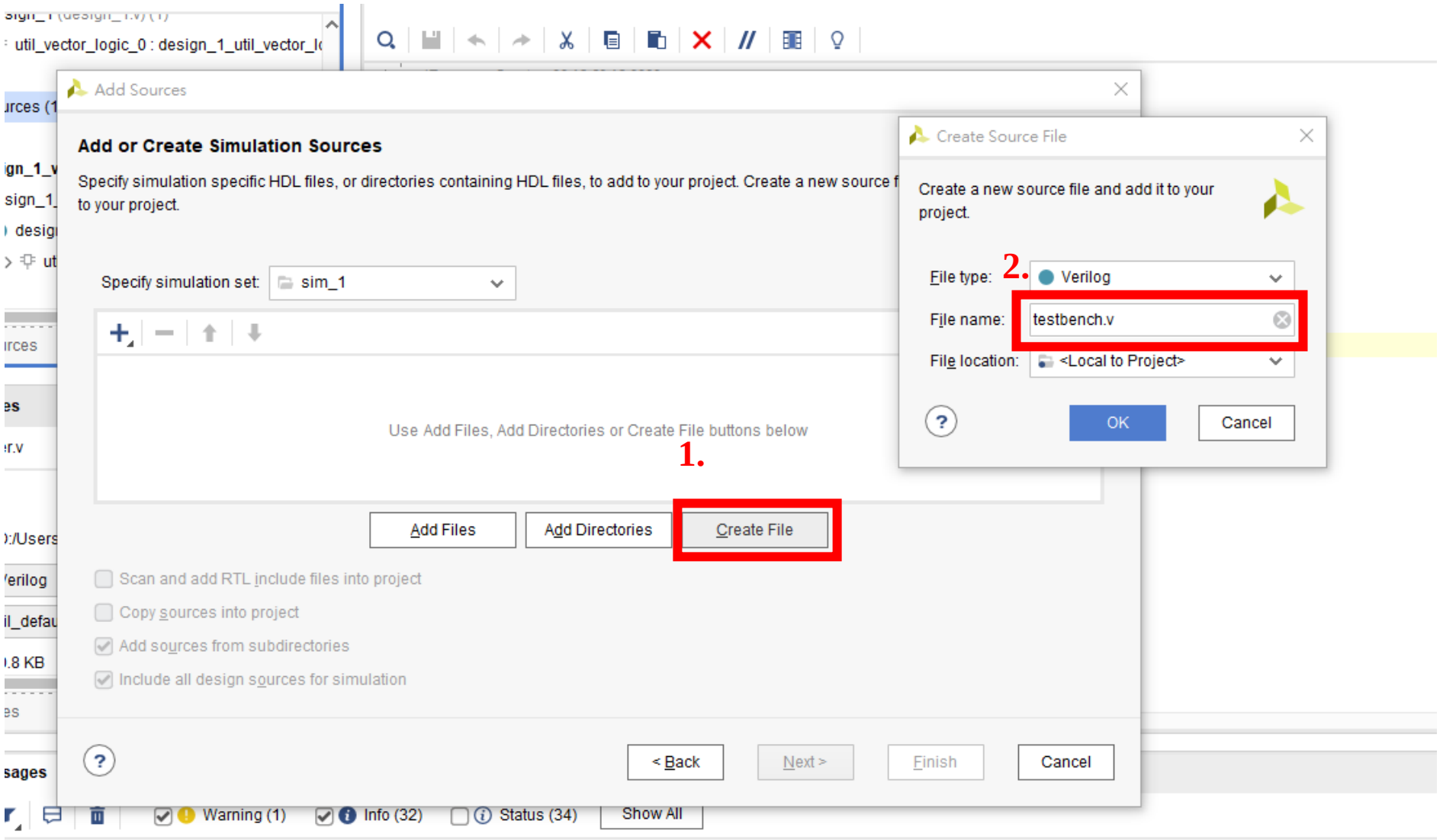
3-1、Testbench



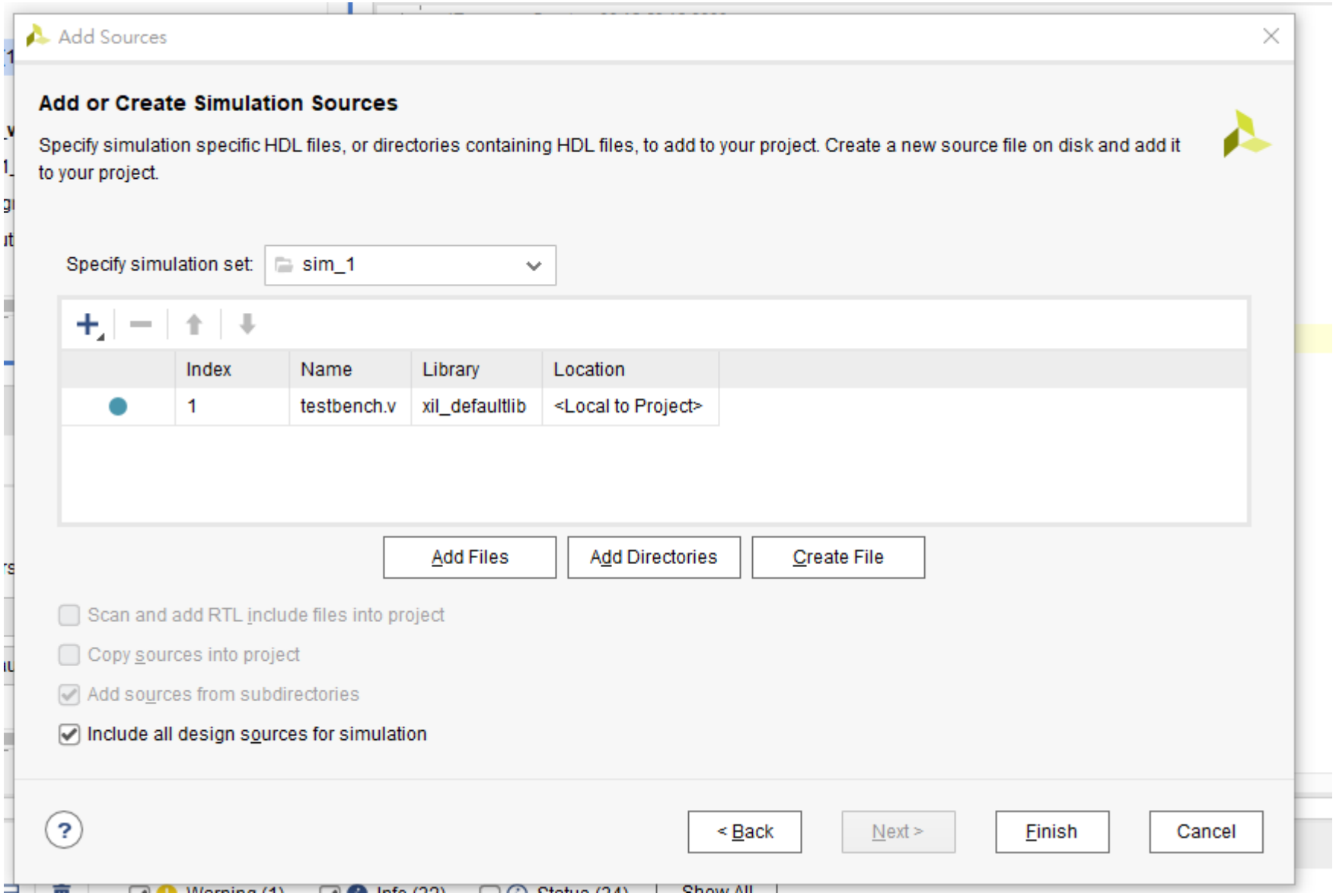
3-2、Testbench



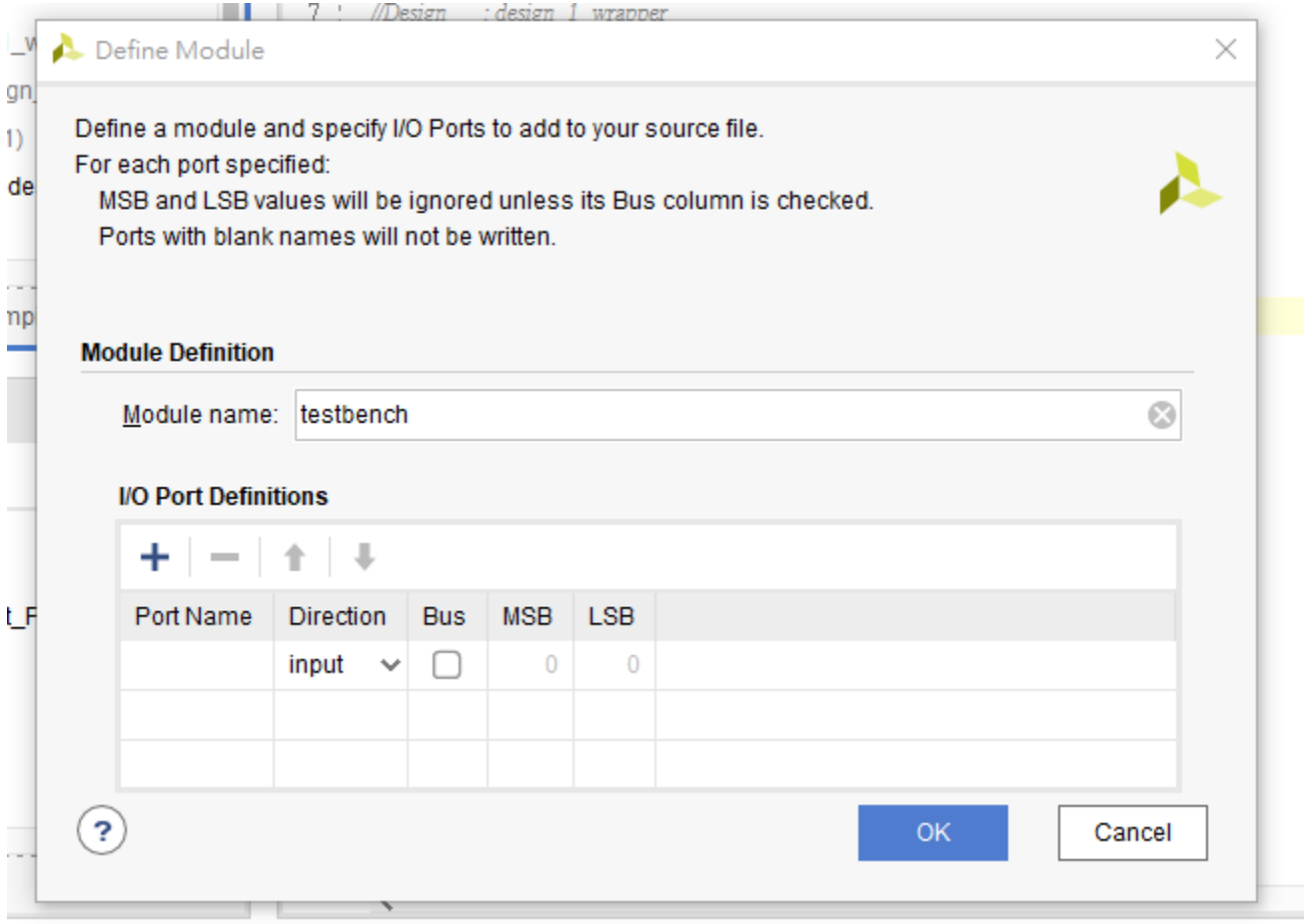
3-3、Testbench



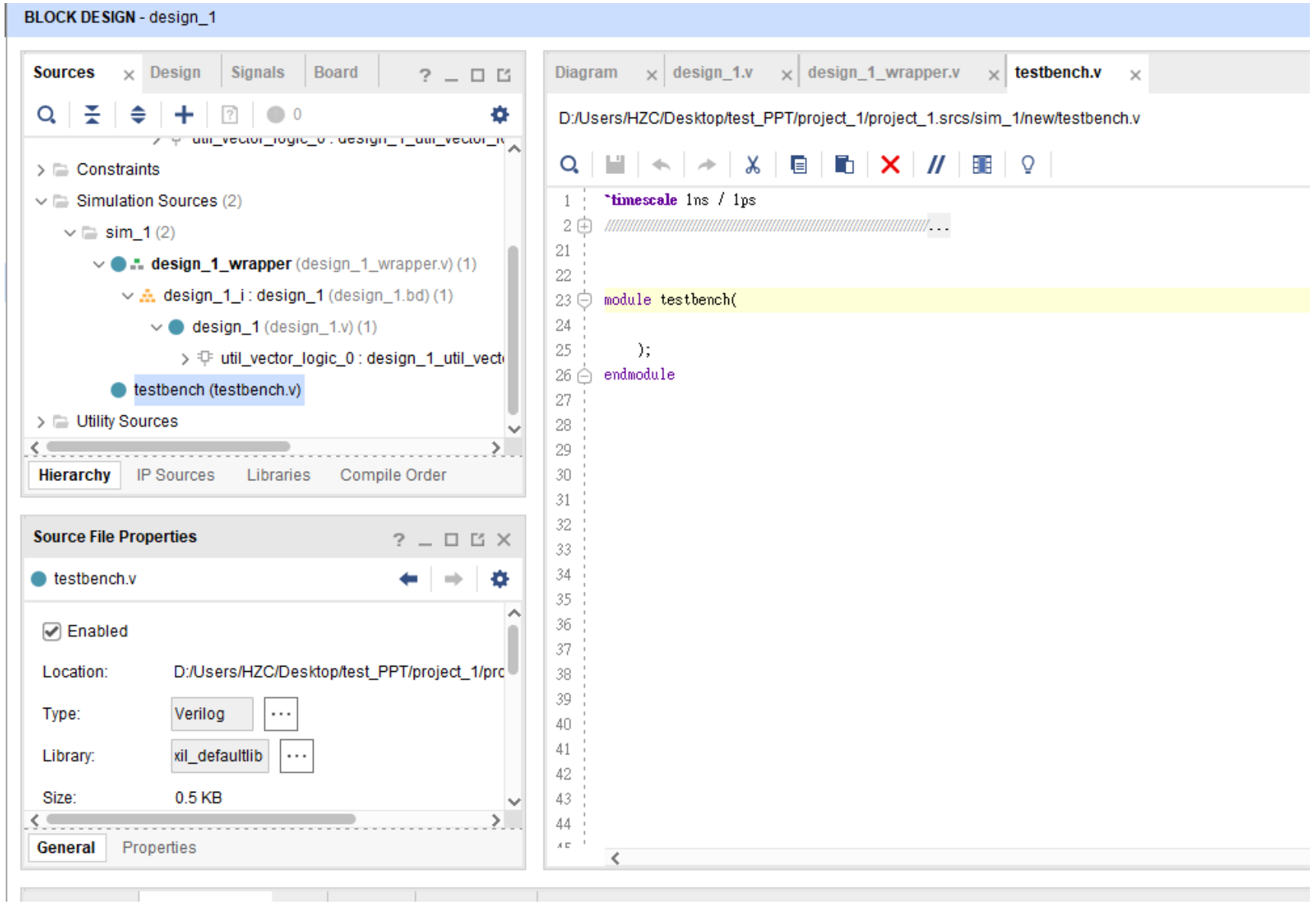
3-4、Testbench



3-5、 Testbench



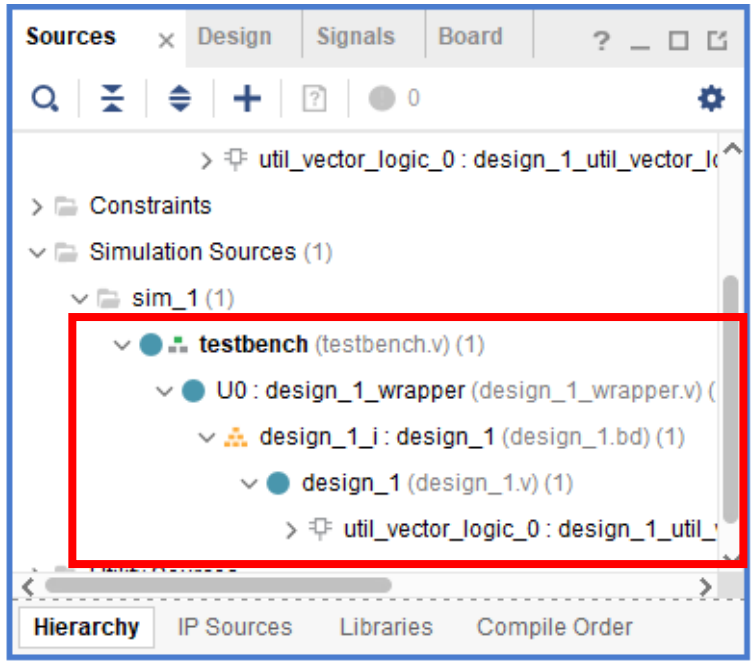
3-6、Testbench

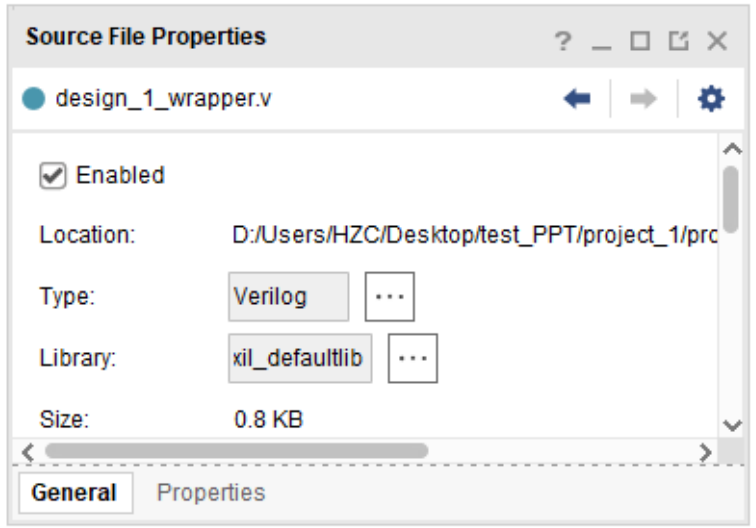


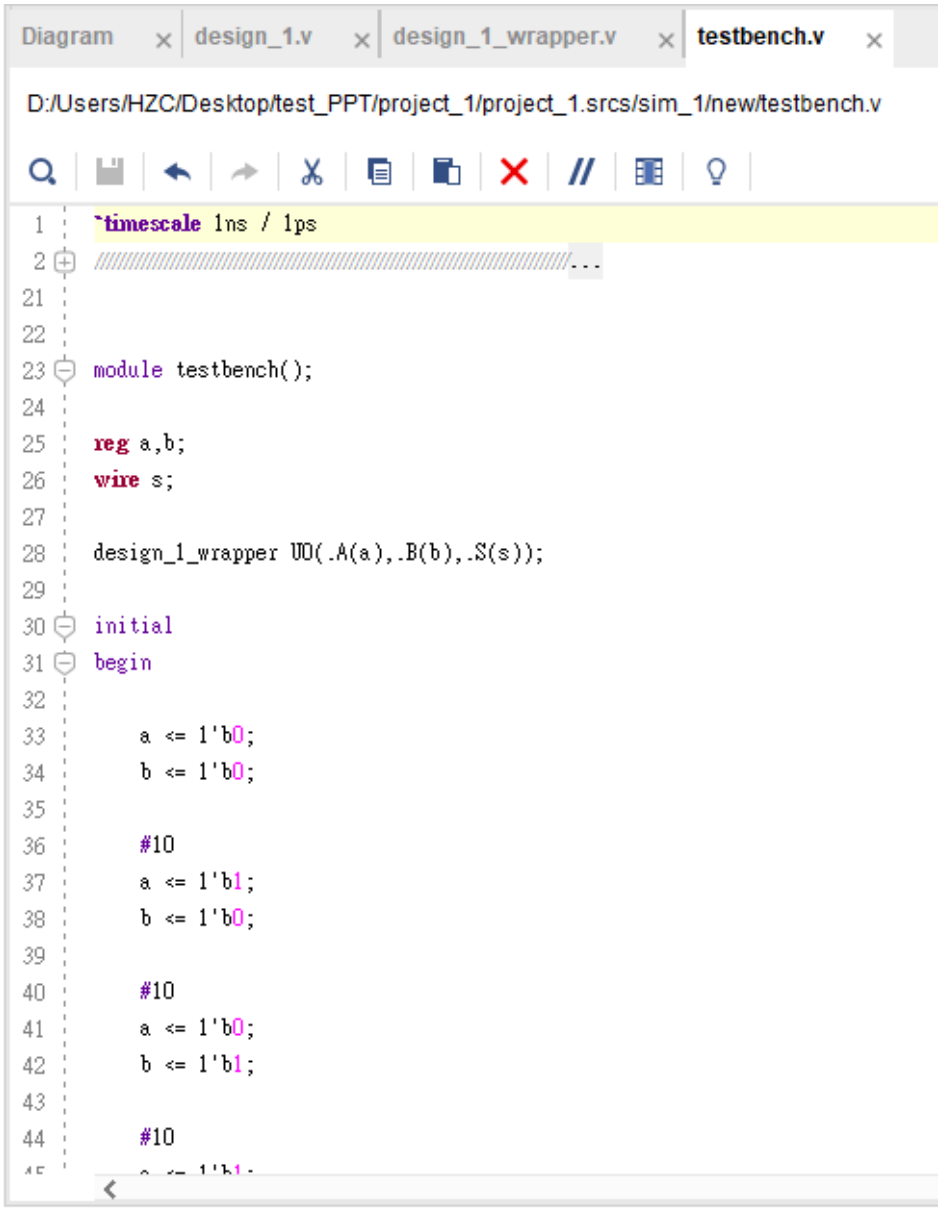
3-7、 Testbench

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////...
21  module testbench();
22
23  reg a,b;
24  wire s;
25
26  design_1_wrapper UO(.A(a),.B(b),.S(s));
27
28  initial
29  begin
30
31      a <= 1'b0;
32      b <= 1'b0;
33
34      #10
35      a <= 1'b1;
36      b <= 1'b0;
37
38      #10
39      a <= 1'b0;
40      b <= 1'b1;
41
42      #10
43      a <= 1'b1;
44      b <= 1'b1;
45
46      #10
47      $finish;
48
49  end
50  endmodule
```

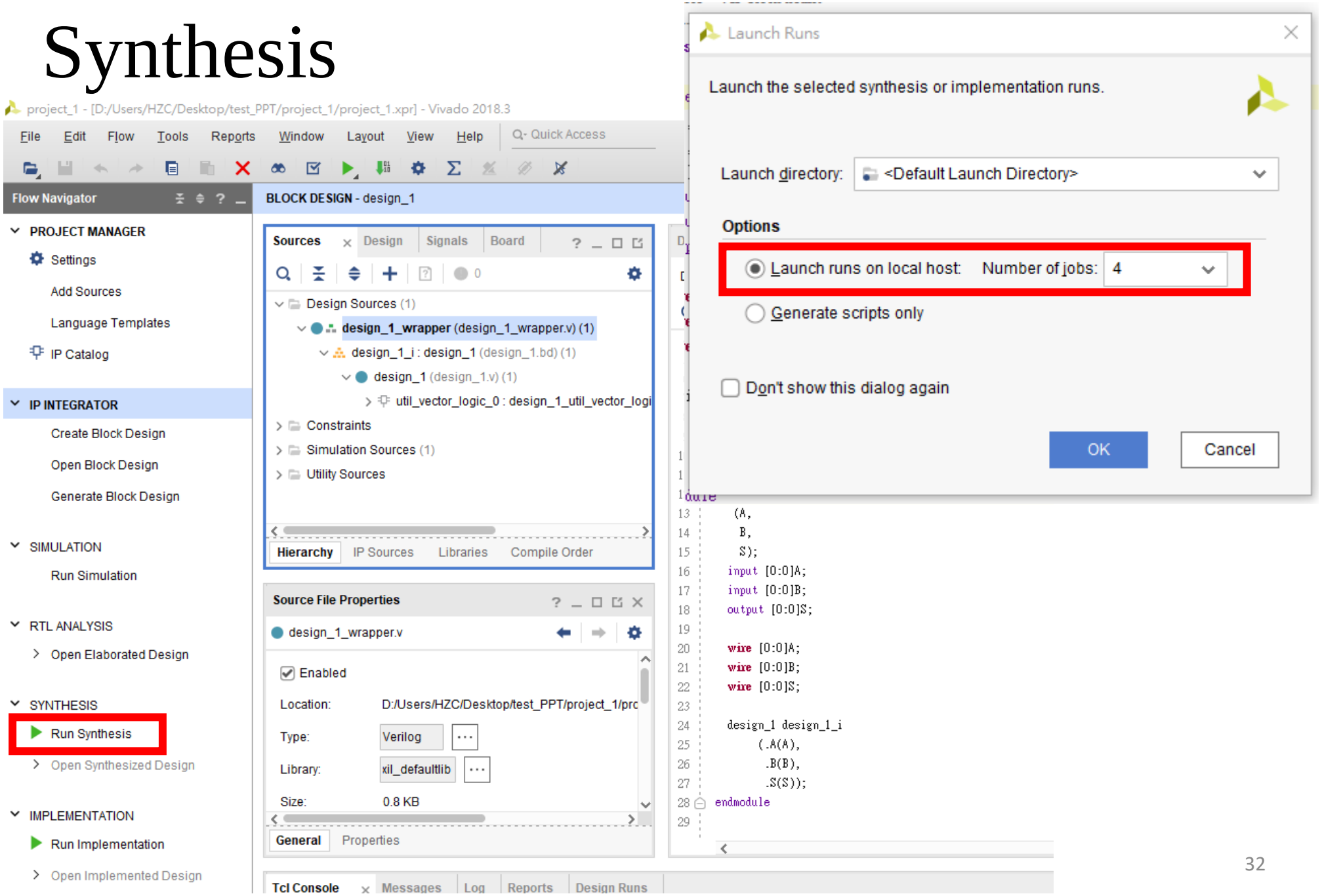
3-8、Testbench



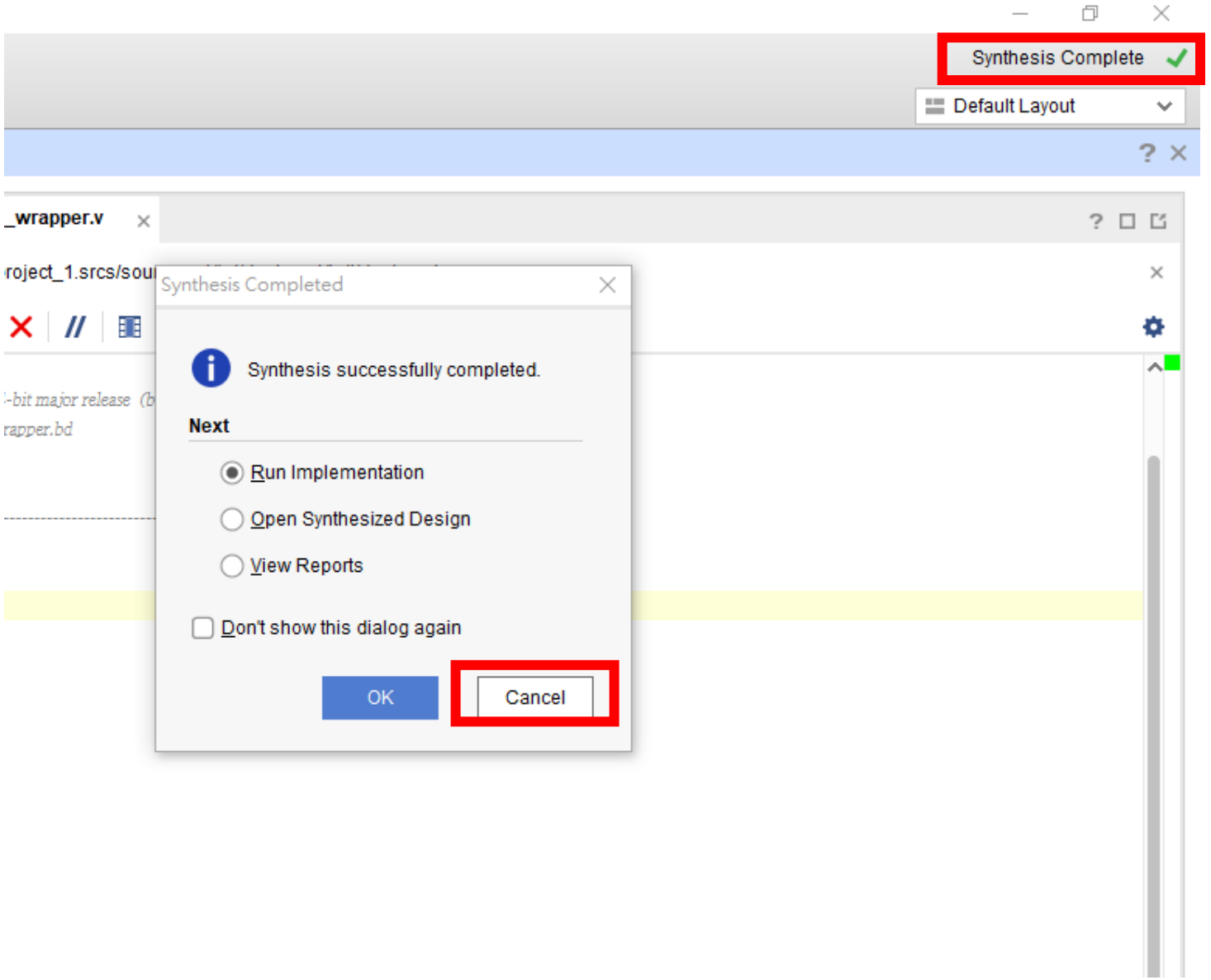




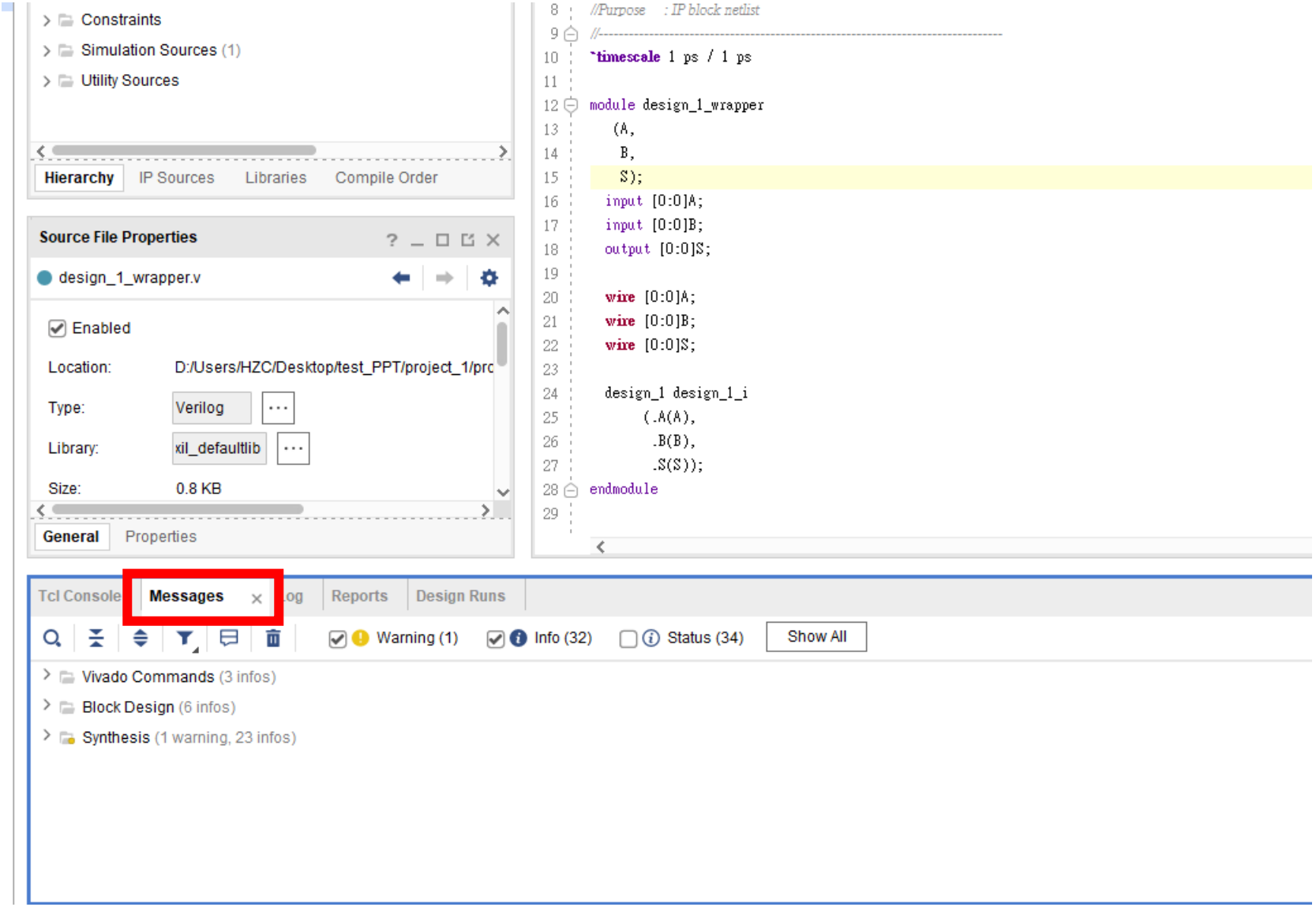
4-1、Synthesis



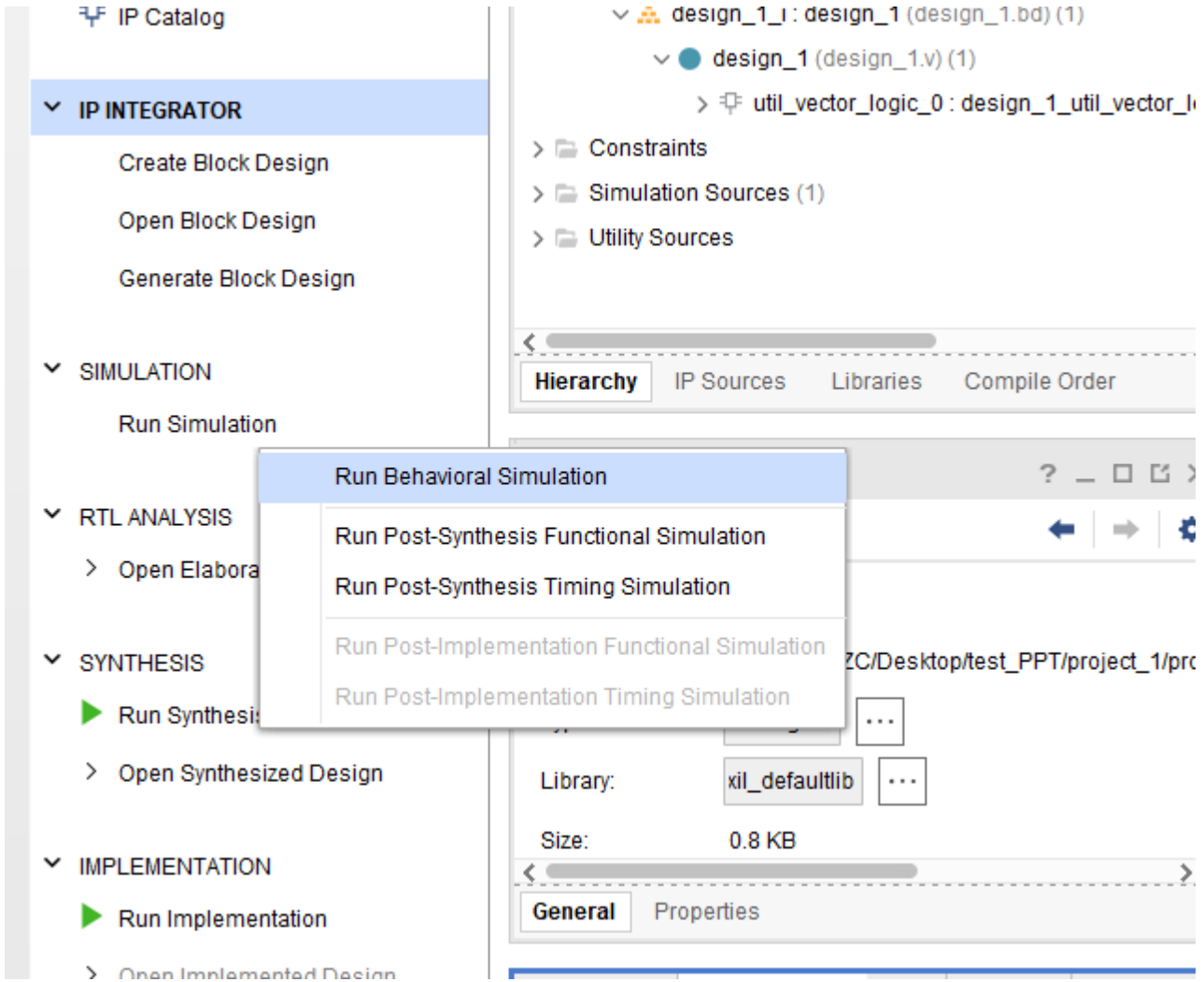
4-2、 Synthesis



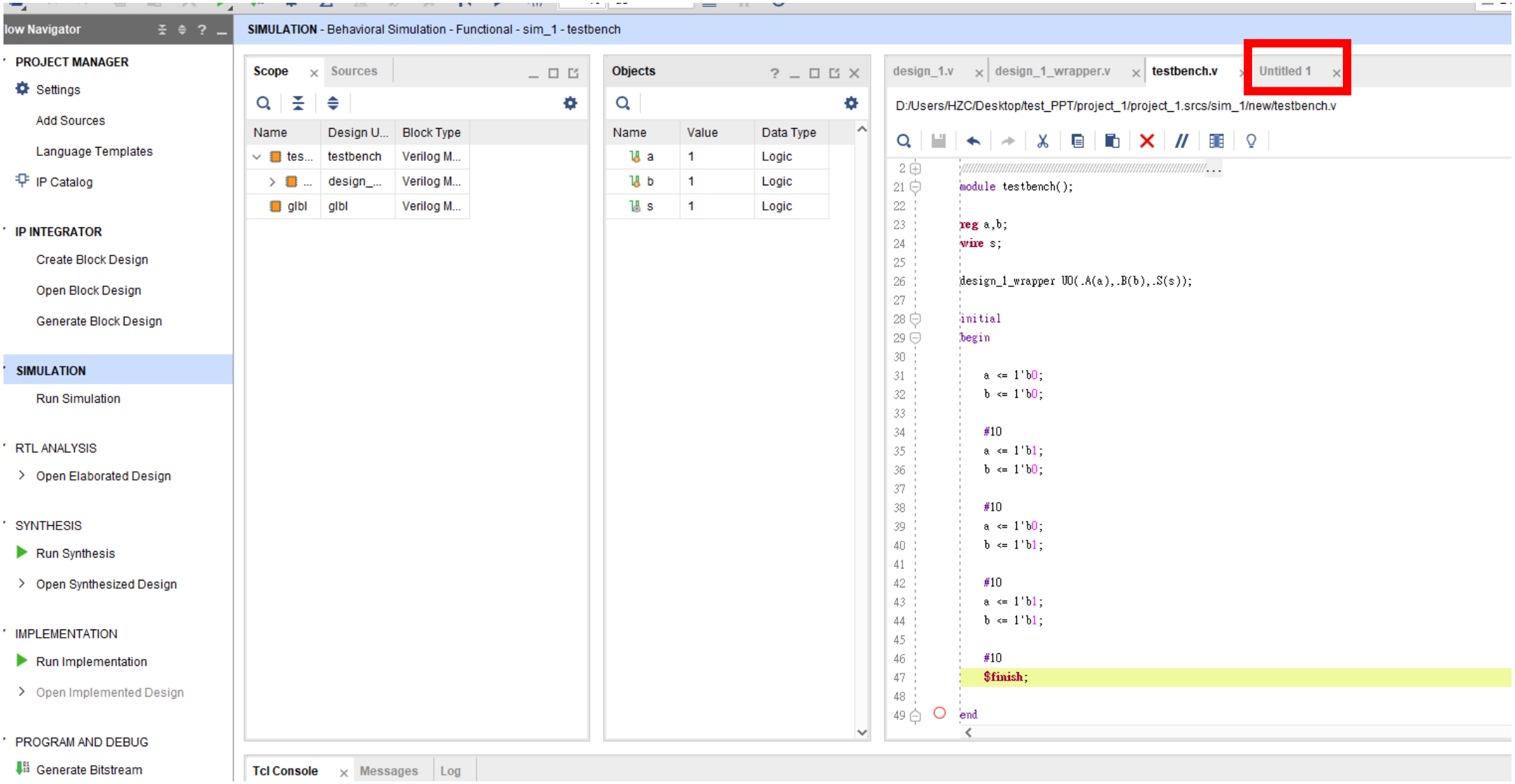
4-3、 Synthesis



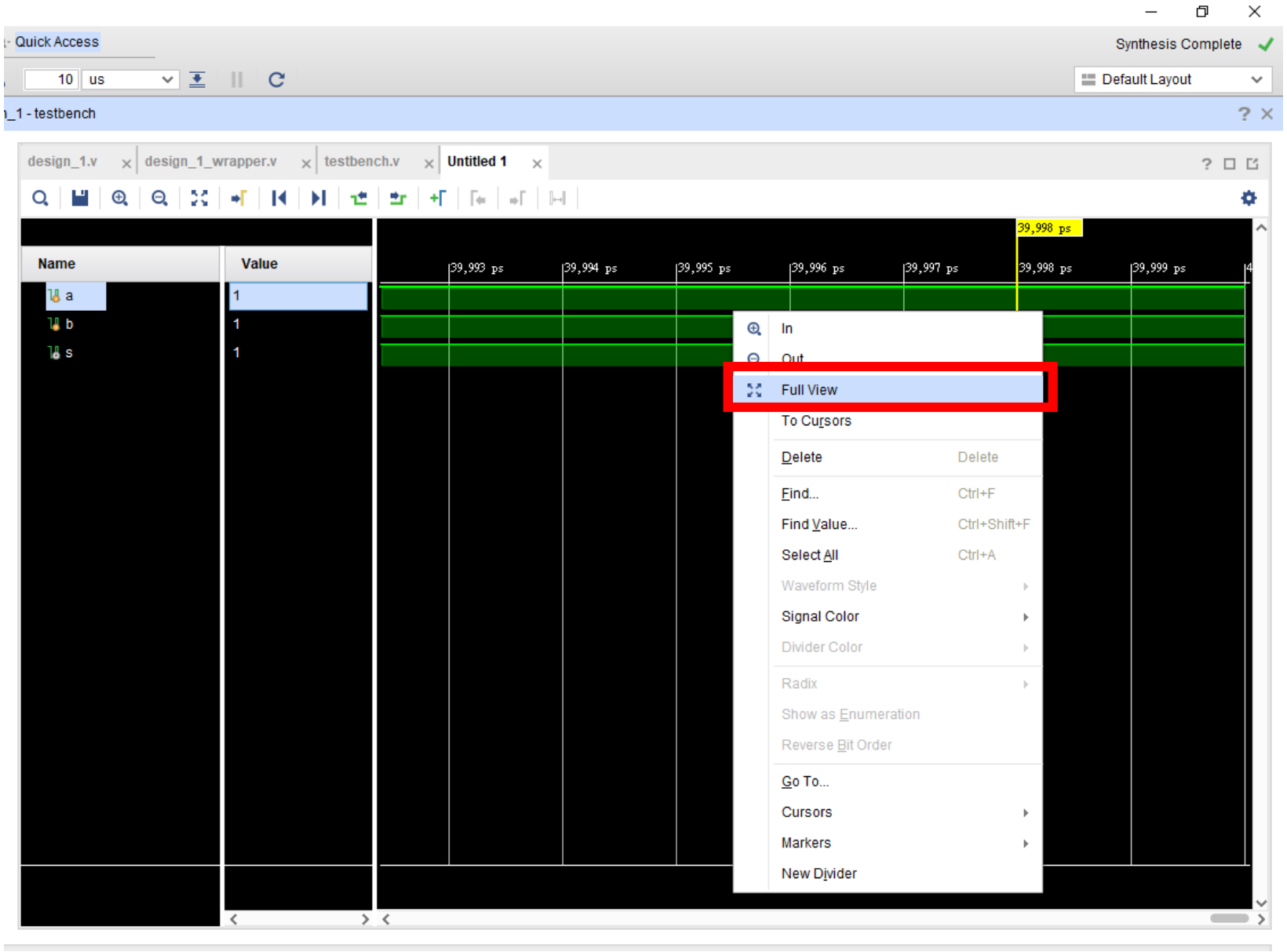
5-1、Simulation



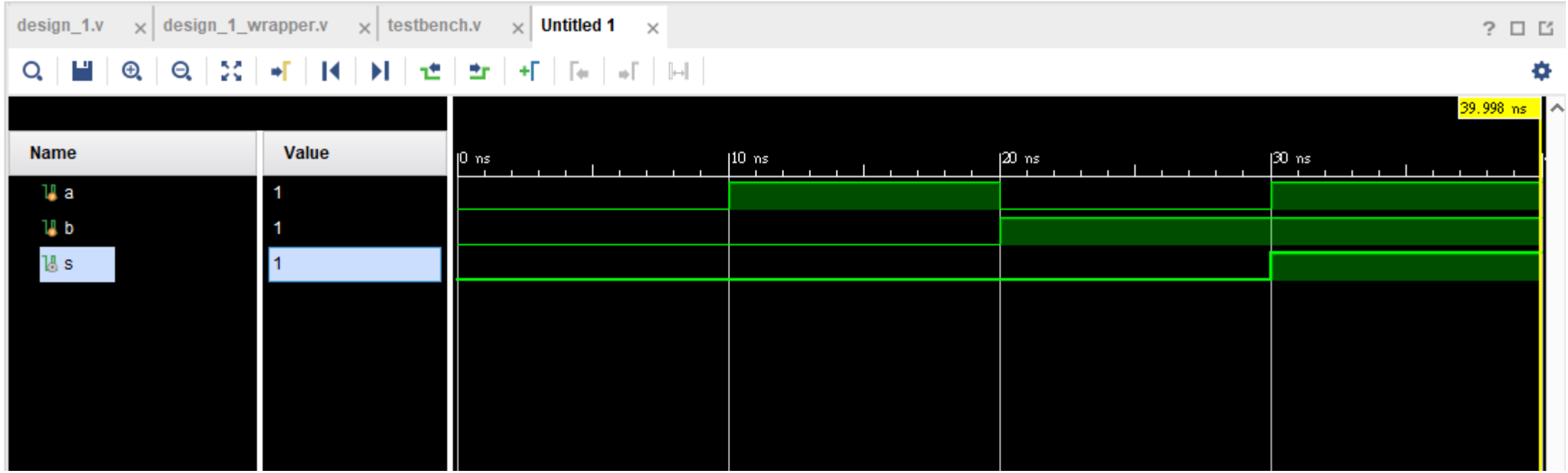
5-2、Simulation

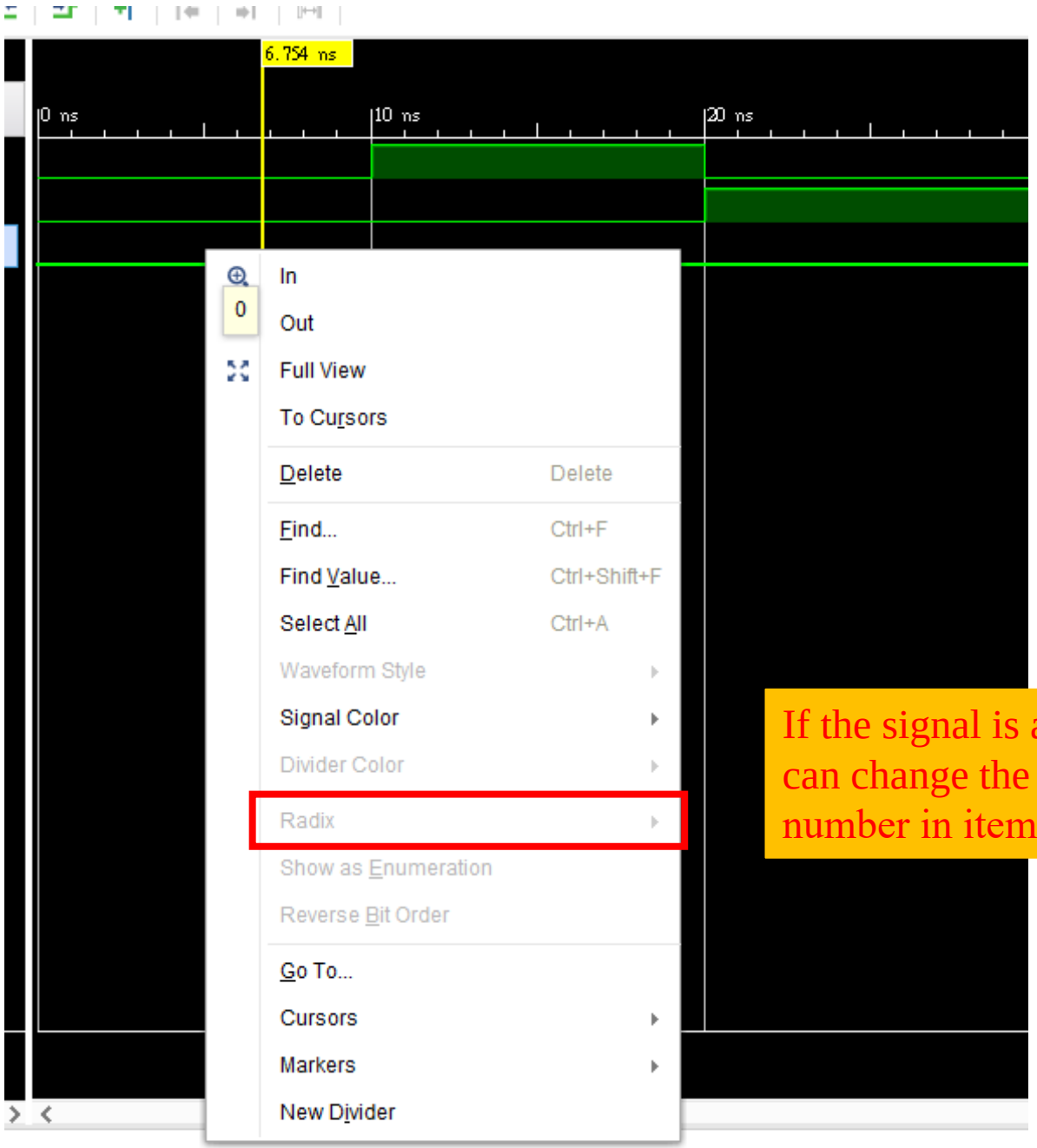


5-3、Simulation



5-4、 Simulation





If the signal is a vector, you can change the displayed number in item “Radix”.