DSLab. 07 Karnaugh Map (2)

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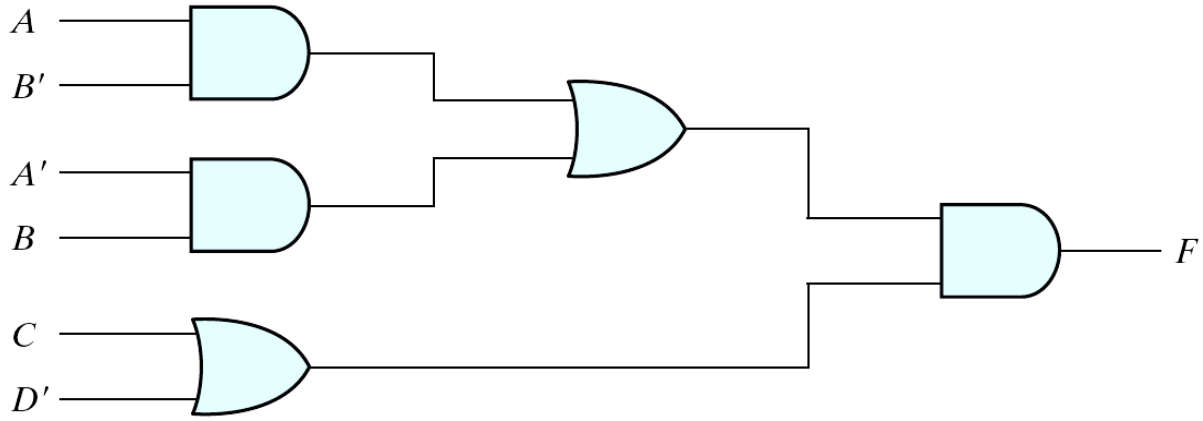
- Design and Verify the following circuits using Verilog HDL and Schematic
- Verilog
  - Behavioral level modeling
  - Dataflow modeling
  - Structural level modeling
- Schematic
- Please write and upload the lab report (Lab07) -- Due on 2022/10/21 23:59

Exercise 1

- $F = (AB' + A'B)(C + D')$
  - Implement *F* with AND-OR gates (denoted as *F1*)
  - Implement *F* with multi-level NAND gate circuit (denoted as *F2*)
  - Implement *F* with multi-level NOR gate circuit (denoted as *F3*)
  - Verify *F1* = *F2* = *F3* (using Verilog Structural level modeling)



(a) AND–OR gates

Exercise 2

- Simplify the following Boolean function using Karnaugh maps:
  $F(x,y,z) = \Sigma\,(1,2,3,4,5,7)$
- Find the simplest sum of products (*F4*) and draw its logic diagram (two-level implementation)
  - Implement *F4* with two-level NAND gate circuit (denoted as *F5*)
  - *F6* = (*F4*')', implement *F6* with two-level OR-NAND (OAI) circuit
  - Verify *F4* = *F5* = *F6* (using Verilog Structural level modeling)

Exercise 3

- Simplify the following Boolean function using Karnaugh maps: $F(x,y,z) = \Sigma\,(1,2,3,4,5,7)$
- Find the simplest product of sums (*F7*) and draw its logic diagram (two-level implementation)
  - Implement *F7* with two-level NOR gate circuit (denoted as *F8*)
  - Implement *F7* with two-level AND-NOR (AOI) circuit (denoted as *F9*)
  - Verify *F7* = *F8* = *F9* (using Verilog Structural level modeling)