Lab11

實驗主題:D Latch and D Flip-flop

實驗日期:2022/11/14

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實驗內容: Design and Verify the following circuits using Verilog HDL:

D Latch D Flip-Flops

Exercise1:

D Latch

D Latch Design and verify the D latch using Verilog HDL

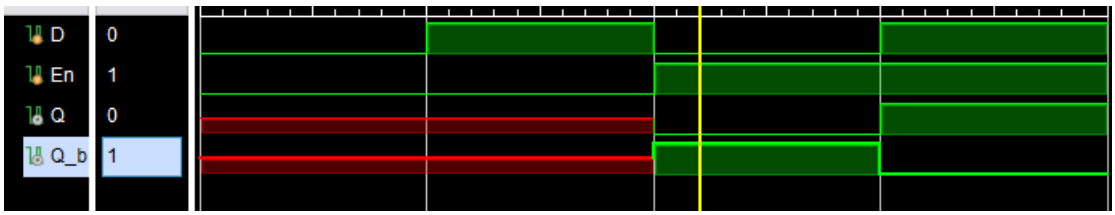
Code:

```
module e1(Q,Q_b,D,En);
    output Q,Q_b;
    input D,En;
    wire n1,n2,n3;
    nand(n1,D,En);
    not(n2,D);
    nand(n3,n2,En);
    nand(Q,n1,Q_b);
    nand(Q_b,n3,Q);
endmodule
```

Tb:

```
module tb;
reg D,En;
wire Q,Q_b;
e1 UUT(.D(D),.En(En),.Q(Q),.Q_b(Q_b));
initial begin
   En=1'b0;D=1'b0;#10
   En=1'b0;D=1'b1;#10
   En=1'b1;D=1'b0;#10
   En=1'b1;D=1'b1;#10
   $finish;
   end
endmodule
```

波形圖:



Exercise1 實驗結果與分析:

D Latch 功能正常。

Exercise2:

Master-slave D Flip-Flop

Design and verify the positive-edge-triggered master-slave D flip-flop using Verilog HDL

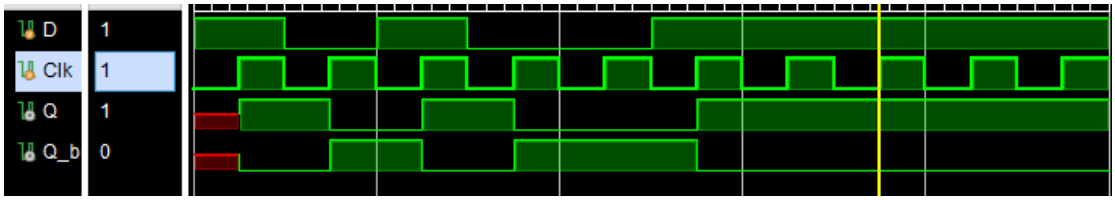
Code:

```
module e1(Q,Q_b,D,En);
    output Q,Q_b;
    input D,En;
    wire n1,n2,n3;
    nand(n1,D,En);
    not(n2,D);
    nand(n3,n2,En);
    nand(Q,n1,Q_b);
    nand(Q_b,n3,Q);
endmodule
module e2(Q,Q_b,D,Clk);
    output Q,Q_b;
    input D,Clk;
    wire Clk_not,n1,n2;
    not(Clk_not,Clk);
    e1 DL1(n1,n2,D,Clk_not);
    e1 DL2(Q,Q_b,n1,Clk);
endmodule
```

Tb:

```
module tb;
    reg D,Clk;
    wire Q,Q_b;
    e2 UUT(.D(D),.Clk(Clk),.Q(Q),.Q_b(Q_b));
    initial #100 $finish;
    initial begin Clk=0; forever #5 Clk = ~Clk; end
    initial fork
    D=1;
    #10D=0;
    #20D=1;
    #30D=0;
    #40D=0;
    #50D=1;
     join
endmodule
```

波形圖:



Exercise2 實驗結果與分析:

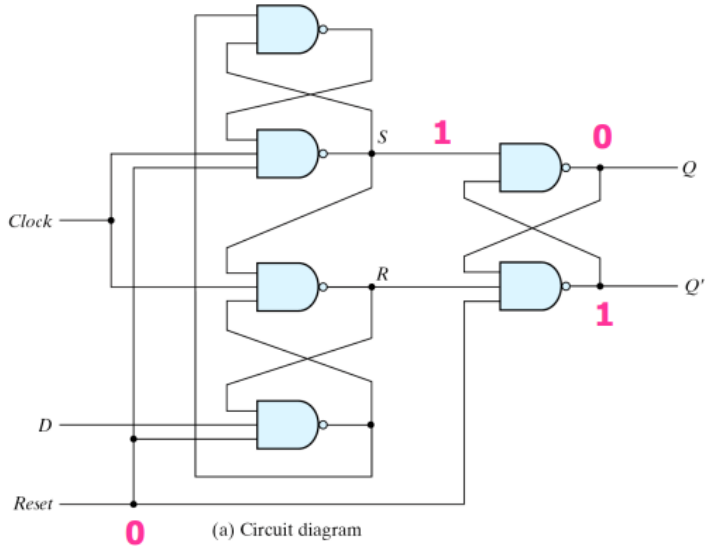
Master-slave D Flip-Flop 功能正常。

Exercise3:

D flip-flop with asynchronous reset

Design and verify the D flip-flop with asynchronous reset shown in Fig. 5.14 using Verilog HDL

Fig. 5.14:



(a) Circuit diagram

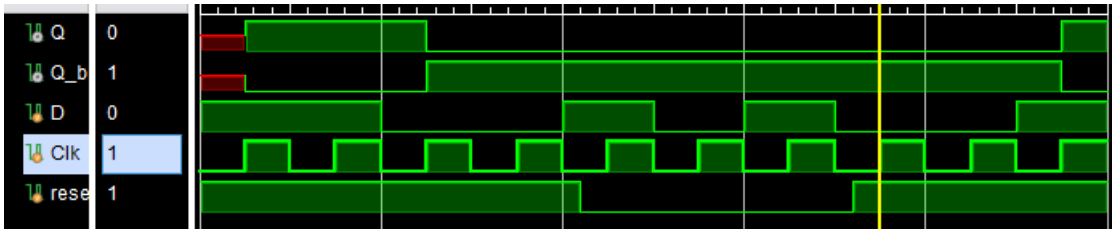
Code:

```
module e3(Q,Q_b,Clk,D,reset);
    output Q,Q_b;
    input Clk,D,reset;
    wire n1,n2,n3,n4,reset_not;
    //not(reset_not,reset);
    nand(n1,n4,n2);
    nand(n2,Clk,n1,reset);
    nand(n3,n2,Clk,n4);
    nand(n4,n3,D,reset);
    nand(Q,n2,Q_b);
    nand(Q_b,n3,Q,reset);
endmodule
```

Tb:

```
module tb;
wire Q, Q_b;
reg D, Clk, reset;
e3 u3 (.Q(Q), .Q_b(Q_b), .D(D), .Clk(Clk), .reset(reset));
initial #100 $finish;
initial begin Clk = 0; forever #5 Clk = ~Clk; end
initial fork
D = 1;
reset = 1;
#20 D = 0;
#40 D = 1;
#50 D = 0;
#60 D = 1;
#70 D = 0;
#90 D = 1;
#42 reset = 0;
#72 reset = 1;
join
endmodule
```

波形圖:



Exercise3 實驗結果與分析:

Flipflop 功能正常。

實驗心得

這次的實驗室這學期第一次遇到 sequential circuit，實作了最基礎的記憶元件，latch 跟 flip-flop。在這次上課之前我其實還對他們的行為不怎麼熟悉，但在這次實作之後，對他們的行為有了掌握。另外近兩次實驗課時天花板上會有老鼠亂竄的聲響，由於我頭上的天花板已經裂了三分之一，因此我在實作途中的心理壓力實屬巨大。除此之外，本次實作過程都還算順利。