DSLab. 08 Combinational Logic

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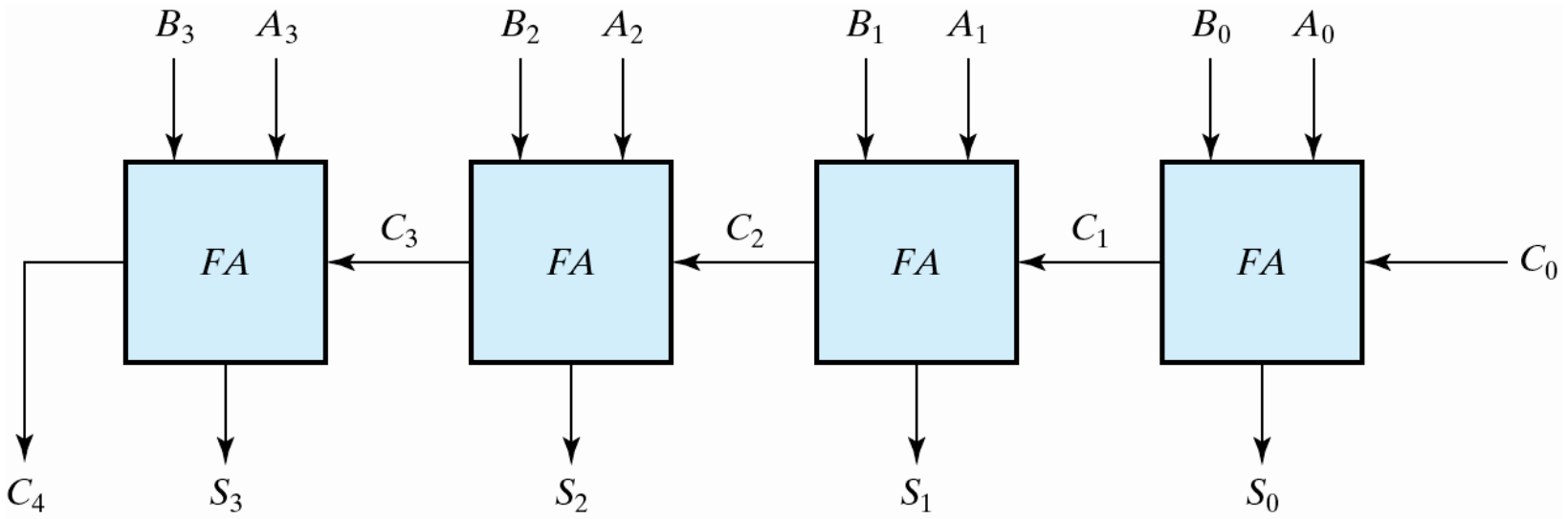
- Design and verify the following circuits using Verilog HDL and Schematic
- Verilog
  - Behavioral level modeling
  - Dataflow modeling
  - Structural level modeling
- Schematic
- Please write and upload the lab report (Lab08) -- Due on 2022/10/28 23:59

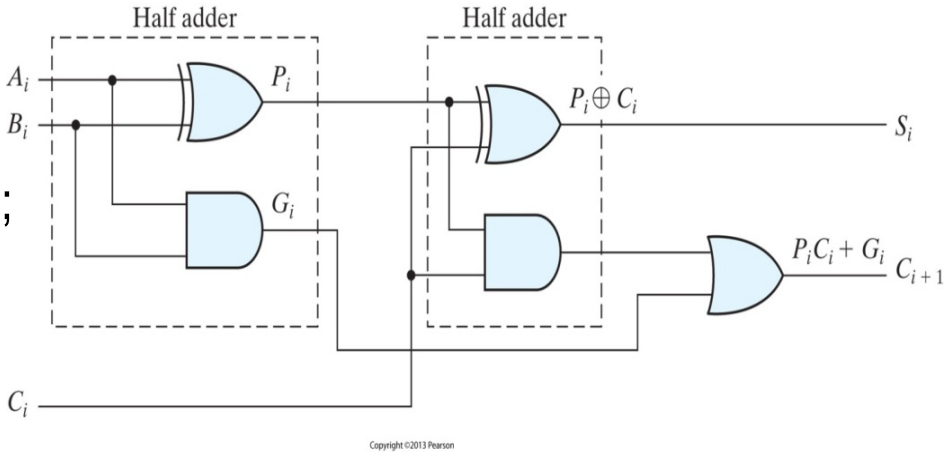
4-bit Ripple-Carry Adder



Gate-level Description of 4-bit Ripple-Carry Adder

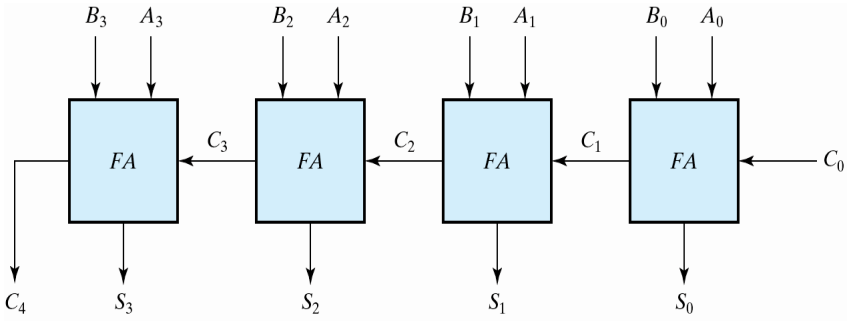
```
module half_adder (output S, C, input x, y);
   xor (S, x, y);
   and (C, x, y);
endmodule

module full_adder (output S, C, input x, y, z);
   wire     S1, C1, C2;
   half_adder HA1 (S1, C1, x, y);
   half_adder HA2 (S, C2, S1, z);
   or G1 (C, C2, C1);
endmodule
```




```
module ripple_carry_4_bit_adder ( output [3: 0] Sum, output C4, input [3:0]  A, B, input C0);
    wire          C1, C2, C3;      // Intermediate carries

    full_adder    FA0 (Sum[0], C1, A[0], B[0], C0),
                  FA1 (Sum[1], C2, A[1], B[1], C1),
                  FA2 (Sum[2], C3, A[2], B[2], C2),
                  FA3 (Sum[3], C4, A[3], B[3], C3);
endmodule
```



Exercise 1: BCD to Excess-3 Code Converter (1/3)

- BCD to Excess-3 Code Converter

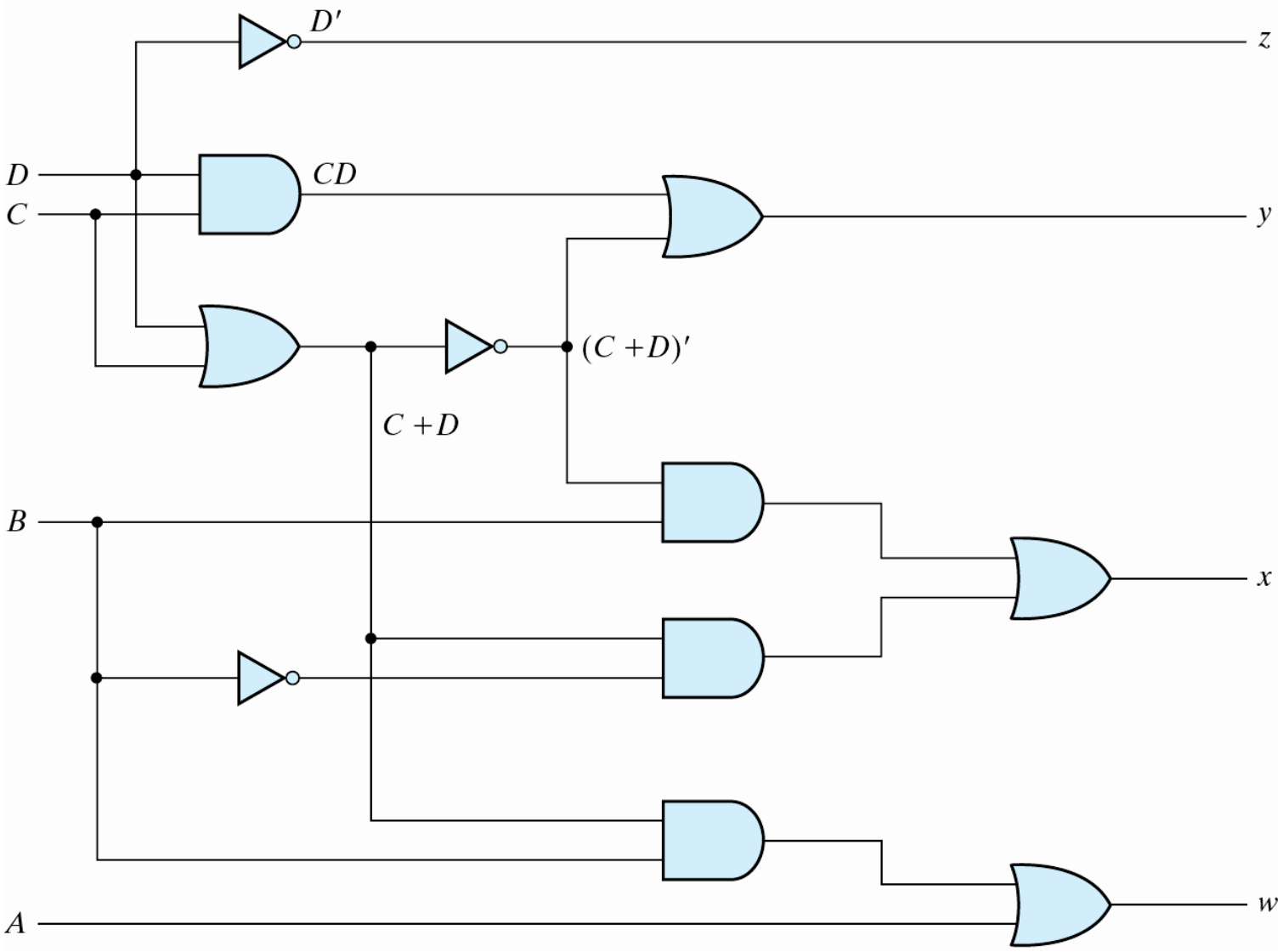
Table 4.2
Truth Table for Code-Conversion Example

Input BCD				Output Excess-3 Code			
A	*B*	*C*	*D*	*w*	*x*	*y*	*z*
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Exercise 1: BCD to Excess-3 Code Converter (2/3)

- The simplified functions (Circuit 1)
  - $z = D'$
  - $y = CD+C'D'$
  - $x = B'C+B'D+BC'D'$
  - $w = A+BC+BD$
- Another implementation (Circuit 2)
  - $z = D'$
  - $y = CD+C'D' = CD + (C+D)'$
  - $x = B'C+B'D+BC'D' = B'(C+D)+B(C+D)'$
  - $w = A+BC+BD = A+B(C+D)$
- Draw the logic diagrams of Circuit 1 and Circuit 2, and then verify Circuit 1 = Circuit 2 (using Verilog Dataflow modeling)

Exercise 1: BCD to Excess-3 Code Converter (3/3)

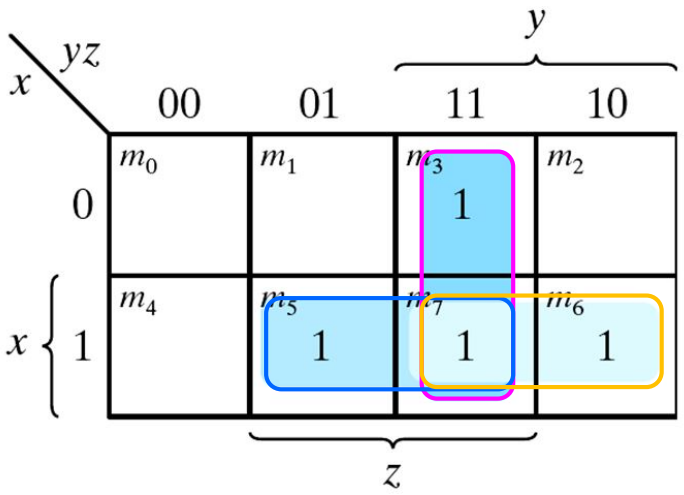


Exercise 2: Full-Adder (1/2)

- Derive the following Boolean functions using Karnaugh maps
- $S = z \oplus (x \oplus y)$, $C = xy + xz + yz$ (Circuit 1)
- Draw the logic diagram of Circuit 1

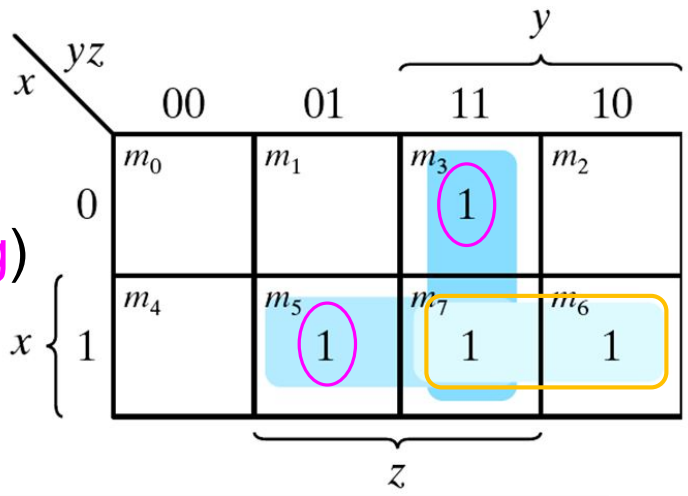
Table 4.4
Full Adder

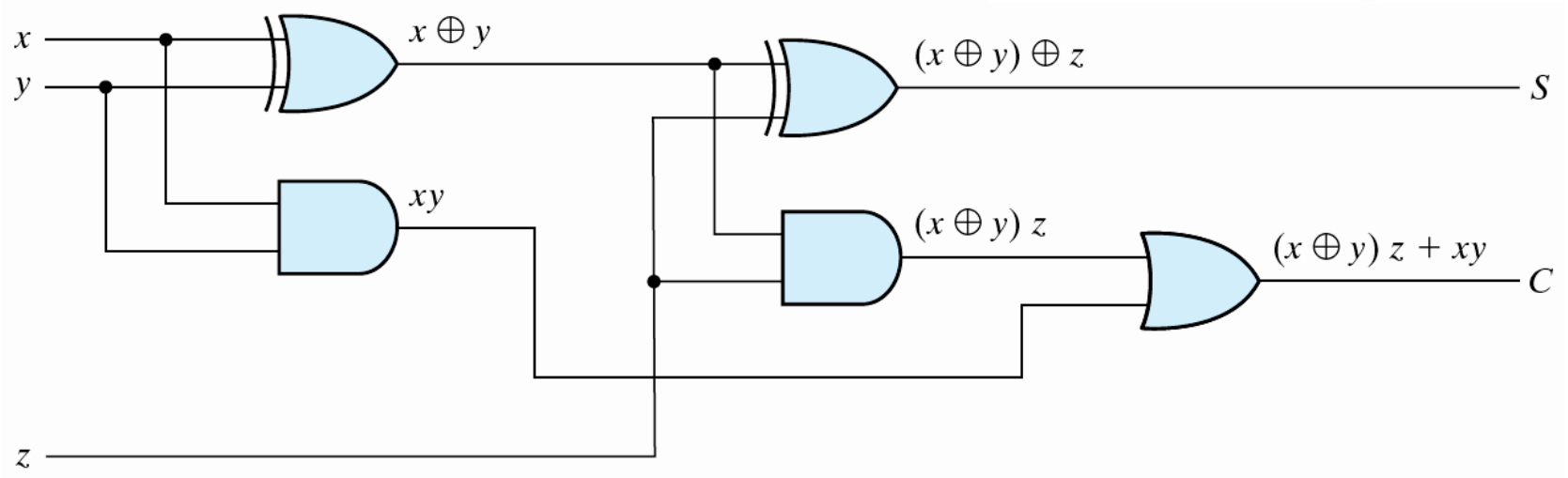
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Exercise 2: Full-Adder (2/2)

- Derive the following Boolean functions using Karnaugh maps
- $S = z \oplus (x \oplus y)$, $C = z(x \oplus y) + xy$ (Circuit 2)
- Draw the logic diagram of Circuit 2
- Verify Circuit 1 = Circuit 2
  (using Verilog Structural level modeling)





Exercise 3: 8-bit Ripple-carry Adder

- Design and verify the 8-bit ripple-carry adder composed of eight full-adders (using Verilog Structural level modeling)