

Introduction of Vivado

Open Vivado



1-1 、 Create a new project

The screenshot displays the Vivado 2018.3 software interface. At the top is a menu bar with 'File', 'Flow', 'Tools', 'Window', 'Help', and a 'Quick Access' search bar. Below the menu bar is the Vivado logo and 'HLx Editions' text. The main workspace is divided into three horizontal panels. The top panel, titled 'Quick Start', has a red rectangular box around the 'Create Project >' button. Below it is the 'Tasks' panel with links for 'Manage IP >', 'Open Hardware Manager >', and 'Xilinx Tcl Store >'. The bottom panel is the 'Learning Center' with a link to 'Documentation and Tutorials >'. On the right side of the interface is a 'Recent Projects' panel listing several projects with their full file paths.

Vivado 2018.3

File Flow Tools Window Help Q- Quick Access

VIVADO.
HLx Editions

Quick Start

Create Project >

Open Project >

Open Example Project >

Tasks

Manage IP >

Open Hardware Manager >

Xilinx Tcl Store >

Learning Center

Documentation and Tutorials >

Recent Projects

test_logic_gate
D:/SOPC/test_logic_gate

project_1
D:/SOPC/HW2/HW2_testbench/project_1

clk_system
D:/Users/HZC/Desktop/SOPC/HW3/clock/clk_system/clk_system

clk_ring
D:/Users/HZC/Desktop/SOPC/HW3/clock/clk_ring/clk_ring

project_1
D:/Users/HZC/Desktop/SOPC/HW3/clock/clk_system_test/project_1

project_1
D:/Users/HZC/Desktop/SOPC/HW3/clock/clk_test/project_1

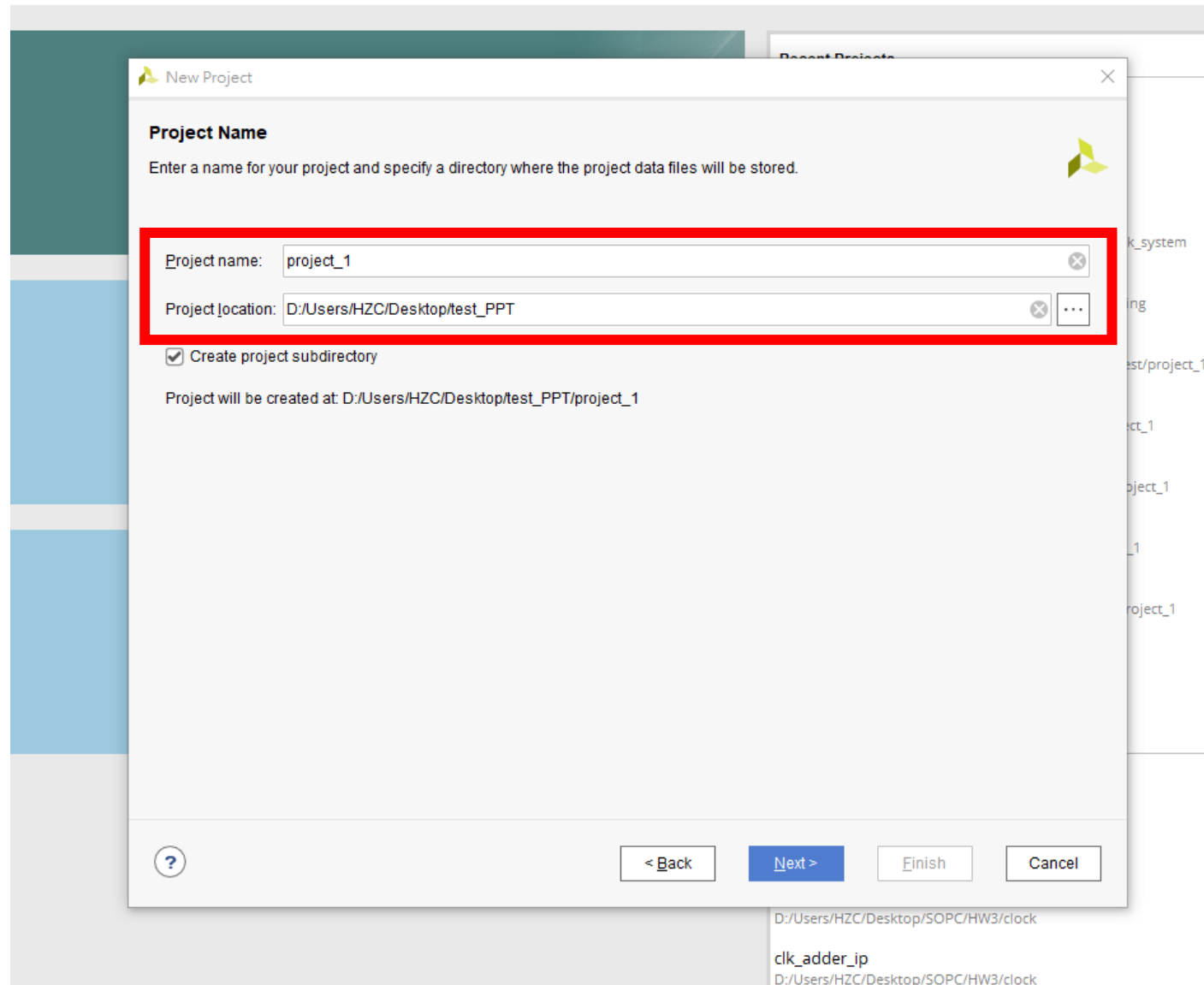
project_1
D:/Users/HZC/Desktop/SOPC/HW2/HW2_testbench/project_1

project_1
D:/Users/HZC/Desktop/SOPC/HW2/HW2_FPGA/project_1

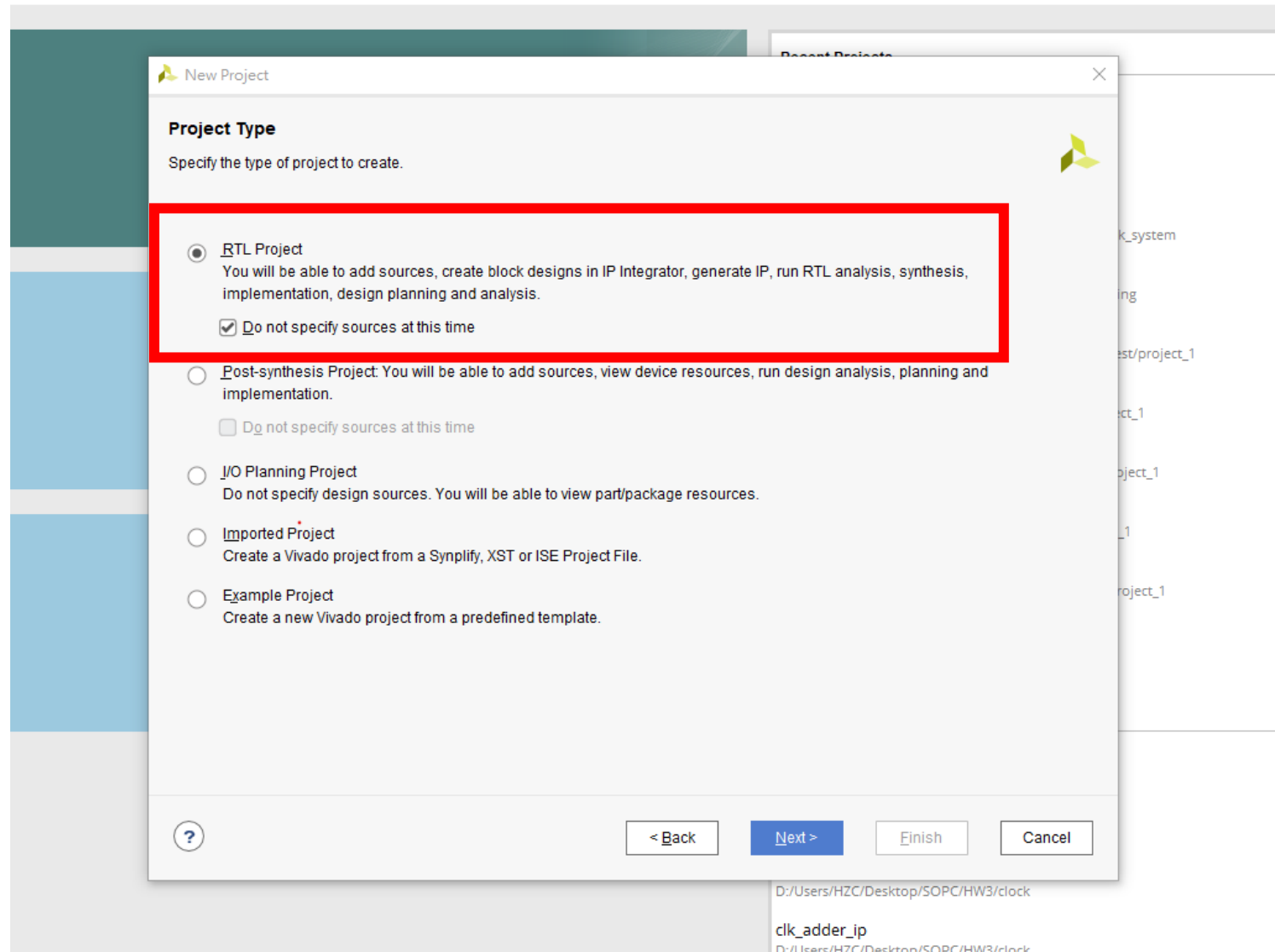
project_1
D:/Users/HZC/Desktop/SOPC/HW2/HW2_FPGA_CNN/project_1

project_1

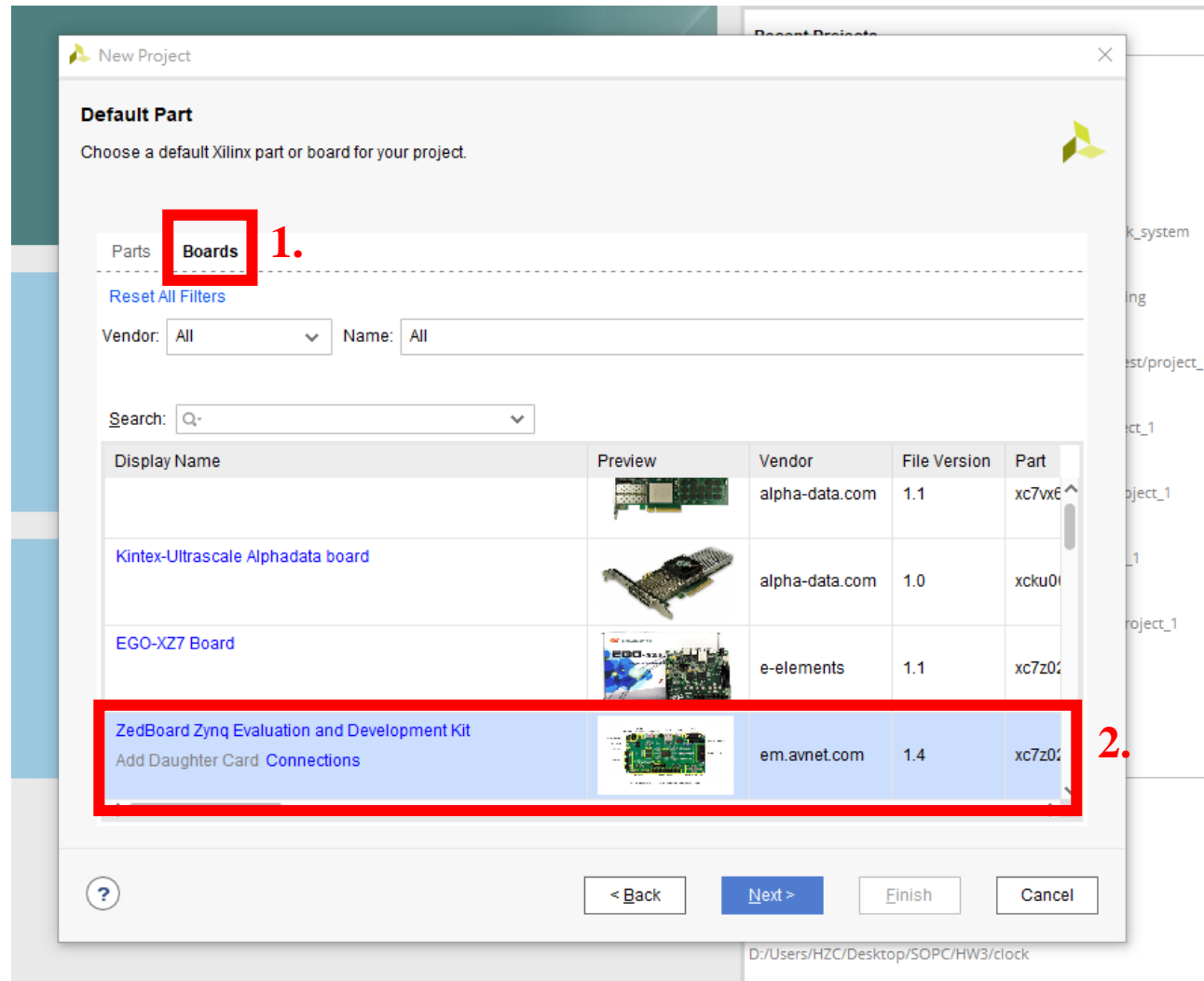
1-2 、 Create a new project



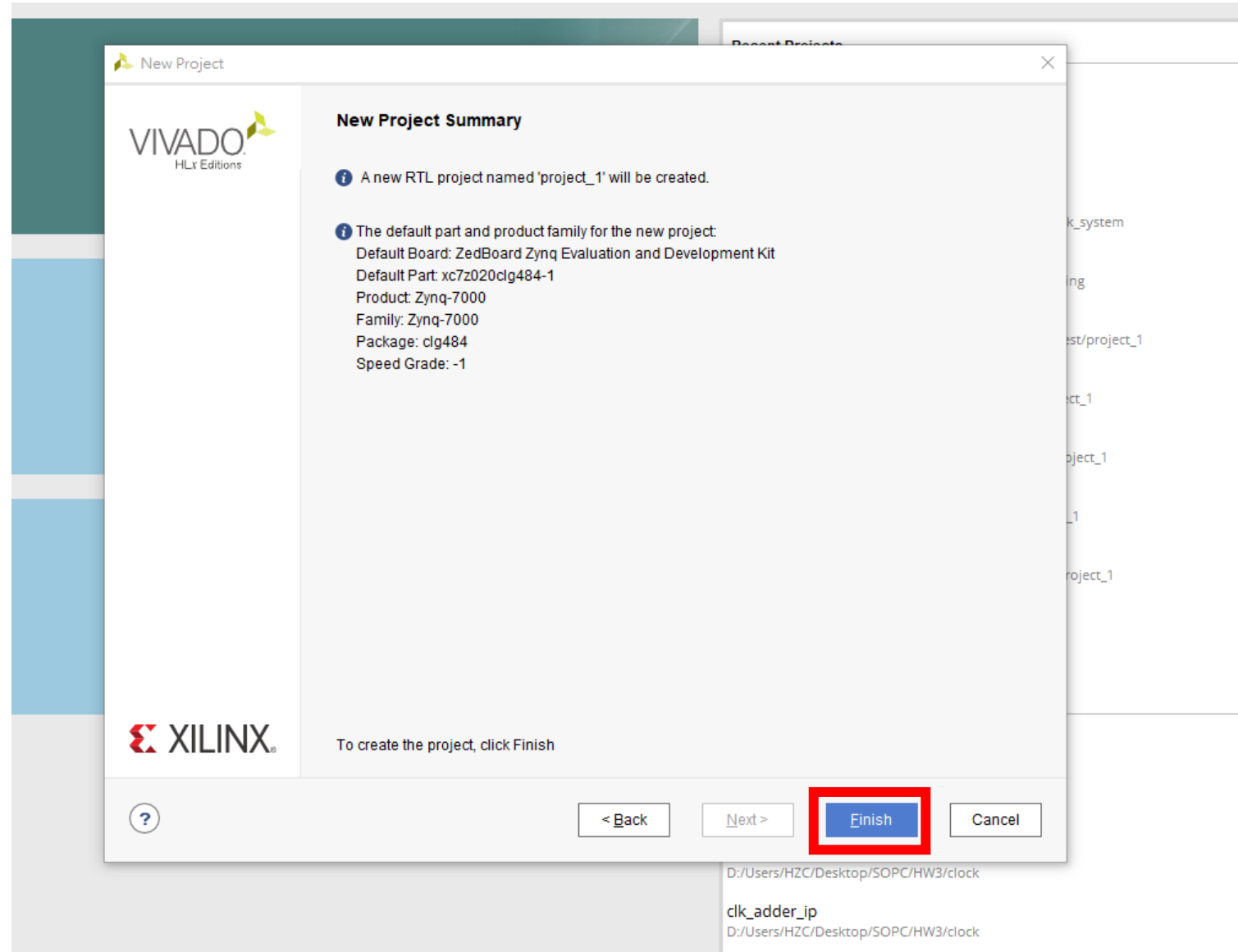
1-3 、 Create a new project



1-4 、 Create a new project



1-5 、 Create a new project



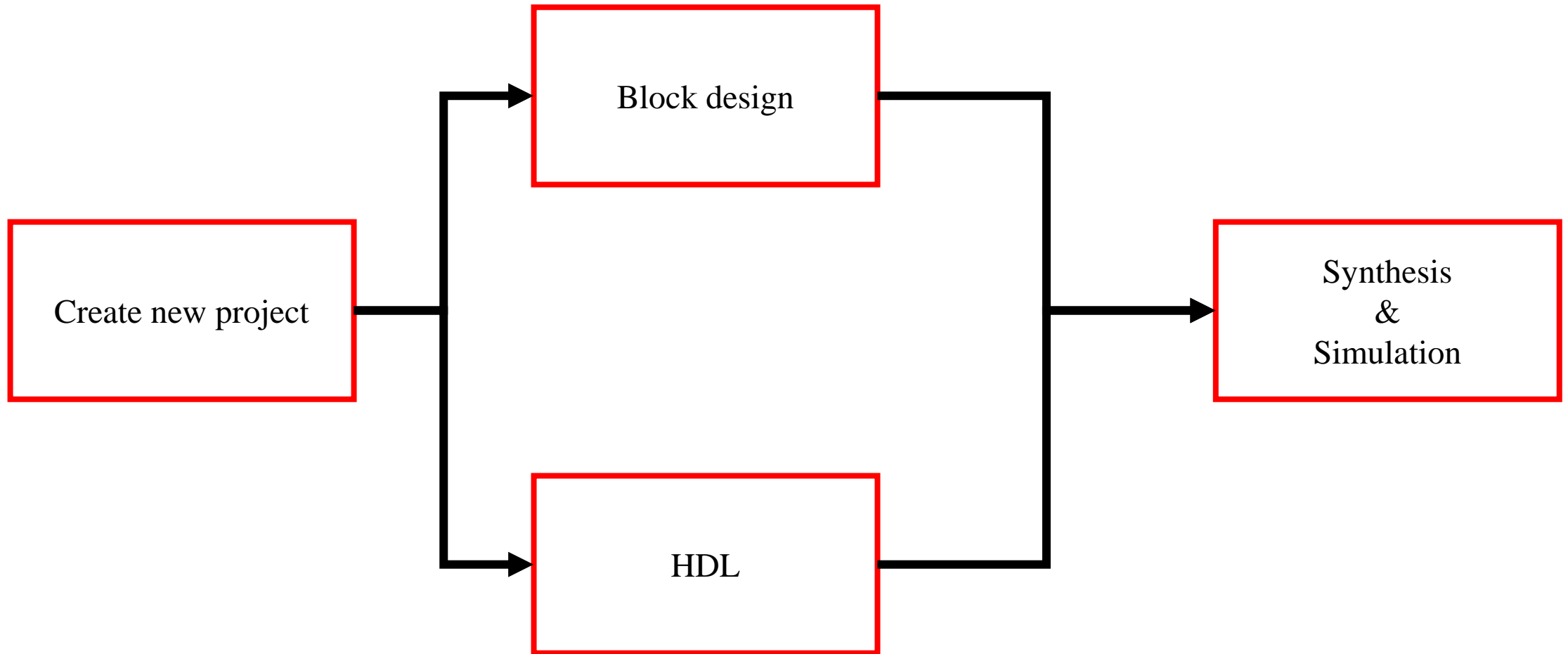
1-6 、 Create a new project

The screenshot displays the Vivado 2018.3 Project Manager interface for a new project named 'project_1'. The interface is divided into several panes:

- Flow Navigator:** A sidebar on the left containing project management tasks such as 'Settings', 'Add Sources', 'Language Templates', 'IP Catalog', 'IP INTEGRATOR', 'SIMULATION', 'RTL ANALYSIS', 'SYNTHESIS', 'IMPLEMENTATION', and 'PROGRAM AND DEBUG'.
- PROJECT MANAGER - project_1:** The main workspace, which includes:
 - Sources:** A tree view showing 'Design Sources' (Constraints, Simulation Sources, Utility Sources) and a 'sim_1' simulation source.
 - Properties:** A pane for viewing the properties of selected objects, currently showing 'Select an object to see properties'.
 - Project Summary:** A pane on the right providing an overview of the project settings.
- Project Summary:** This pane contains the following information:
 - Overview | Dashboard:** Includes 'Settings' and 'Edit' tabs. The 'Settings' tab shows:
 - Project name: project_1
 - Project location: D:/Users/HZC/Desktop/test_PPT/project_1
 - Product family: Zynq-7000
 - Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020dgg484-1)
 - Top module name: Not defined
 - Target language: Verilog
 - Simulator language: Mixed
 - Board Part:** Includes:
 - Display name: ZedBoard Zynq Evaluation and Development Kit
 - Board part name: em.avnet.com:zed:part0:1.4
 - Connectors: No connections
 - Repository path: D:/Xilinx/Vivado/2018.3/data/boards/board_files
 - URL: <http://www.zedboard.org>
 - Board overview: ZedBoard Zynq Evaluation and Development Kit
 - Synthesis and Implementation:** Both sections show a status of 'Not started'.

- Tcl Console / Messages / Log / Reports / Design Runs:** A bottom pane showing the 'Design Runs' table.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Rep
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)	Viva
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)	Viva



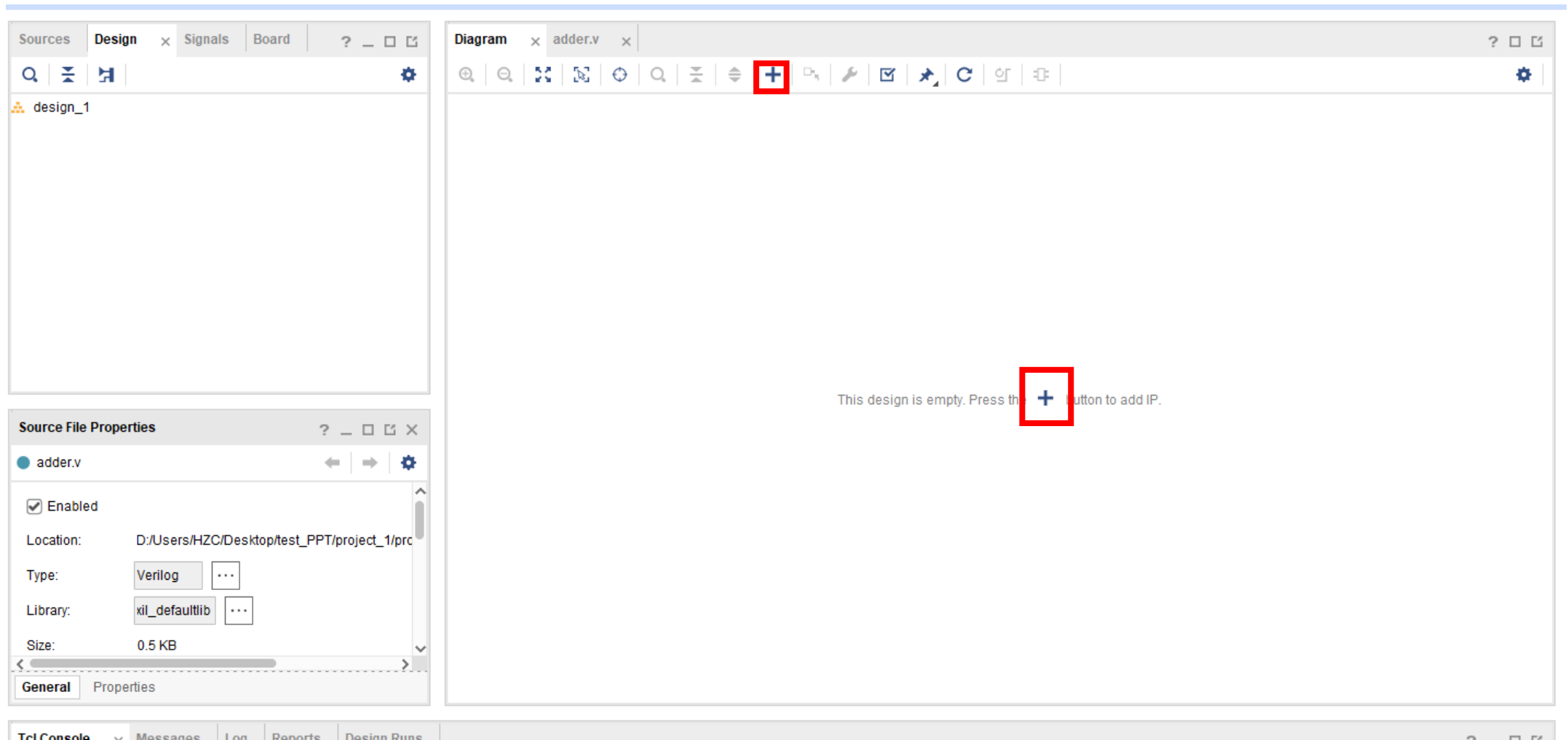
2-1 、 Block design

The screenshot displays the Xilinx IDE interface. On the left, the 'PROJECT MANAGER' pane shows the 'IP INTEGRATOR' section, with 'Create Block Design' highlighted by a red box and a red '1.' next to it. The 'Sources' pane shows the project structure, including 'Design Sources (1)' with 'adder (adder.v)'. The 'Source File Properties' pane shows details for 'adder.v', including its location, type (Verilog), library (xilinx_defaultlib), and size (0.5 KB). The 'Project Summary' pane shows the project path and the Verilog code for 'adder.v'. A 'Create Block Design' dialog box is open, highlighted by a red box and a red '2.' next to it. The dialog box prompts the user to specify the name of the block design, with 'design_1' entered in the 'Design name' field. The 'Directory' is set to '<Local to Project>' and the 'Specify source set' is set to 'Design Sources'.

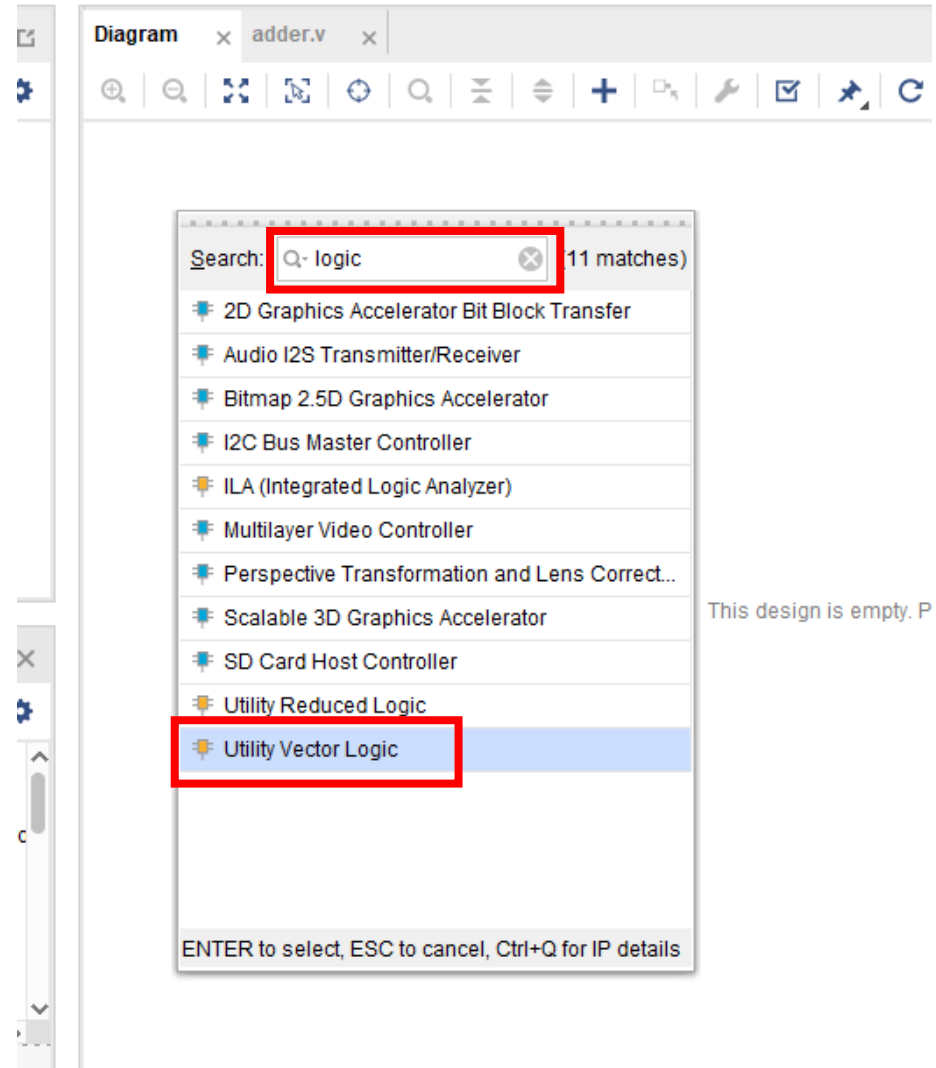
1.

2.

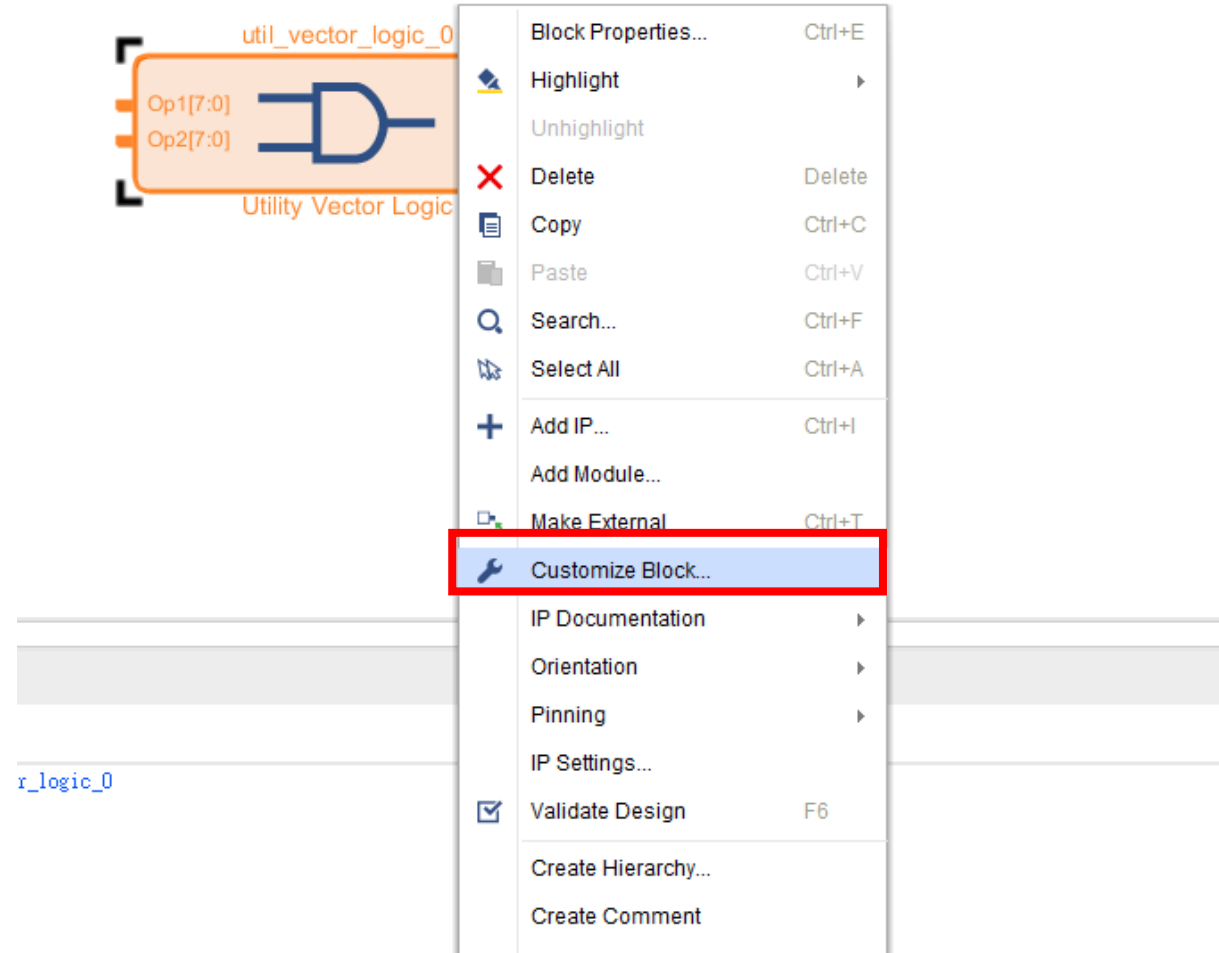
2-2 、 Block design



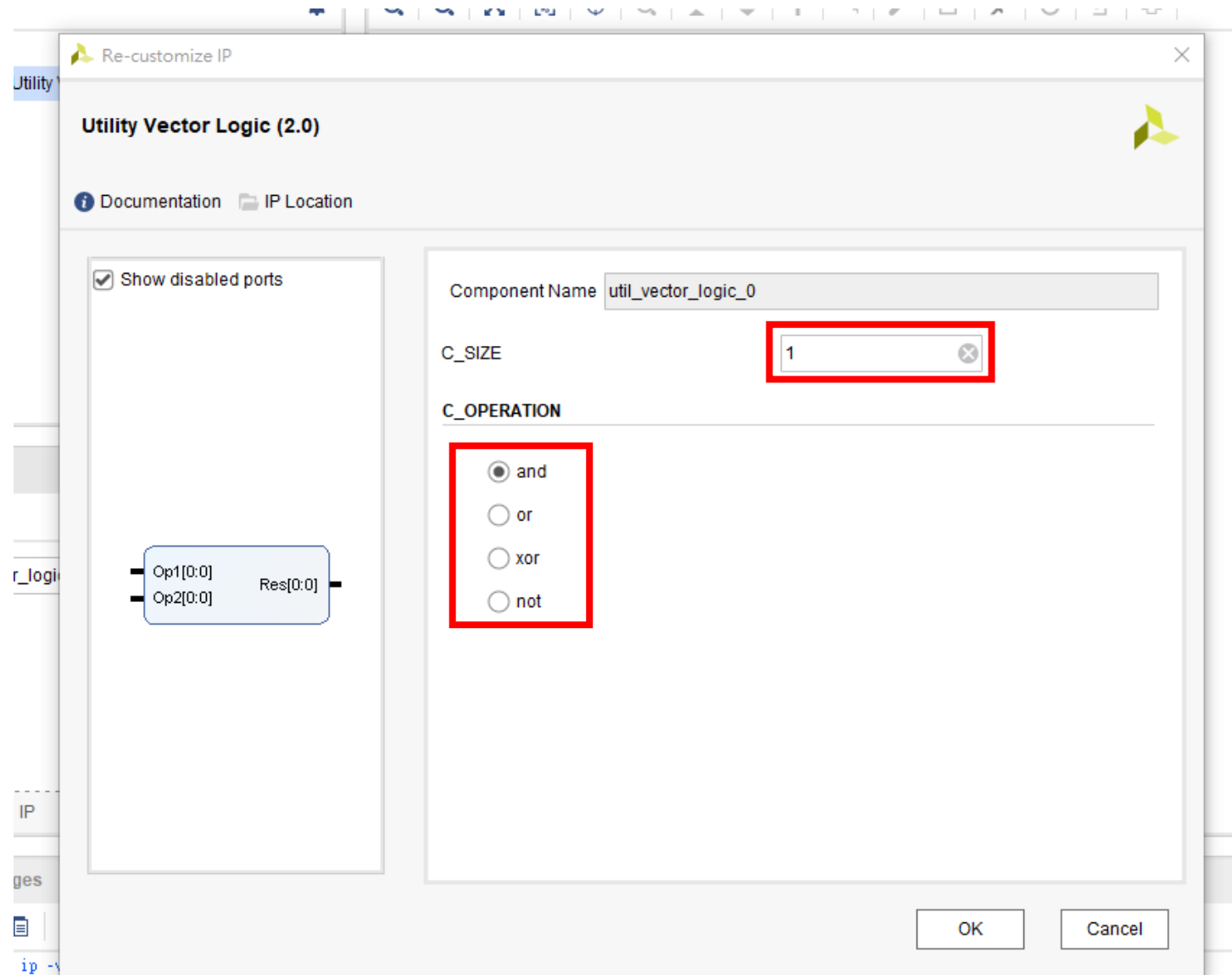
2-3 、 Block design



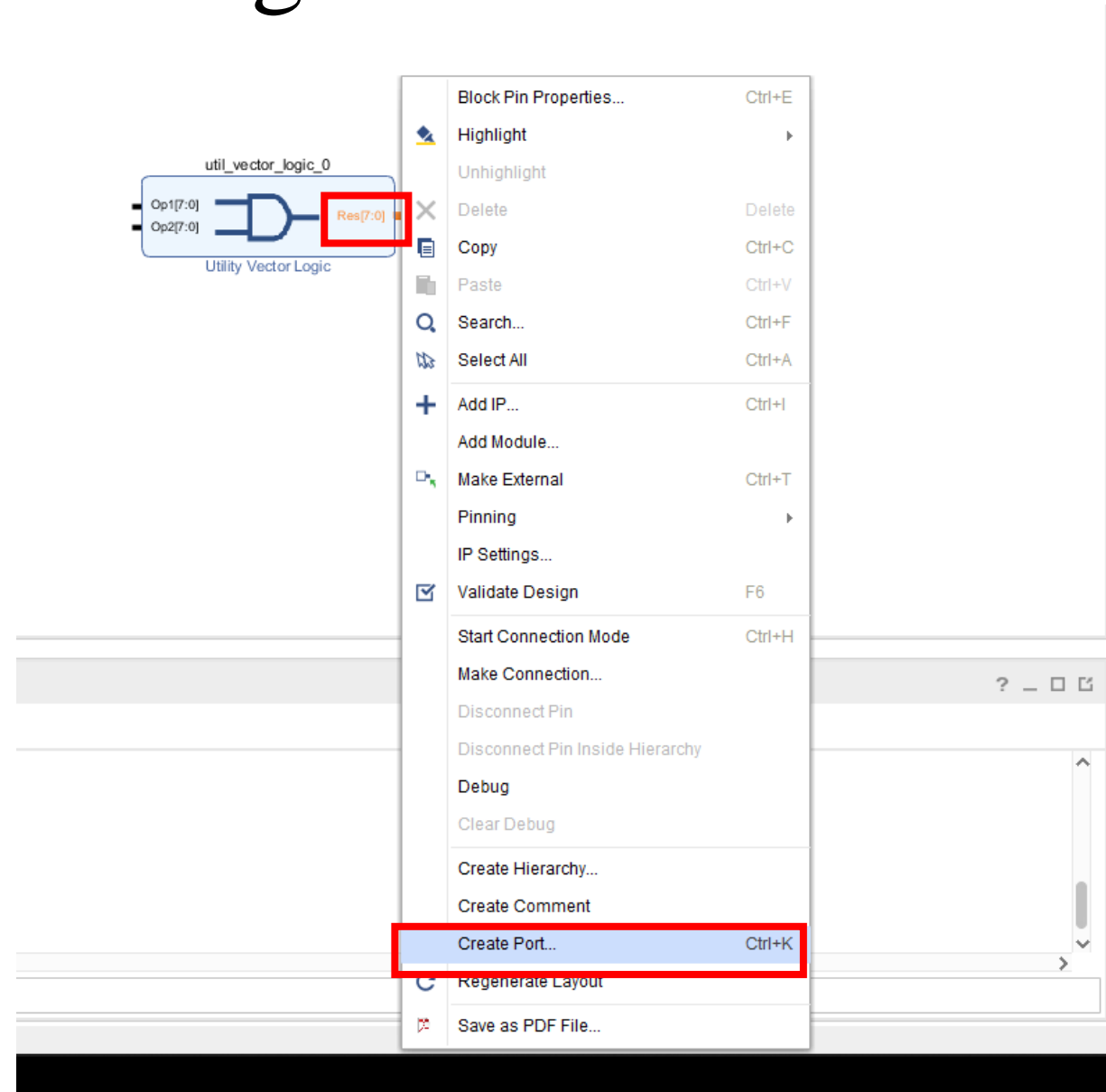
2-4 、 Block design



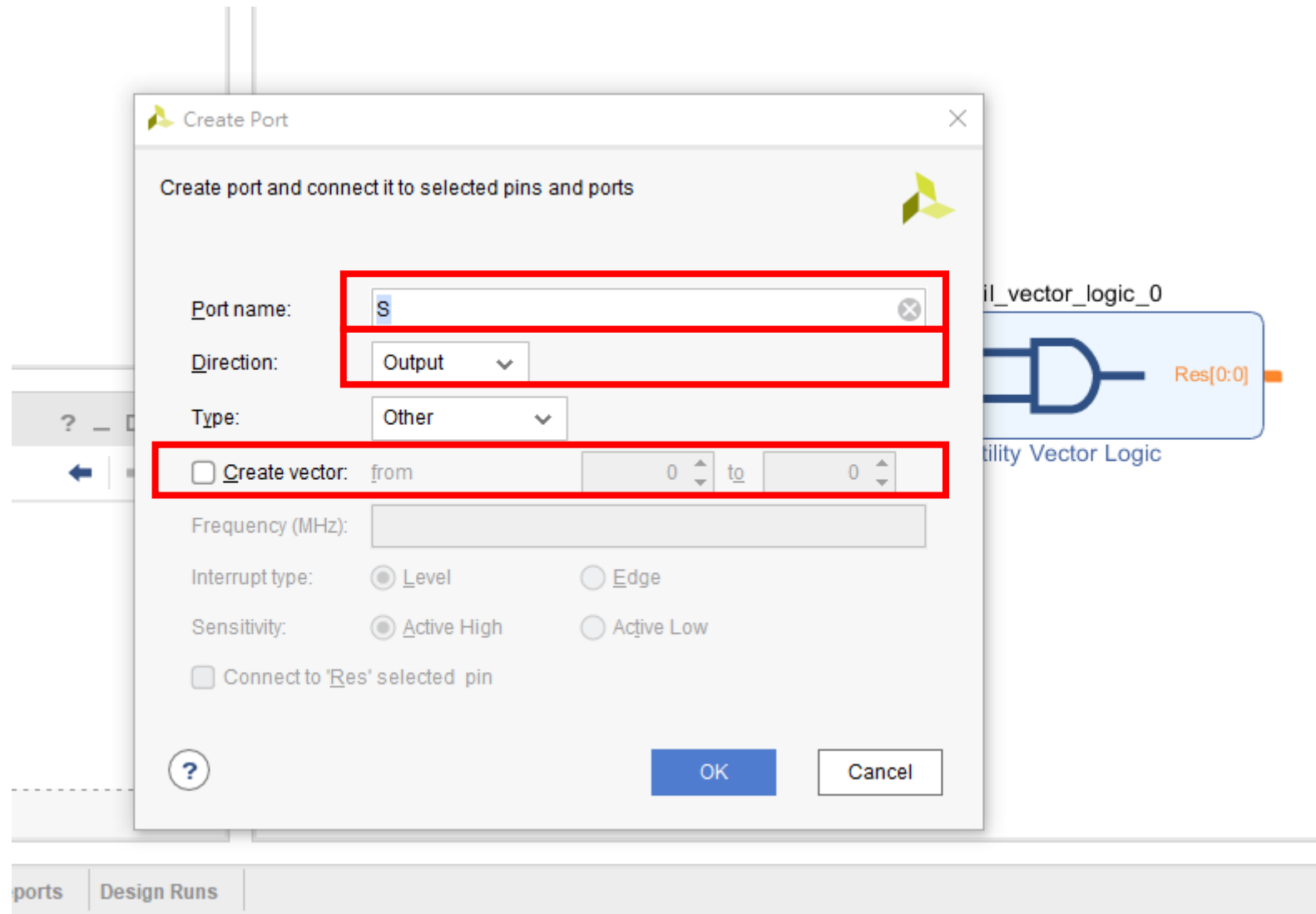
2-5 、 Block design



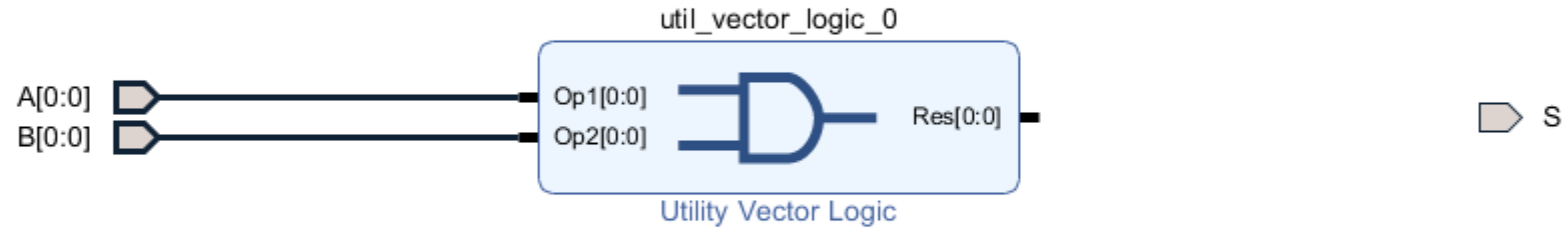
2-6 、 Block design



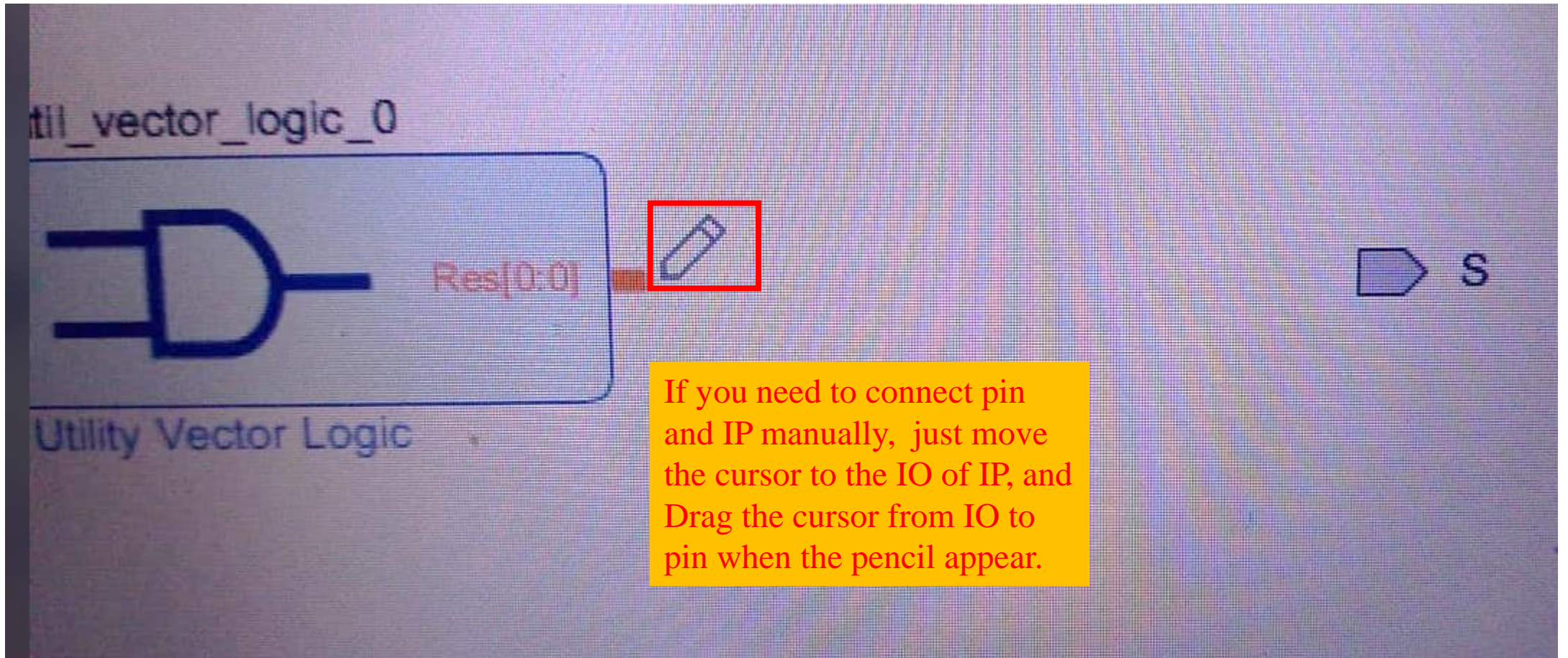
2-7 、 Block design



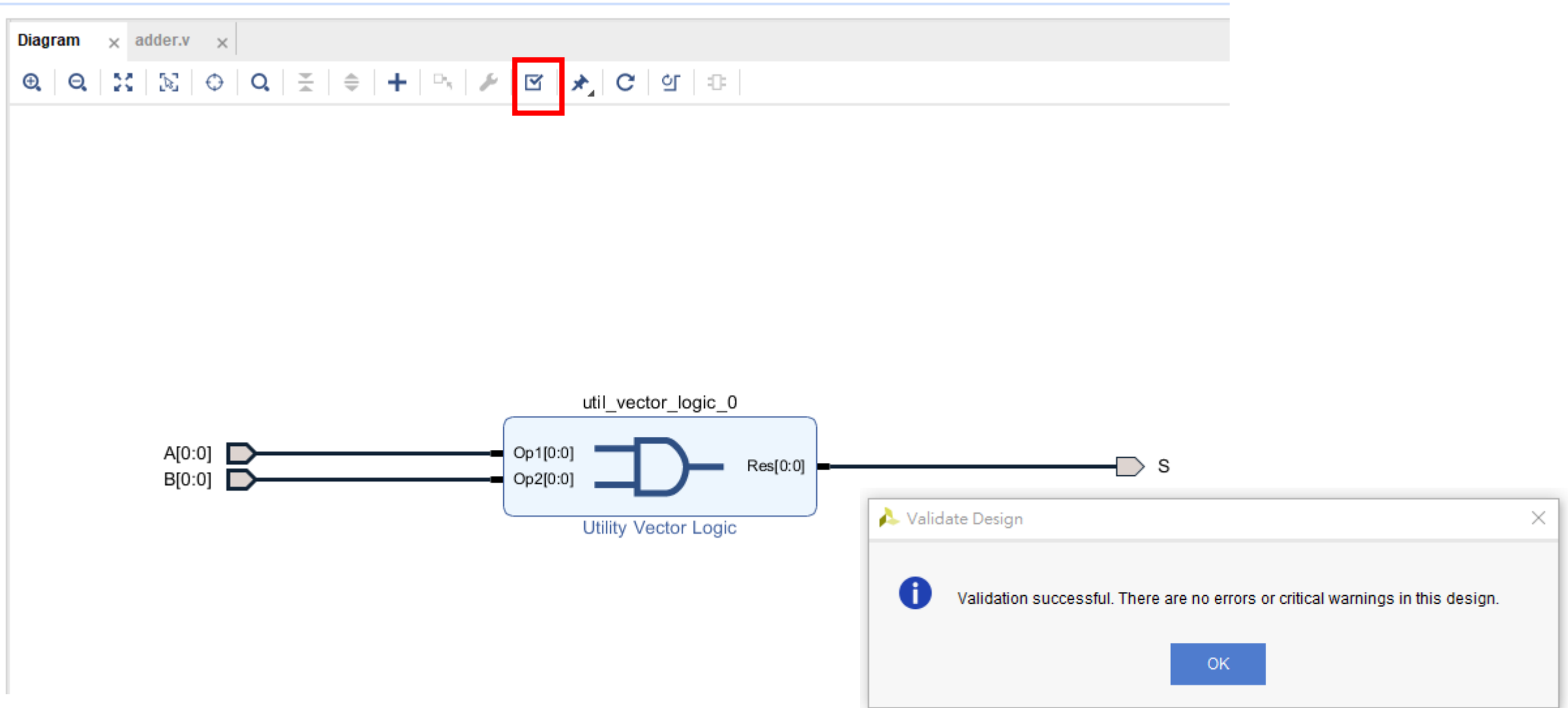
2-8 、 Block design



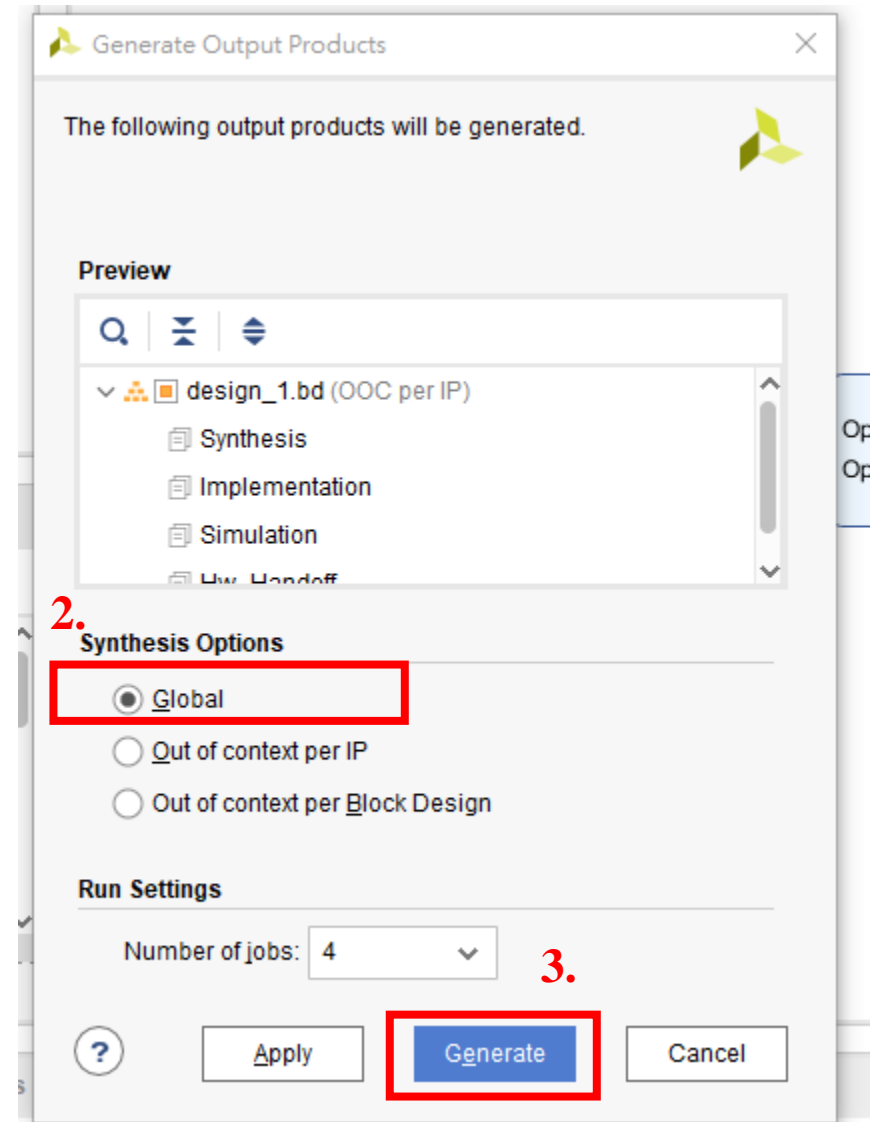
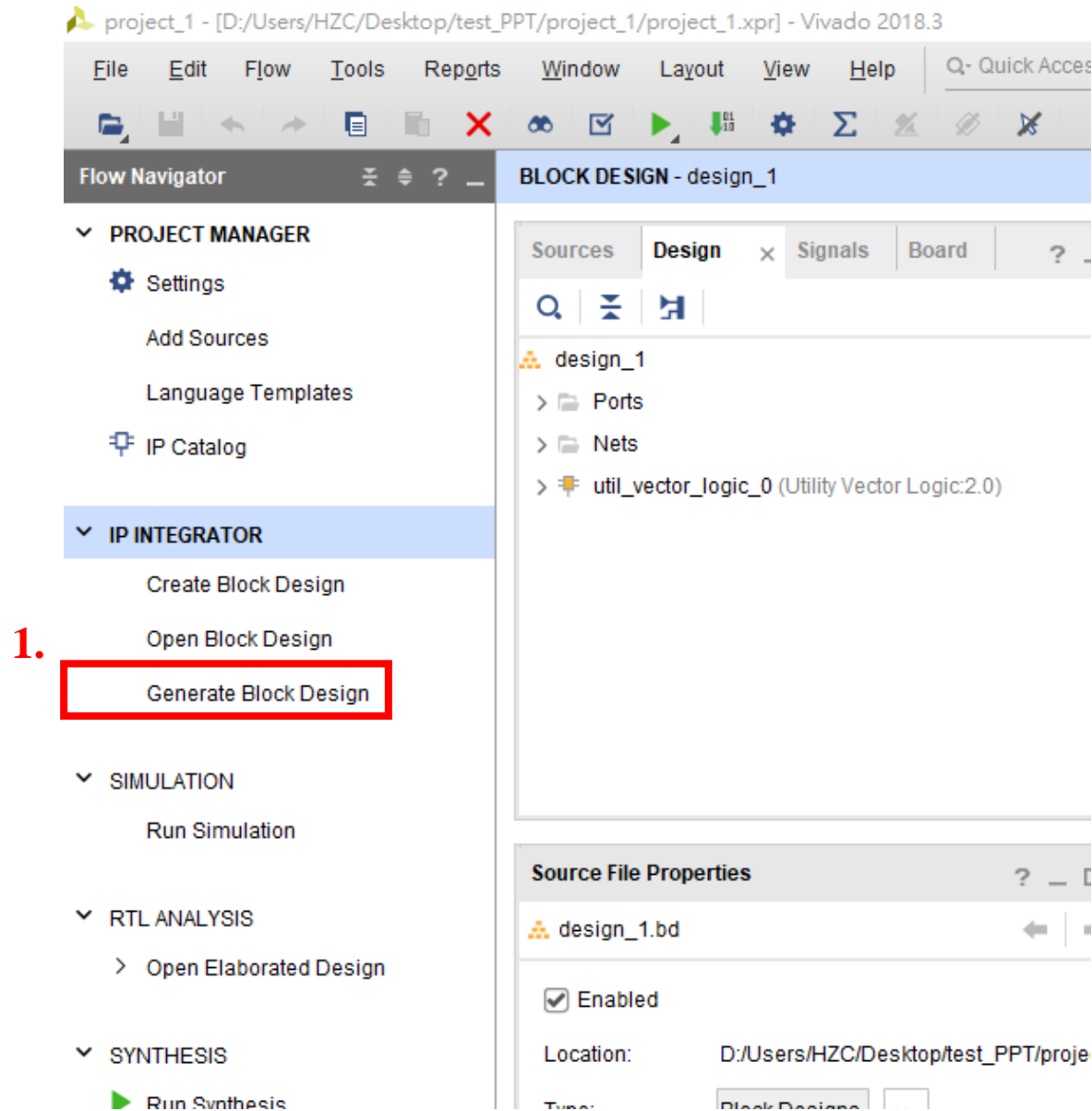
2-9 、 Block design



2-10、Block design



2-11、Block design



2-12、Block design

The screenshot displays the Xilinx Vivado IDE interface. On the left, the **Sources** window shows the project hierarchy. Under **Design Sources (1)**, the file **design_1 (design_1.v) (1)** is selected and highlighted with a red rectangle. Below this, the **Source File Properties** window for **design_1.v** is visible, showing it is **Enabled**, located at **D:/Users/HZC/Desktop/test_PPT/project_1/prc**, of type **Verilog**, in the **xil_defaultlib** library, and has a size of **1.3 KB**.

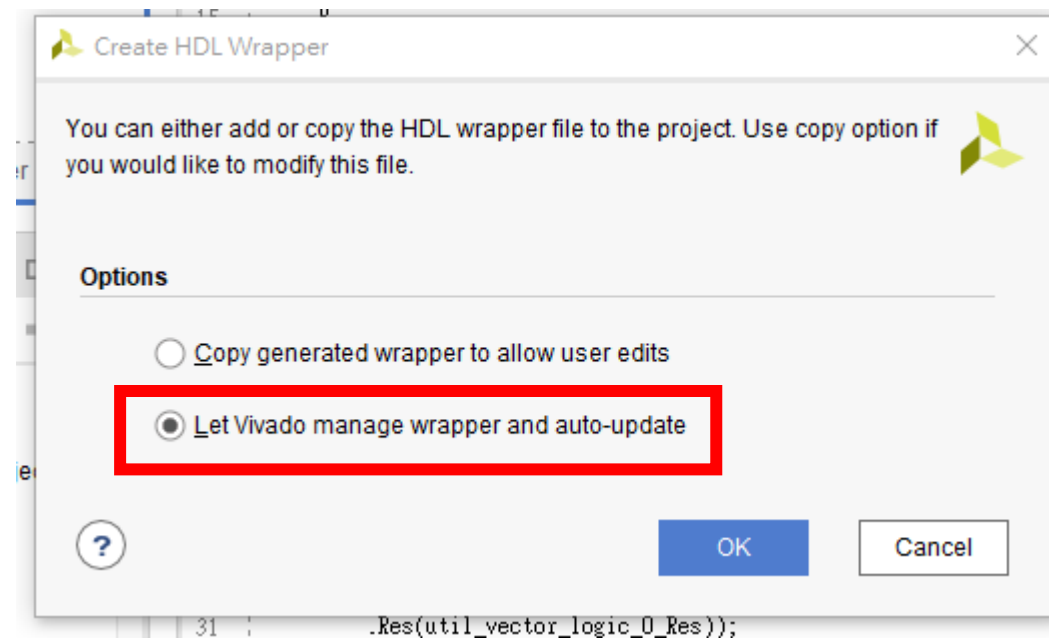
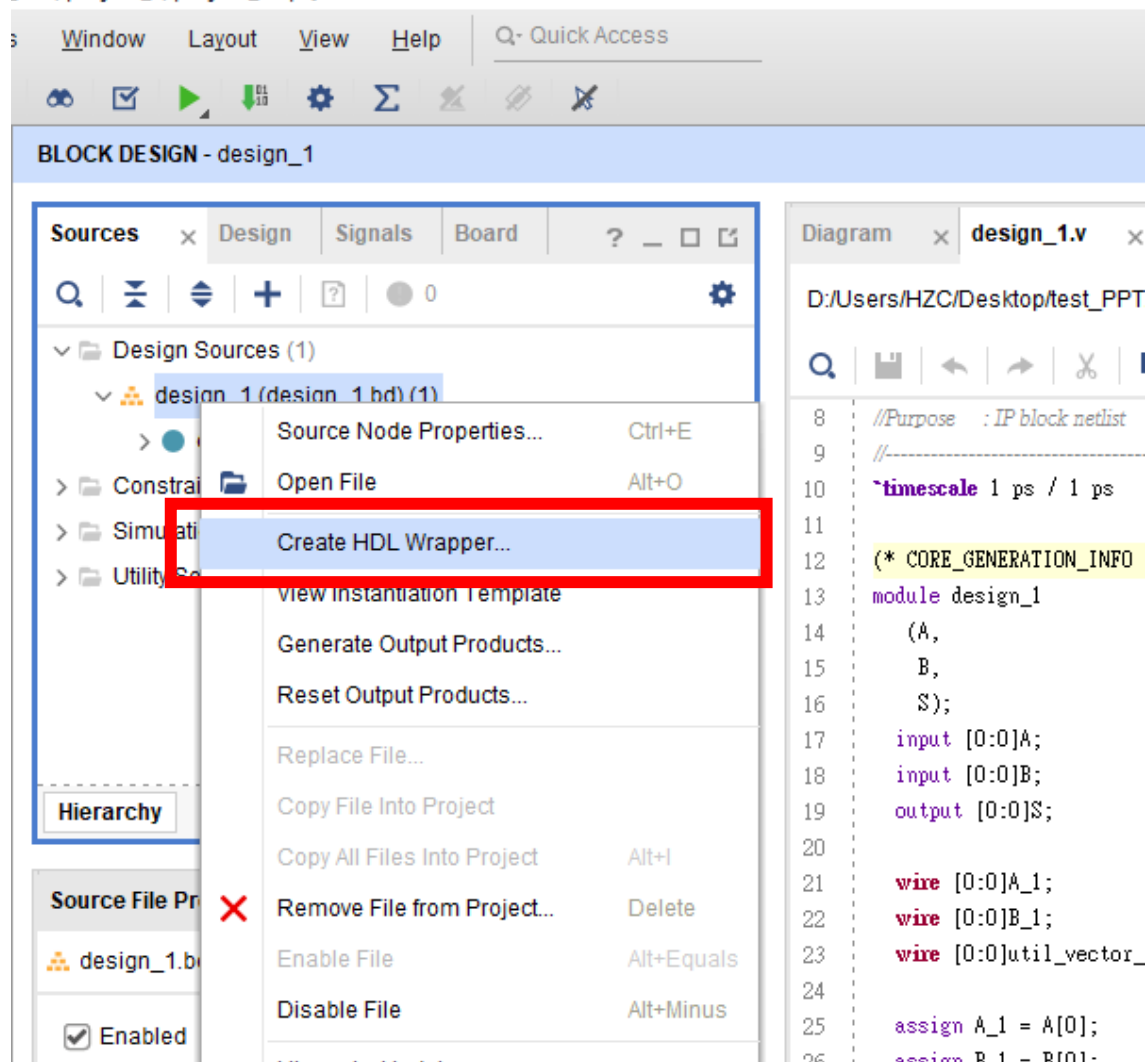
The main editor window, titled **Diagram x design_1.v**, shows the Verilog code for the **design_1** module. The code is as follows:

```
8 //Purpose : IP block netlist
9 //-----
10 `timescale 1 ps / 1 ps
11
12 (* CORE_GENERATION_INFO = "design_1,IP_Integrator,{x_ipVendor=xilinx.com,x_ipLibrary=BlockDiagram,x_ipName=design_1,x_ipVersion=1.00.a,x_ipLanguage=VERI"
13 module design_1
14     (A,
15      B,
16      S);
17     input [0:0]A;
18     input [0:0]B;
19     output [0:0]S;
20
21     wire [0:0]A_1;
22     wire [0:0]B_1;
23     wire [0:0]util_vector_logic_0_Res;
24
25     assign A_1 = A[0];
26     assign B_1 = B[0];
27     assign S[0] = util_vector_logic_0_Res;
28     design_1_util_vector_logic_0_0 util_vector_logic_0
29         (.Op1(A_1),
30          .Op2(B_1),
31          .Res(util_vector_logic_0_Res));
32 endmodule
33
```

The bottom right corner of the IDE shows the page number **21**.

2-13 、 Block design

_PPT/project_1/project_1.xpr] - Vivado 2018.3



2-14、Block design

The screenshot displays the Xilinx Block Design tool interface for a project named "design_1".

Left Panel: Sources

- Design Sources (1)
 - design_1_wrapper (design_1_wrapper.v) (1)** (highlighted with a red box)
 - design_1_i: design_1 (design_1.bd) (1)
 - design_1 (design_1.v) (1)
 - util_vector_logic_0: design_1_util_vector_logi
- Constraints
- Simulation Sources (1)
- Utility Sources

Bottom Panel: Source File Properties

design_1_wrapper.v

- ☒ Enabled
- Location: D:/Users/HZC/Desktop/test_PPT/project_1/prc
- Type: Verilog
- Library: xil_defaultlib
- Size: 0.8 KB

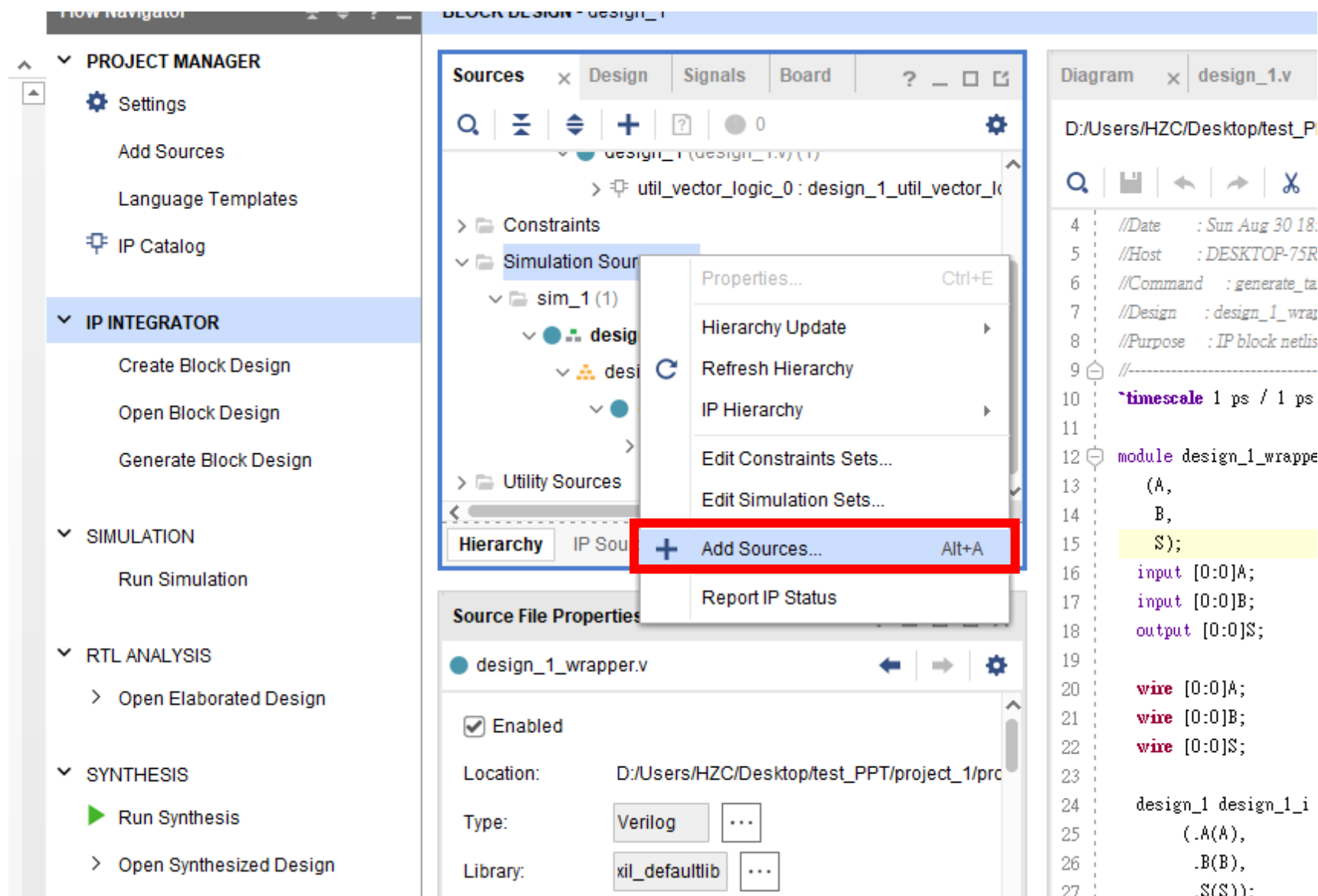
Right Panel: Diagram

design_1.v x design_1_wrapper.v x

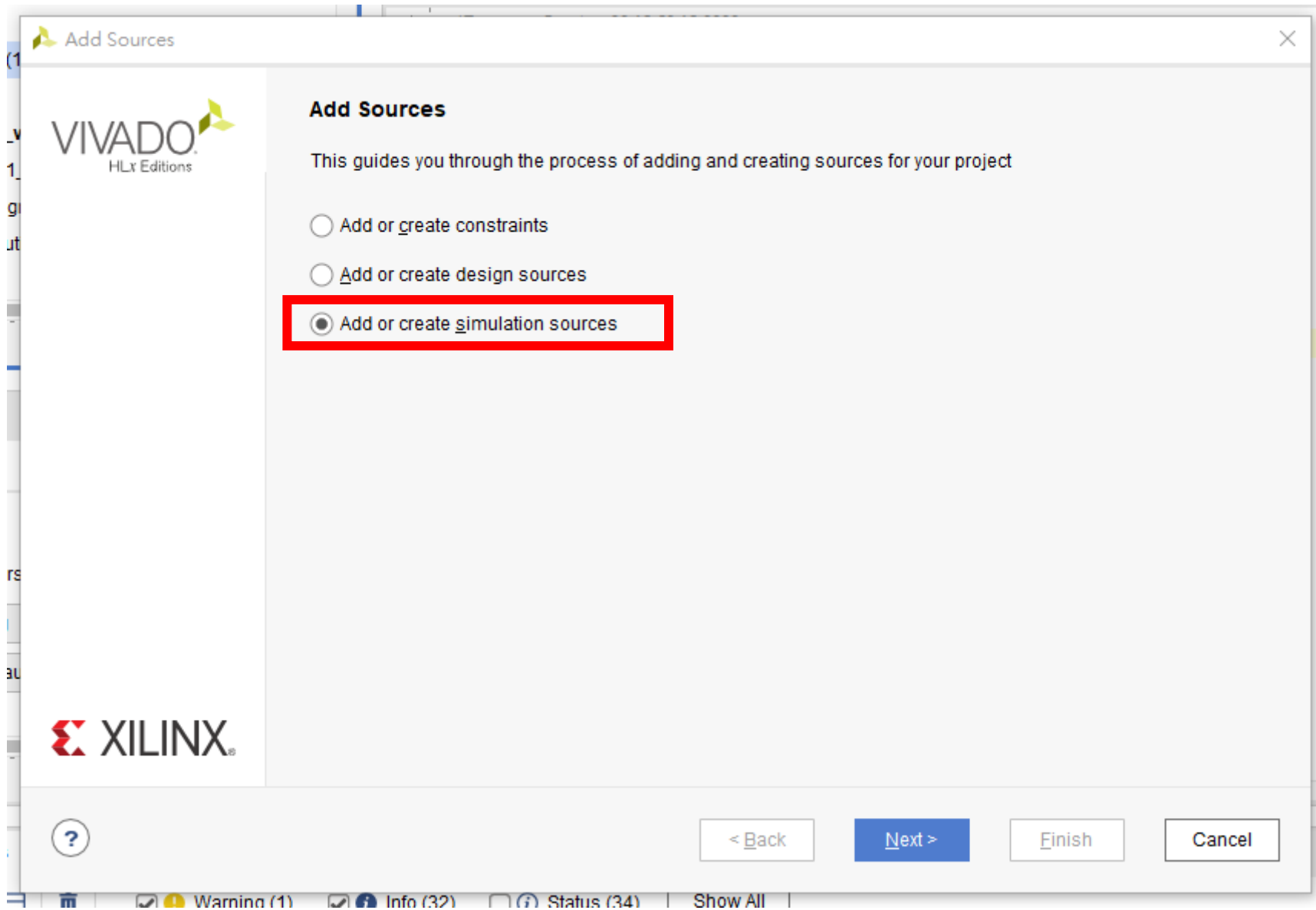
D:/Users/HZC/Desktop/test_PPT/project_1/project_1.srscs/sour

```
4 //Date : Sun Aug 30 18:52:18 2020
5 //Host : DESKTOP-75RI9S4 running 64-bit major release (b
6 //Command : generate_target design_1_wrapper.bd
7 //Design : design_1_wrapper
8 //Purpose : IP block netlist
9 //-----
10 *timescale 1 ps / 1 ps
11
12 module design_1_wrapper
13     (A,
14      B,
15      S);
16     input [0:0]A;
17     input [0:0]B;
18     output [0:0]S;
19
20     wire [0:0]A;
21     wire [0:0]B;
22     wire [0:0]S;
23
24     design_1 design_1_i
25         (.A(A),
26          .B(B),
27          .S(S));
28 endmodule
29
```

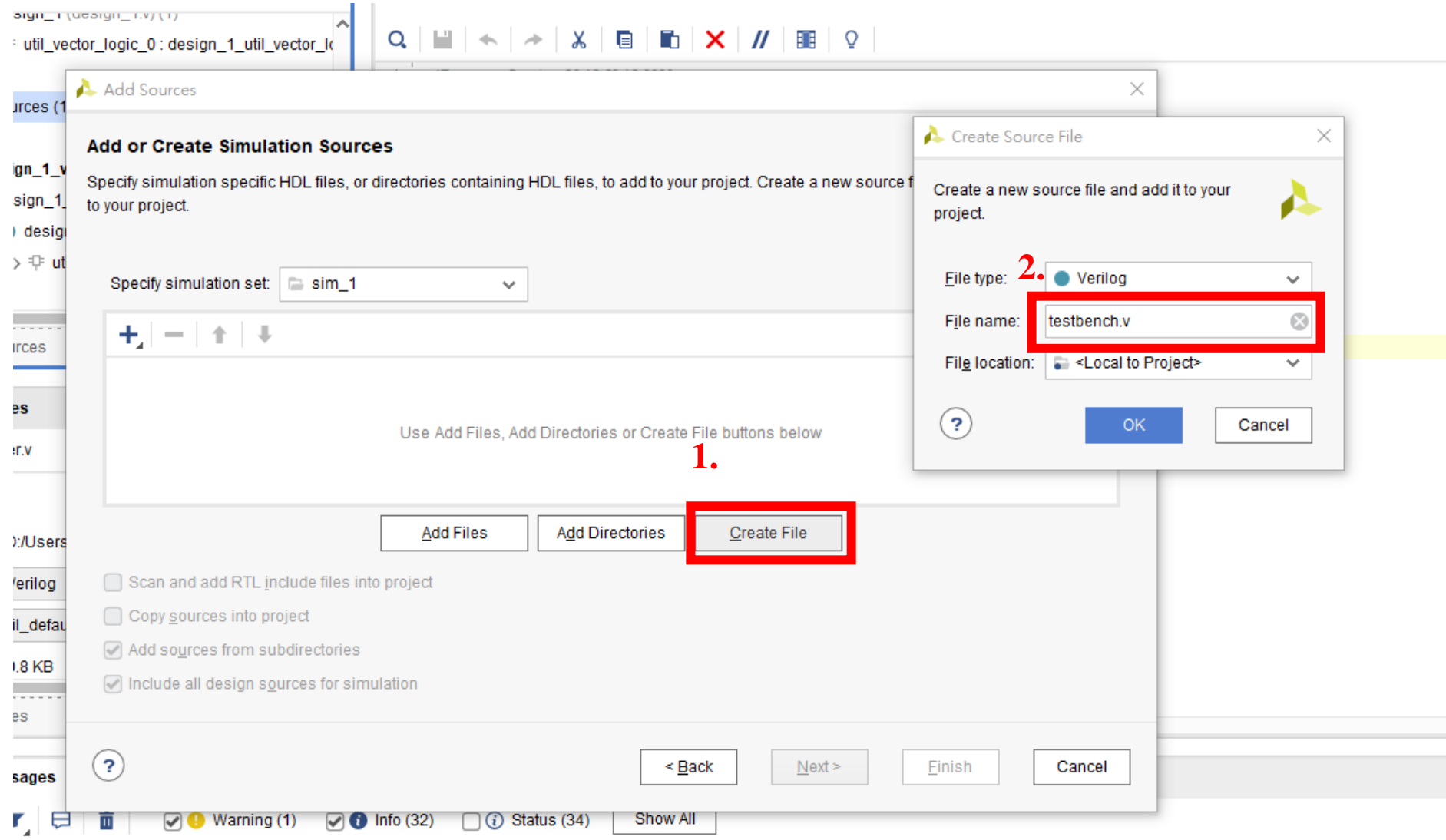
3-1、Testbench



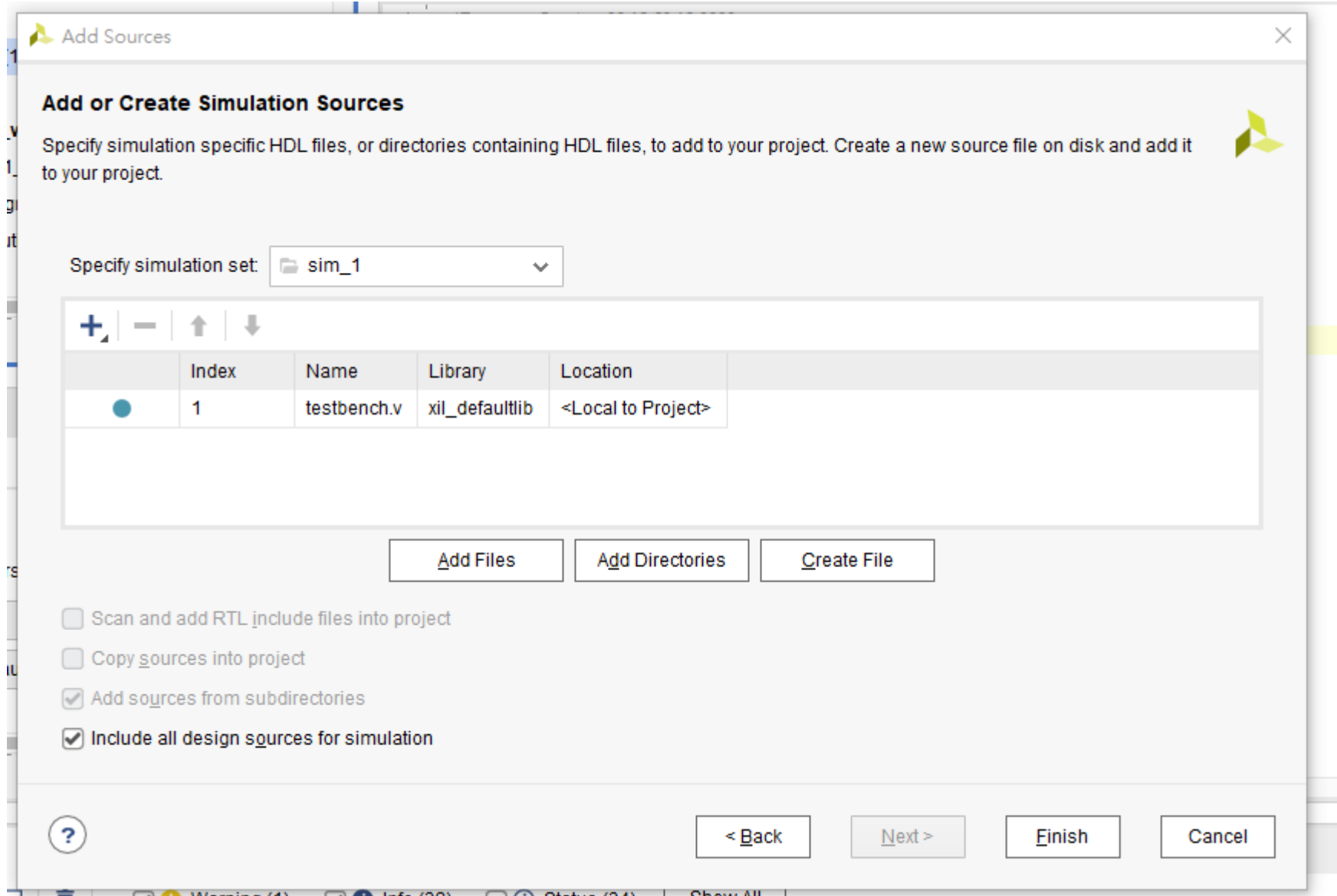
3-2、Testbench



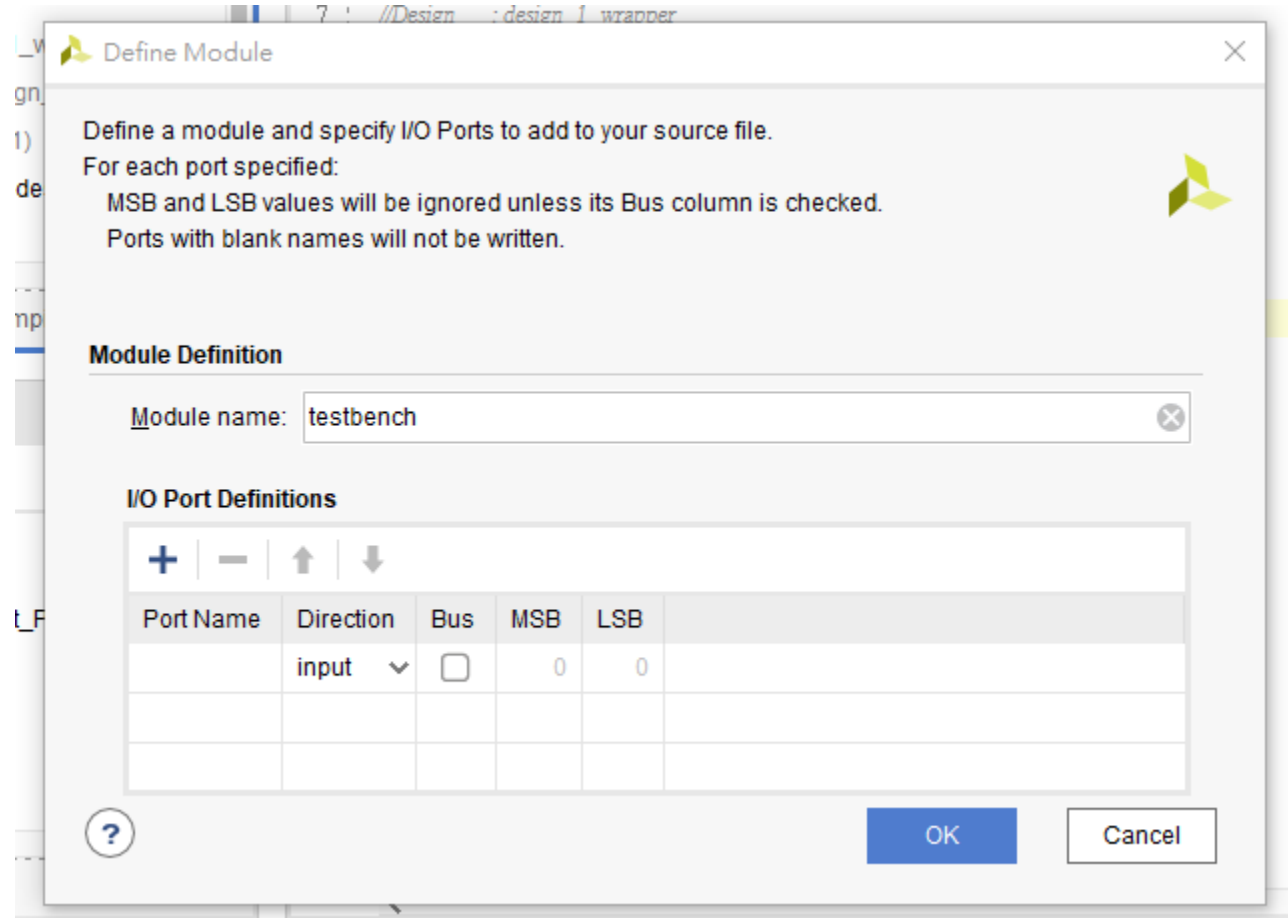
3-3、Testbench



3-4、Testbench



3-5 、 Testbench



3-6、Testbench

The screenshot displays the Xilinx Vivado IDE interface for a project named "BLOCK DESIGN - design_1".

Sources Panel: Shows the project hierarchy. Under "Simulation Sources (2)", the "sim_1 (2)" folder contains "design_1_wrapper (design_1_wrapper.v) (1)". Inside this wrapper, "design_1_i: design_1 (design_1.bd) (1)" is listed, which contains "design_1 (design_1.v) (1)". This design_1 block contains "util_vector_logic_0: design_1_util_vect". The "testbench (testbench.v)" file is also listed under "Utility Sources".

Source File Properties Panel: Shows the properties for the selected "testbench.v" file. It is "Enabled", located at "D:/Users/HZC/Desktop/test_PPT/project_1/prc", has a "Type" of "Verilog", and a "Library" of "xil_defaultlib". The size is "0.5 KB".

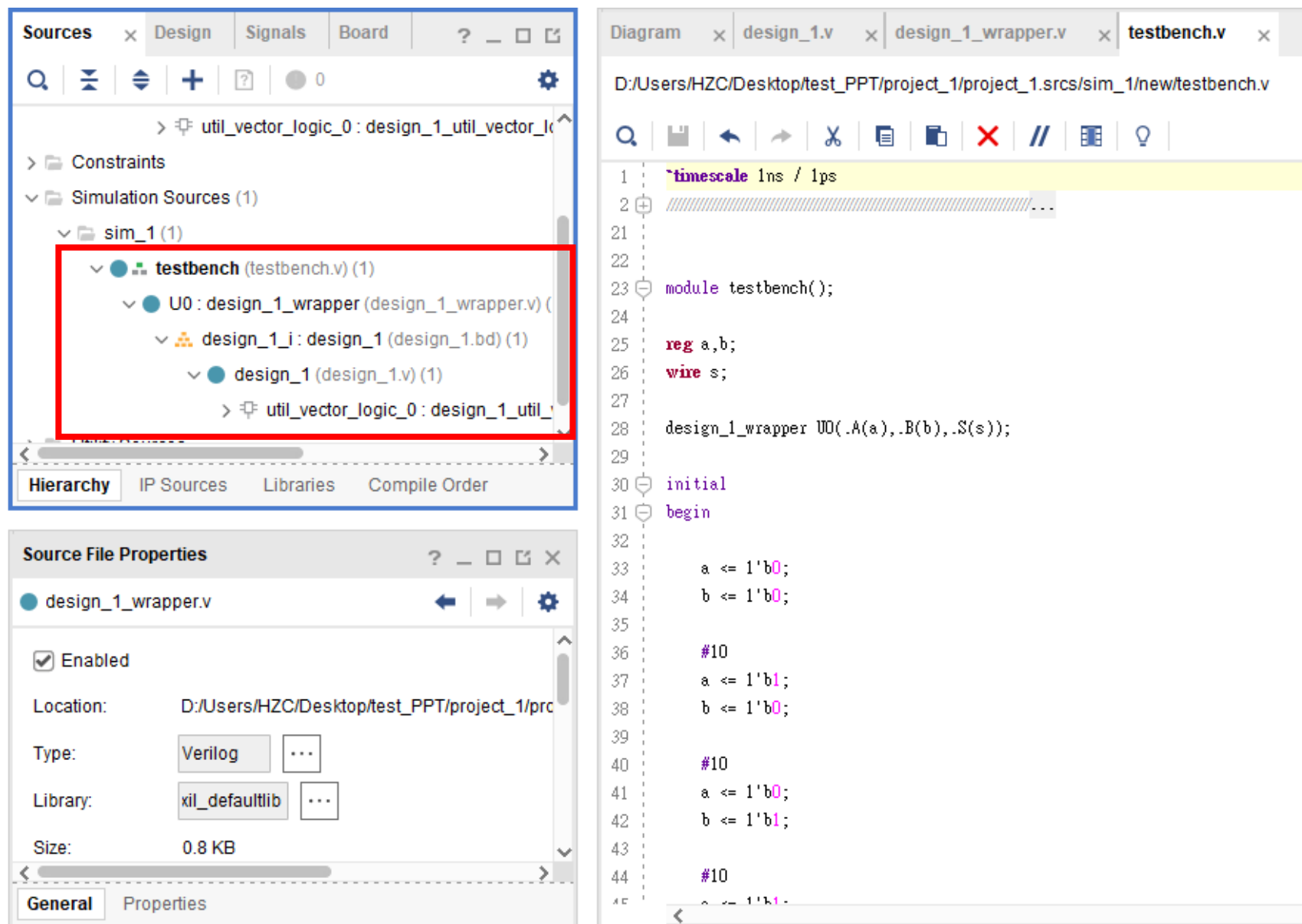
Diagram Panel: Shows the Verilog code for "testbench.v". The code includes a timescale declaration and a module definition.

```
1 *timescale 1ns / 1ps
2 //////////////////////////////////////...
21
22
23 module testbench(
24
25 );
26 endmodule
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
```

3-7、Testbench

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////...
21 module testbench();
22
23     reg a,b;
24     wire s;
25
26     design_1_wrapper U0(.A(a),.B(b),.S(s));
27
28     initial
29     begin
30
31         a <= 1'b0;
32         b <= 1'b0;
33
34         #10
35         a <= 1'b1;
36         b <= 1'b0;
37
38         #10
39         a <= 1'b0;
40         b <= 1'b1;
41
42         #10
43         a <= 1'b1;
44         b <= 1'b1;
45
46         #10
47         $finish;
48
49     end
50 endmodule
```

3-8、Testbench



The screenshot displays a Verilog IDE interface with three main panes:

- Sources Pane (Left):** Shows a project hierarchy. The 'testbench' file is highlighted with a red rectangle. The hierarchy is: `util_vector_logic_0 : design_1_util_vector_logic_0` (parent), `Constraints`, `Simulation Sources (1)`, `sim_1 (1)`, `testbench (testbench.v) (1)`, `U0 : design_1_wrapper (design_1_wrapper.v) (1)`, `design_1_i : design_1 (design_1.bd) (1)`, `design_1 (design_1.v) (1)`, and `util_vector_logic_0 : design_1_util_vector_logic_0`.
- Source File Properties Pane (Bottom Left):** Shows properties for `design_1_wrapper.v`. The file is **Enabled**. Location: `D:/Users/HZC/Desktop/test_PPT/project_1/project_1.srcs/sim_1/new/testbench.v`. Type: `Verilog`. Library: `xil_defaultlib`. Size: `0.8 KB`.
- Diagram Pane (Right):** Shows the Verilog code for `testbench.v`. The code is as follows:

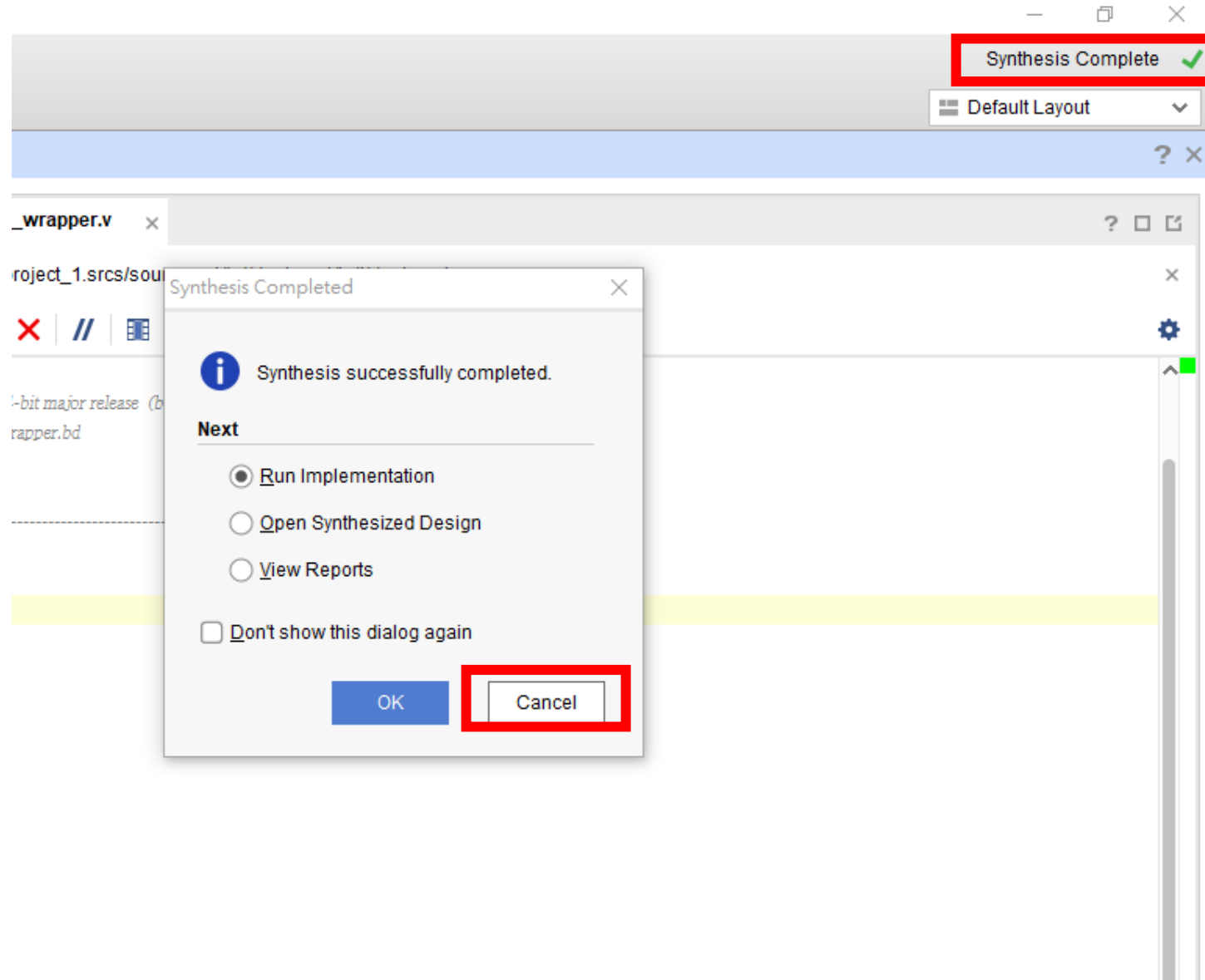
```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////
21
22
23  module testbench();
24
25      reg a,b;
26      wire s;
27
28      design_1_wrapper U0(.A(a),.B(b),.S(s));
29
30      initial
31      begin
32
33          a <= 1'b0;
34          b <= 1'b0;
35
36          #10
37          a <= 1'b1;
38          b <= 1'b0;
39
40          #10
41          a <= 1'b0;
42          b <= 1'b1;
43
44          #10
45          a <= 1'b1;
```

4-1、Synthesis

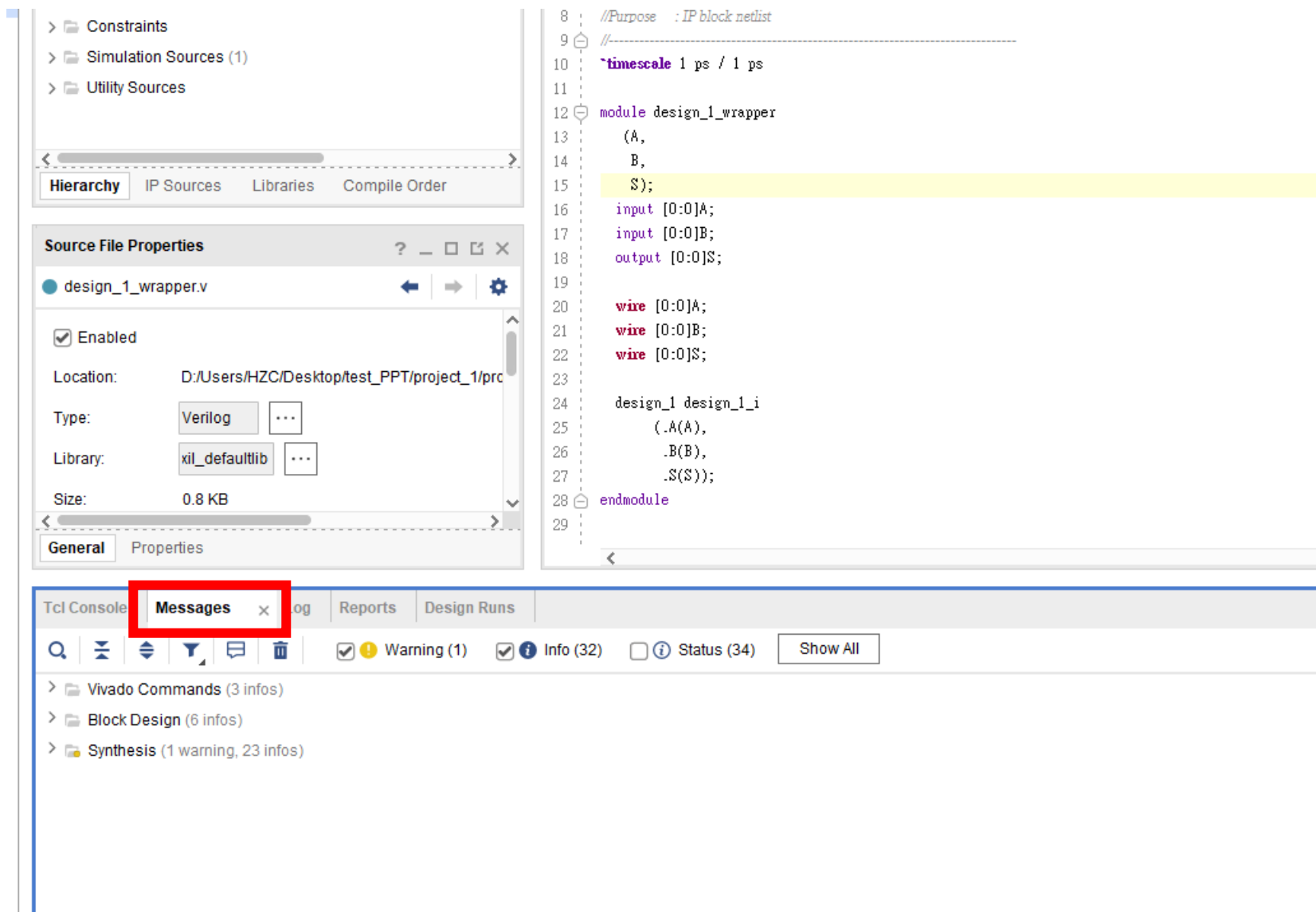
The screenshot displays the Vivado 2018.3 IDE interface. On the left, the 'PROJECT MANAGER' and 'IP INTEGRATOR' panels are visible. The 'SYNTHESIS' section is expanded, and the 'Run Synthesis' button is highlighted with a red rectangle. The main workspace shows the 'BLOCK DESIGN - design_1' hierarchy, with 'design_1_wrapper' selected. The 'Source File Properties' panel for 'design_1_wrapper.v' is open, showing it is enabled and located at 'D:/Users/HZC/Desktop/test_PPT/project_1/project_1.xpr'. The 'Launch Runs' dialog is open, showing the 'Launch directory' as '<Default Launch Directory>'. The 'Options' section has 'Launch runs on local host' selected, and the 'Number of jobs' is set to 4. The 'OK' button is highlighted. The background code editor shows Verilog code for a module named 'design_1'.

```
module
13 (A,
14 B,
15 S);
16 input [0:0]A;
17 input [0:0]B;
18 output [0:0]S;
19
20 wire [0:0]A;
21 wire [0:0]B;
22 wire [0:0]S;
23
24 design_1 design_1_i
25 (.A(A),
26 .B(B),
27 .S(S));
28 endmodule
29
```

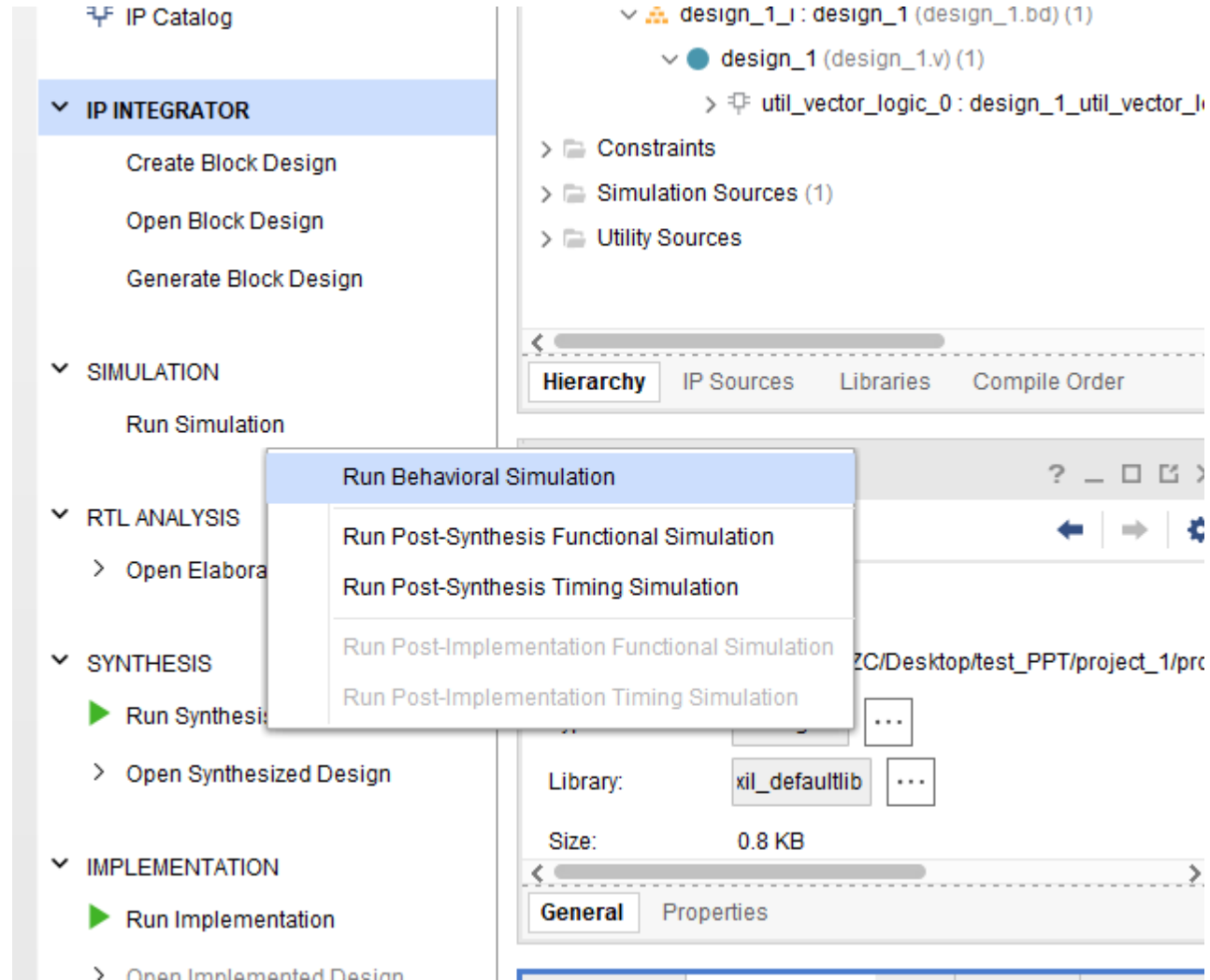

4-2、Synthesis



4-3 、 Synthesis



5-1 、 Simulation



5-2 、 Simulation

low Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION**
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream

SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench

Scope

Name	Design U...	Block Type
tes...	testbench	Verilog M...
> ...	design_...	Verilog M...
gbl	gbl	Verilog M...

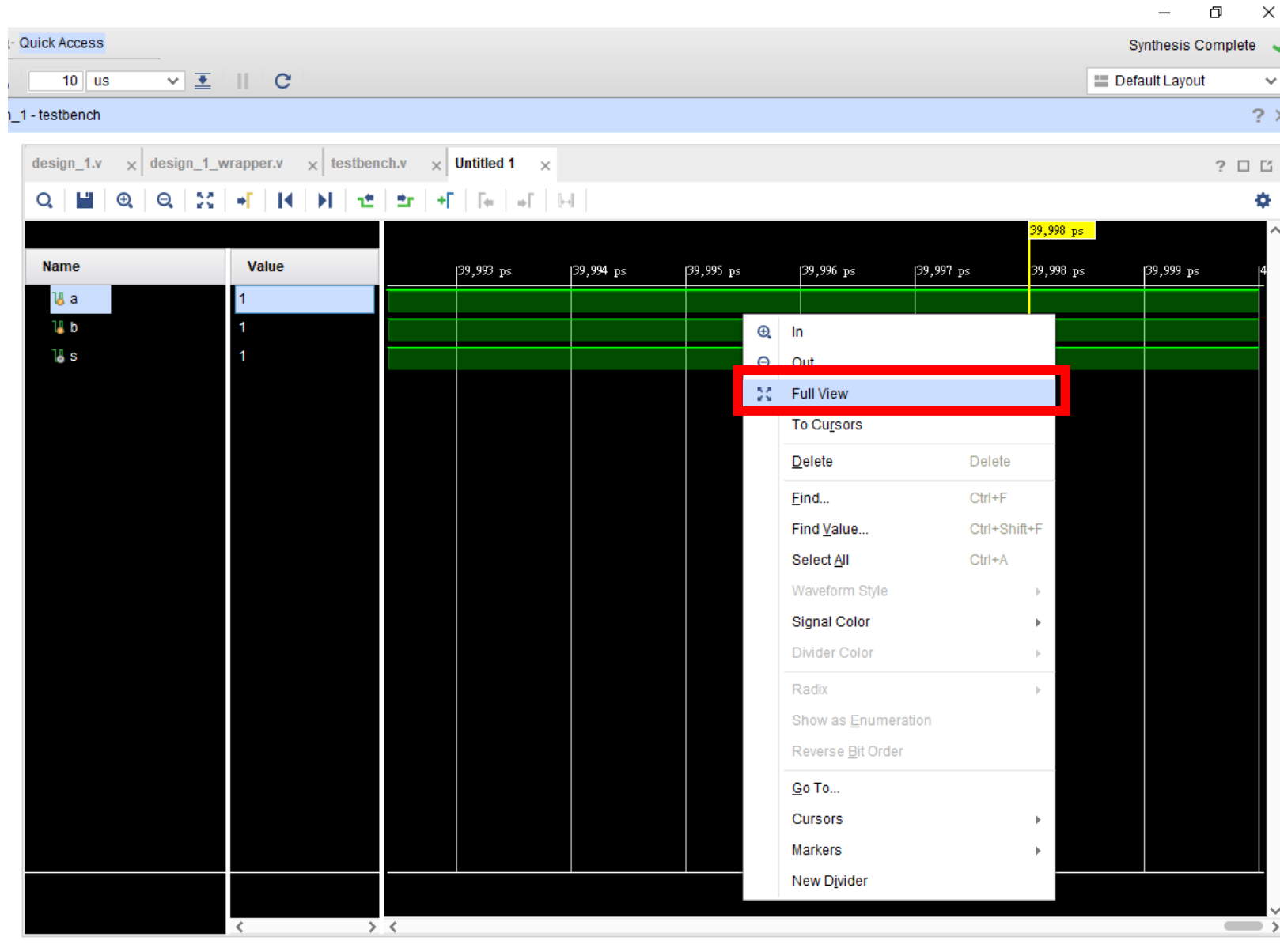
Objects

Name	Value	Data Type
a	1	Logic
b	1	Logic
s	1	Logic

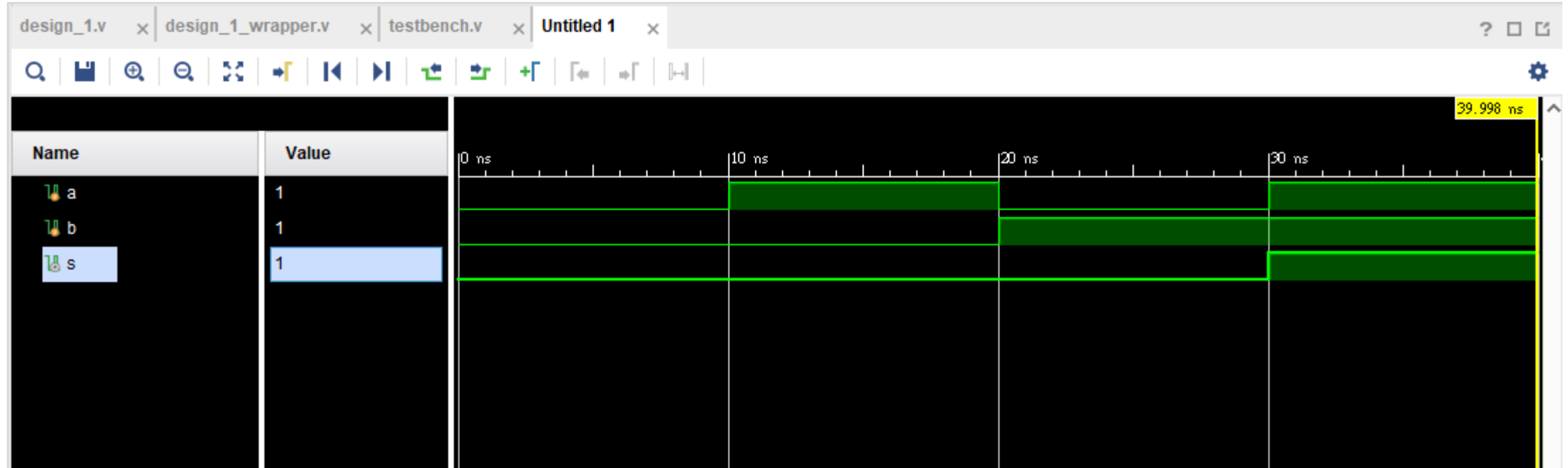
testbench.v

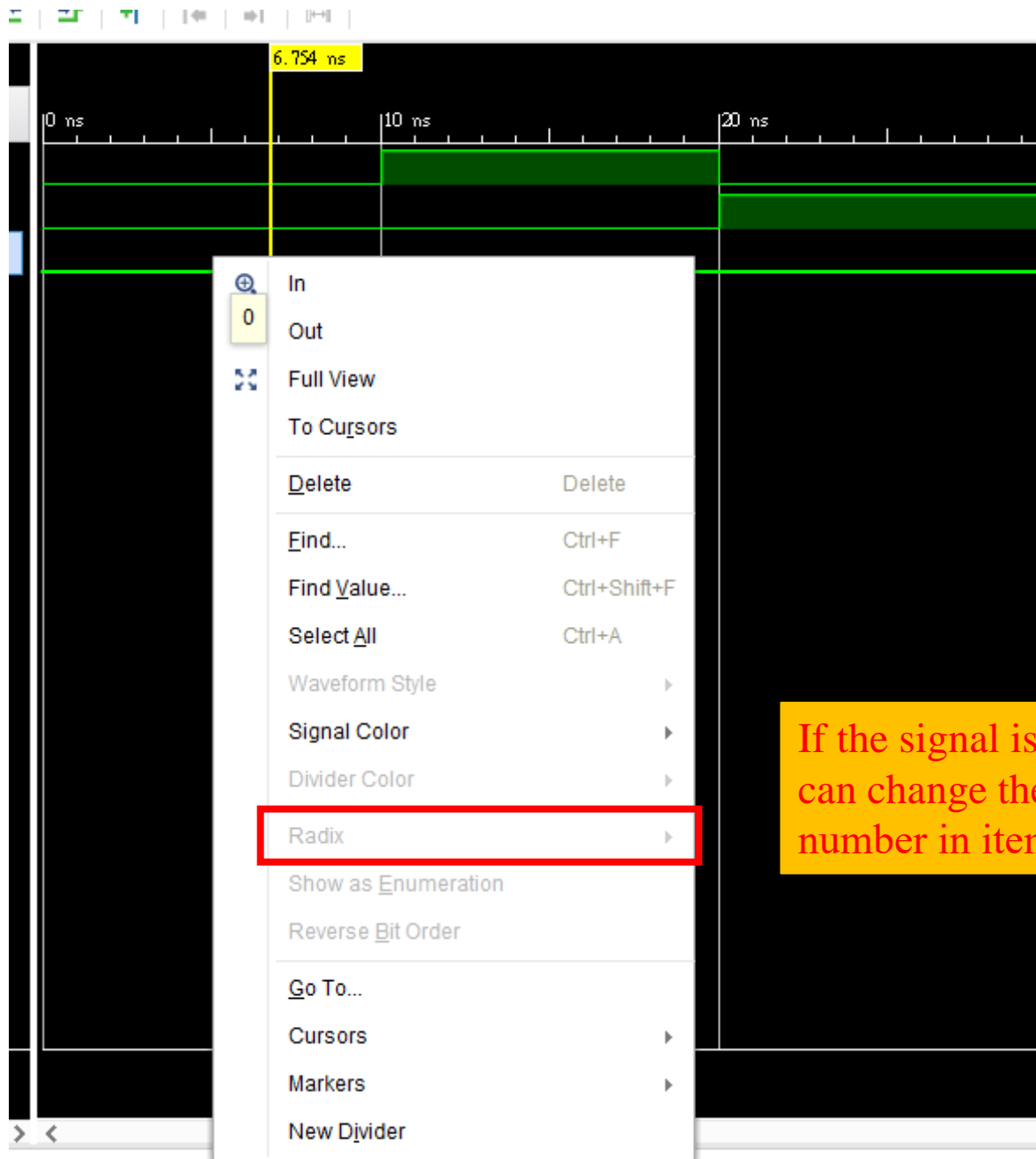
```
21 module testbench();
22
23     reg a,b;
24     wire s;
25
26     design_1_wrapper U0(.A(a),.B(b),.S(s));
27
28     initial
29     begin
30
31         a <= 1'b0;
32         b <= 1'b0;
33
34         #10
35         a <= 1'b1;
36         b <= 1'b0;
37
38         #10
39         a <= 1'b0;
40         b <= 1'b1;
41
42         #10
43         a <= 1'b1;
44         b <= 1'b1;
45
46         #10
47         $finish;
48
49     end
```

5-3 、 Simulation



5-4 、 Simulation





If the signal is a vector, you can change the displayed number in item “Radix”.