Operating System HW3 Blo3040009 \$1\frac{2}{2}\$

1. Memory - mapped IID: Put the IID registers in the regular memory space so that they can be accessed just as any other memory locations.

2. Most I/O require the transfer of bytes between the I/O device and consecutive memory locations over and over again. DMA allows this transfer to be done by a special clip, therefore let the CPU do other tasks.

3. (a) FCFS:	Pı	P	P3 P4	P5				
	8	1	2 1	Ь				
/~~·	_							
\$JF :	P2 P4 P3	P5		Pı				
	1 1 2	6		8				
Non-preemptive priority P2 P5 P3 P1 P4								
priority	Ps Ps	Рз		Pı P4				
' 0	<b>І</b> ь	a		8 1				

RR: P1 P2 P3 P4 P5 P1 P3 P5 P1 P5 P1

(b) Turnaround time	Pı	Pz	P3	P4	P5	
FCFS	8	9	11	12	18	
	18		+	a	Jο	
non-preemptive priority	1)	1	9	18	)	
T RR	18	l	η	4	16	

(c)	Waiting time	Pı	Pz	P3	P4	Ps	Avg
	FCFS	0	8	9	1	اع	8
	SJF	JO	0	2	J	4	17/5
	non-preemptive	9	0	)	١)		34/5
	T RR	) 0		5	3	10	29/5

## (d) SJF scheduling

4. I feel like "subvontine" is the apt term to use here rather than "corontine", which is a more general term to use.

Every time the user part invokes the kernel part, the kernel will start out in the same place.

This behavior is similar to a procedure (subroutine).