



PRINTSHOP: SERIAL PRINTER ENVIRONMENTS AND SECURITY

Research Proposal

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ABSTRACT

Securing supply chains for critical infrastructure and any production environment is a growing concern. Third-parties or nation state level attackers have been shown to target employees or infrastructure indirectly to gain access to their target's network. One of the devices being examined to aid this research is the SNBC BTP-S80, a USB/serial connected thermal printer. These devices are made with foreign software and hardware, and they are used off the shelf without any security review. In some instances, the devices implement an MPU/MCU and an FPGA for I/O processing, which creates a potential gap for data to be modified. The proposed research aims to assess these devices for any risks and demonstrate that they could be used as a part of supply chain attacks.

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Introduction

1.1 Background

Serial printers are devices commonly used for instant reporting of system data for industrial control systems (ICS) and receipts for point-of-sale (POS) systems. These devices are connected to their host using Wi-Fi, bluetooth, ethernet, or USB; in some cases, serial RS232 is an option as well. The goal of this research is to assess what software and hardware protections are enabled, as well as, how configurable the serial printers are for further exploit research.



Figure 1.1: Comparison of common POS systems

Figure 1.1 shows us two similar looking point-of-sale systems. However, the operating system and required hardware used by both is different. Typically, unless you have the Square provided terminal, their software/client is installed onto an Android or iOS device and connected to a Square compatible card reader [1]. Whereas, the SurePoS, NCR, or other common EFTPoS system will run a proprietary OS based on Windows or Linux [2]. Furthermore, these PoS require some form of printing receipts as record keeping for the business owner and customer. And these devices also vary in terms of processing capabilities and operating system.

For instance, a common thermal printer seen with PoS systems, integrated with fuel pumps, or other industrial control equipment, is the SNBC BTP-S80 thermal printer [3], [4]. There are multiple versions of the device with support for Bluetooth, USB only, or combination of USB/Serial/Ethernet. The bluetooth hardware is provided over an accessory 25-pin serial connection, with more I/O as a serial connection via RS232C connector and USB Type-B. It has driver support for various platforms: Android, iOS, Windows, Linux, and MacOS. The most interesting aspects are the processor, an Arm Cortex M4 clocked at 3.54MHz, and the operating system, a proprietary version of FreeRTOS. The system architecture is Armv7E-M with JTAG/SWD hardware debugging support [5], [6].

By default, the printer has enough headroom to process ESC/POS commands for printing paper and a webserver for debugging or general diagnostics. In theory, the uncompromised device could be flashed with modified firmware to act as a decoy and human-input-device (HID) against the host PoS. The viability of any vulnerabilities would likely be dependent upon supply chain attacks or physical bait-and-switch tactics [7].

1.2 Significance

According to the Federal Trade Commission (FTC), there were 37,932 reports of credit card fraud in 2012 and 87,451 reports in 2022 [8], [9]. This marks an increase of credit card payment fraud by an estimated, 30.5%. By comparison, since 2020, there has been a 14.6% increase in credit card related fraud. Which does not include the millions of other fraud reports the FTC receives every year. In 2022 alone, there were around 5.1 million fraud, identity theft, and miscellaneous reports in total [8], [9]. The statistics for these reports stresses how crucial the security of payment systems are, both physical and online. And, the need to secure them grows every year.

Spyduino is [10] a working example of a programmable BadUSB device using an Arduino to mimic a Human Interface Device (HID). Arduinos are typically more accessible

and easily developed compared to an embedded device whose design is more single purpose [11], [12]. Especially if the goal is to not modify hardware or require hands-on access for exploitation. However, the research shows us that it is possible create HID clones from scratch if the hardware is compatible.

The Arduino used in their research is powered by an ATmega328P microcontroller with 32KB flash memory, 2KB SRAM, and 1KB EEPROM. Compared to the most likely target device of our proposed research, the SNBC BTP-S80, it features an ARM Cortex M4 microcontroller with 512KB flash memory, 96KB SRAM, 4KB of EEPROM. This is relevant to the proposed research, because it shows that a device with similar hardware specifications was feasible; meaning, it is likely that our own research will be successful. BadUSBs are a known and tested area of research. The novelty of this proposal comes from the assessment of the printer devices and showing whether one could be used maliciously within their environments (e.g., PoS systems, or ICS).

1.3 Research Goals and Objectives

This research primarily focuses on physical POS systems or terminals and their hardware (serial accessories), rather than online solutions. For instance, not mobile payment apps like Venmo, CashApp, Zelle, or Paypal [13] since their environments typically do not use serial print devices. It is also likely that more research would be needed for emulating touch inputs for mobile environments versus the traditional keyboard attacks that will be implemented. Presumably, the host-to-guest communication will not differ greatly between other environments (e.g., ICS). If the printers have demonstrable weaknesses with an Ubuntu host, that will fulfill the testing requirements.

The goal of this research is to further establish academic works in regards to embedded printer devices testing and security. This area is loosely documented within academia and only mentioned vaguely in relation to statistical reports or applied research using

entirely different environments. For instance, most researchers limit their analysis of the environment to smartphones and the corresponding payment app, or detection systems for card skimmers [7].

Through this research we hope to identify supply chain risks using side channel attacks from auxiliary devices. Some examples of how the research could be applied in the future vary: BadUSB/BashBunny [14], JuiceShop [15], DVWA [16], or Webgoat [17]. Works within the PoS system context or embedded systems discussing supply chain attacks through third-party hardware are limited.

1.4 Research Questions

The research questions that this proposal seeks to answer are as follows:

- Q1: Can the hardware be reflashed with a modified firmware image (e.g., FreeRTOS, ReconOS, VxWorks)? Testing a version of the original firmware with additional libraries, or an alternative OS, allows us to see if supply chain attacks are a concern. Either by the manufacturer, supplier, or other party. Reflashing is not novel by itself, however, the device might have protections in place to prevent it.
- Q2: Does the hardware and firmware have enough resources to support HID functionality on-top of printing? In other words, can we maintain operation of standard printer command interpretation and side-channel input attacks without causing crashes or delays? The viability of the attack depends on it going unnoticed by operators or technicians.

Each of these goals will be approached individually as prescribed by the methodology.

Related Works

2.1 RTOS: Software and Security

[18] introduces several embedded kernels and discusses their differences in regard to developing a secure mass storage device. For this research, we are primarily interested in RTOS-like kernels because of existing support for a sample device like the SNBC BTP-S80 printer. However, the paper criticizes such operating systems because their "real-time driven design is barely compatible with the overhead produced by security mechanisms." For many applications, there is a trade off with RTOS where performance is the main criteria and security is not a priority. [19] introduces several common RTOS and discusses their security issues. Notably, most RTOS are susceptible to code injection, cryptography inefficiency, unprotected shared memory, priority inversion, denial of service attacks, privilege escalation, and inter-process communication vulnerabilities. Depending on the MPU (microprocessor unit), the vendor has hardware protections like Intel SGX or Arm Trust Zone. These are all areas that can be used for pivoting onto the device, especially shared memory and privilege escalation. If the target device firmware is outdated (or, even libraries used by the firmware) and there are known CVEs that can be repeatedly exploited, persistence mechanisms are not a requirement to gain routine access.

2.2 PoS Attack Patterns

Typically, when discussing attack patterns for PoS systems they are limited to card skimming, fake payment processor requests, or EMV cloning. In rarer cases, they might deliver malware to perform memory scraping within the PoS system or attempt swapping hardware while employees are distracted. None of these attacks include thermal printers at any point during their attack chain or delivery.

Easily the most common and well known type of attack is card skimming. Attackers will place these devices directly on top of the existing equipment to skim, or gather, credit card information at the time of purchases. They can be incredibly difficult to identify because of the sleek and stealthy designs that fraudsters use. But there is plenty of research being presented on how to quickly detect these devices [7], [20].

Without going into too much technical detail, card skimming attacks are accomplished by reading the signals emitted when swiping a magnetic card or by using an NFC reader in proximity to the payment terminal. When the customer goes to pay and uses their card, the nearby skimmer will record the transaction data being transferred. NFC skimmers, however, are not limited to being used near the terminals. Skimmer capabilities vary, and in some cases they have cameras as well or keypads for capturing PIN and zip code data.

In response to the susceptibility of magnetic cards, EMV cards were created. They are able to avoid the issues that magnetic cards and NFC share by using a chip to securely exchange transaction data with the payment terminal using secret authentication codes. The idea is that these codes cannot be tampered with or easily cloned. Despite these security advancements, EMV cards are susceptible to pre-play attacks targeting the "unpredictable number" (UN) algorithm used by ATMs [21].

Social engineers use payment processor mobile applications to directly target their victims instead of using elaborate and technical attacks against servers or user equipment [22]. The attackers simply send payment requests disguised as payments using their preferred platform. Unwittingly, the victim will accept the request thinking they were receiving money instead.

In some cases, the fraudster sends the victim money but requests a refund shortly after. As a result, the victim is either charged fees for processing the transactions or they have already spent the refunded money. These attacks are much simpler in-terms of delivery compared to the others and the intended outcomes are different. There are instances where the user device is compromised by malware specifically for exfiltrating

banking data or similar PCI, but further discourse is outside the scope of the proposed research [23].

Researchers at Stony Brook University [24], demonstrated a successful introspection-based memory scraping attack against nine commercial PoS applications. Within their environment, it is assumed that the given VM (i.e., Dom0) within the shared virtualization platform (i.e., Xen) is compromised and it has escaped the guest environment. Because the privileges associated with the first VM, it has read access to the others and can perform out-of-VM memory scraping. This exact attack is likely limited to the platform used for the experiment, Xen Hypervisor; attempting something similarly against VMWare, Virtualbox, or QEMU would require further experimentation due to architectural differences. Also, PCI-DSS and PA-DSS requirements were not an obstacle for this attack since the data is not stored to disk and it is read from memory instead.

2.3 BadUSB-like Devices

BadUSB is a well-known and documented attack vector. One of the most popular hacker tools is built-on the concept [14]. However, there are some limitations:

- Precision of attacks is limited since scripts or effects are typically deployed blind. There is no knowledge of the user environment nor ability to interact with functional user interface mechanisms (e.g., a mouse clicking a button).
- Limited to the USB 2.0 standard. Meaning, no support for video adapters like HDMI, DisplayPort, or PowerDelivery like with USB 3.0.
- There are existing methods for limiting USB access from the host, such as GoodUSB [25].

GoodUSB supports the Linux USB stack, so another solution would be required for Windows systems or RTOS. This all depends on the environment of the connected host,

the PoS system. It is entirely possible that the PoS could have software like CrowdStrike Falcon deployed, which would monitor system behavior and mass storage device access [26]. Although the experiment environment will not use such software, it is an important distinction to make.

In [27], they describe several attacks at each of the applicable layers to USB attacks: the human, application, transport, and physical layers. These attacks would typically require some human element for deployment, but that is not the focus of the research (e.g., social engineering versus hardware hacking). Whereas the physical layer could allow signal eavesdropping or injection. This could enable a modified printer to overvolt the host (USBKiller [28]) to cause physical damage or perform other side-channel attacks [29]. Either of those methods would require investigating the device hardware to determine what level of control the bootloader or operating system has over power delivery.

2.4 Summary

As demonstrated by the previous works, vulnerability assessment of an embedded device is a well documented process. However, the extent that a serial thermal printer (e.g., Figure 1.1) can be maliciously expanded through a modified FreeRTOS image, while supporting original functionality, has not. And, given success in the assessment, it could suggest room for continual and improved research.

Proposed Research

3.1 Methodology

For this research, the quantitative approach and case study research will be used [30], [31] to create a design artifact. The goal being to gather and examine, point-in-time, data from a serial printer device as a common sample representative of the affected population. By using quantitative survey research, it is possible to evaluate potential vulnerabilities for the attacks hypothesized, as well as, prototype a modified firmware image to use them against the host environment. Each step of the process is described as follows:

- I. **Problem Identification:** A research gap exists when identifying the risks that off-the-shelf hardware exposes to host environments (i.e., PoS systems, HMI, ICS). Auxiliary devices, like serial printers, are black box pieces of equipment with questionable supply chain and development life cycles.
- II. **Objectives and Solutions:** This research aims to thoroughly examine such a device and demonstrate that it can be used as a part of a hypothetical supply chain attack. Using the information gathered, a modified firmware image with HID cloning will be created. This solution should prove that such an attack is a viable method and there are existing issues with sourcing third-party hardware.
- III. **Research Design:** The research design process begins by tearing down the target device and identifying components. That information is then used to recover the firmware for analysis, as well as, analyze the network and USB communications with a host. After reviewing, a modified firmware image will be created and then flashed to the device. All information is documented and collected. Refer to Section 4.1 for further detail about the exact process.

- IV. **Demonstration:** Using the artifact, the researcher will demonstrate that scripted HID attacks against the host are possible. Should the host filter devices using restricted vendor IDs, this attack will still work irregardless of the host operating system. It is also important that original functionality is maintained with the modified firmware.
- V. **Evaluation:** Whether or not the research has been successful depends on several factors: firmware recovery, firmware modification (using recovered firmware or third-party), attack development, and sustaining the original ESC/POS print functions. Assuming each step has been completed, the final demonstration should be able to show working print operations and scripted attacks against the host. These attacks should also work irrespective of target environment.
- VI. **Communication:** The research will present the identified gaps and issues to the embedded security field. By demonstrating the research and artifacts, the researchers hope to greater increase the scrutiny for auxiliary, third-party hardware and the associated risks. In addition, the artifacts could potentially be used for future research into embedded security and exploit development.

Research Plan

4.1 Design Process

The design process is divided into two parts, information collection and exploitation. Beginning with teardown of the equipment, identification of components, and then analysis of the firmware, networking, and lastly, the USB communications between the host and device. Using the information gathered within the first stage, modifications will be made to the firmware installed on the serial printer. Each step of the process shown in Figure 4.1, is described as follows:

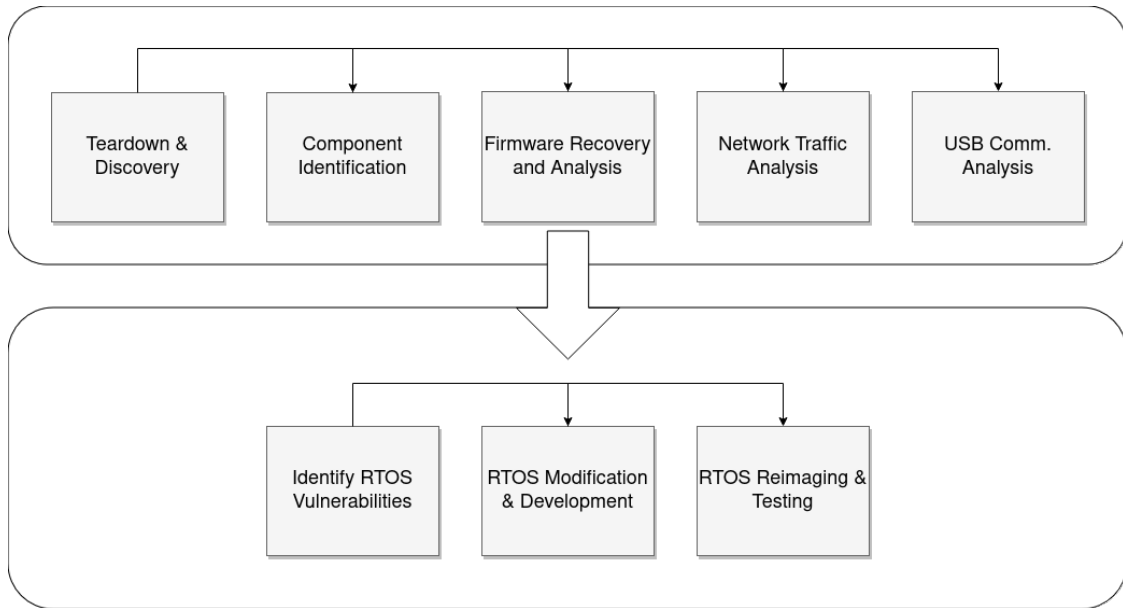


Figure 4.1: Design process diagram

- **Teardown and Discovery:** The device is disassembled and documented at each step. Pictures are taken of each component, part numbers are identified, and technical datasheets are collected.
- **Component Identification:** Using information from the prior step, component

function is identified and any information needed to interface with the component is documented.

- **Firmware Recovery and Analysis:** Using the technical datasheets, firmware is recovered and analyzed in a disassembler (e.g., Ghidra). Libraries used by the operating system and their opensource repositories are documented. Using the opensource information, potential vulnerabilities are identified within the firmware.
- **Network Traffic Analysis:** Any network traffic created during use is captured and analysed using software tools (e.g., WireShark). In conjunction with prior firmware analysis and identification of operating system libraries, communications are reviewed for potential vulnerabilities. This is a potential area for remote code execution (RCE) if the management software is poorly implemented.
- **USB Communication Analysis:** Communications between the host and device are captured for future development of human-interface-device (HID) cloning. The information is needed for accurately cloning identifiers assuming hosts restrict devices using vendor IDs.
- **Identify RTOS Vulnerabilities:** Should analyses identify any exploitable vulnerabilities, further research is conducted to discover any public releases or proof of concepts (PoCs).
- **RTOS Modification and Development:** Opensource RTOS firmware is modified to allow HID cloning while maintaining original print functionality. The attack vector is crucial step towards proving viability of supply chain attacks using the print devices.
- **RTOS Reimaging and Testing:** Firmware is built and reimaged/reflashed onto the target device. Testing includes the verification of ESC/POS commands interpreter operation and HID attack vector.

4.2 Data Collection Process

The data collection process begins with gathering technical specifications from device manufacturers. Typically, these contain information about the capabilities of the intended device functions. For a printer, this could contain information ranging from hardware specifications (e.g., CPU, architecture, memory) to things like printed pages per minute. This information forms the baseline for the device survey. Afterwards, further specifications will be gathered for components as each device is disassembled and examined.

The next step in the data collection process would be identifying the SoC. In the event that there is no beforehand knowledge, the SoC can be identified by comparing gathered datasheets during the components discovery. This is easily accomplished using an online service like FindChips [32]. The expected type and format for SoCs is described by Figure 4.1.

The process for gathering flash/memory chip specifications is similar; identify serial number and manufacturer, then find the component datasheet. Gathering the pin layouts and format is useful for later stages, should manual flash recovery be needed. The expected format for memory chips can be seen at Figure 4.2.

Specifications	
Architecture	32-bit ARM
Platform	ARM Cortex-M3
Frequency	80-MHz, 100DMIPS performance
Memory	128KB single-cycle Flash memory 64KB single-cycle SRAM
Firmware	Internal ROM loaded with StellarisWare
Advanced Comm. Interfaces	UART, SSI, I2C, I2S, CAN
Debug Interfaces	JTAG, SWD
Package format	100-pin LQFP 108-ball pin BGA

Table 4.1: SoC technical specs example using Stellaris LM3S2793 Microcontroller

The final report will contain each of these tables for the device and their identified core components. Operating system features and protections will be loosely summarized for the device, and there is no set reporting format or requirements. The identified information will aid the final step of the process, creating a design artifact.

Specifications	
Single power supply operation	2.7 to 3.6V
Software Features	SPI Bus Compatible Serial Interface
Memory architecture	Uniform 64KB sectors 256 byte page size
Programming	Page programming (up to 256 bytes) Operations are page-by-page basis Accelerated mode via 9V W#/ACC pin Quad page programming
Erase commands	Bulk erase function Sector erase for 64KB sectors Sub-sector erase for 4KB and 8KB sectors
Protections	W#/ACC pin used with Status Register Bits to protect specified memory regions and configure parts as read-only One time programmable area for permanent and secure identification
Package format	16-pin SO 8-contact WSON 24-ball BGA, 5x5 pin config 24 ball BGA, 6x6 pin config

Table 4.2: Memory specs example using Infineon Technologies S25FL064P [33]

4.3 Hardware Assessment

NIST SP 800-115 [34] provides general guidelines for performing information security testing and assessment, however, there is little information regarding hardware reverse engineering and firmware analysis. Their guidelines are aimed more towards single/multi-tasking operating systems like Windows or Unix-like, those where network logging and listener agents is feasible. For the targeted devices in this research proposal, a different approach is needed that evaluates hardware protections of the SoC and flash memory.

Analysis of device components, once disassembled, requires using a hardware debugger tool with the correct interface. The majority of the targeted devices are expected to use joint test action group (JTAG) or single wire debugging (SWD). By referring to the manufacturer datasheet for a given SoC, it is possible to identify the pin layout for serial debugging access.

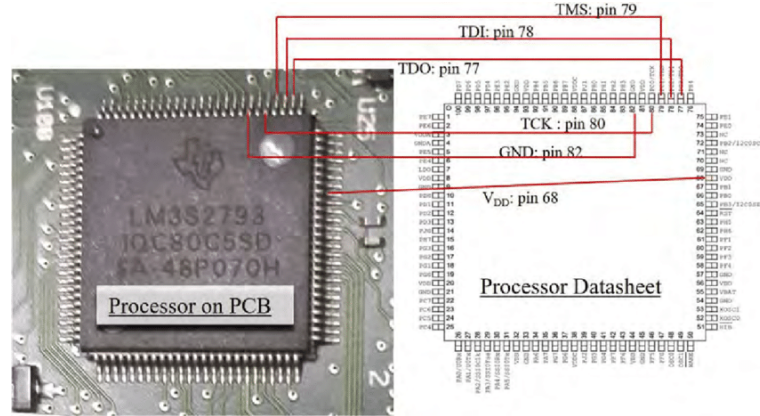


Figure 4.2: JTAG pin out example for Texas Instruments LM3S2793

Figure 4.2 is an example showing what the physical SoC looks like on a PCB compared to the pin layout described in the datasheet. The dot in the top left of the SoC denotes the beginning of the pin layout. Counting in a counter-clockwise method indicates the pin number and the associated functions. For instance, to access the JTAG debug interface on the LM3S2793:

Function	Pin #	Function	Pin #
TDO	77	TDI	78
TMS	79	TCK	80
GND	82	V _{DD}	68

Table 4.3: Example JTAG pin-out for the LM3S2793

Using this information, a device like the JTAGULATOR [35] can be connected and enumerate or verify pin layouts as described. Ball joint SoCs require a different process and are much harder to debug if there is no visible header available on the board. Once an interface is connected, if debugger access is not disabled, the researcher can interact

with the bootloader to further investigate enabled protections and recover flash storage.

If the JTAG is disabled, the researcher will then attempt to recover flash manually using a device like the Segger J-Link [36]. The Segger has pre-defined and existing support for working with flash memory and flash breakpoints, whereas using OpenOCD with the JTAGULATOR would require time crafting custom configurations. Assuming there are no access protections to the flash memory, the researcher can begin performing firmware analysis to identify the operating system or potential vulnerabilities. Documenting the size and address range of memory regions is a key part of the process.

4.4 Network Traffic Analysis

Capturing and understanding the traffic between the serial printer and the host helps to identify incorrect implementations or misconfigurations. This information can then be analyzed to further identify any misuses of authentication methods, cookies, or input validation. All of which are potential areas an attacker could use to leverage unprivileged access.

For example, the Treck TCP/IP networking library, before version 6.0.1.68, had multiple input validation and out-of-bounds read vulnerabilities that allowed attackers unauthenticated remote access [37]–[40]. Following that example, one of the goals of this research is to identify vulnerabilities within the serial printer firmware or networking libraries that could be used to gain unauthenticated access. This is not the only method that will be used to gain access for in-memory modification or reflashing, but it is relevant to identifying supply chain risks and the indirect methods that attackers could use to compromise equipment. Preliminary research into serial devices, and the target of this proposal, identified that the printer uses WebNet v1.0.0 [41]. This library is an independent package developed by RT-Thread to support basic HTTP functionality.

Knowing that information, all network traffic between the serial printer and host will

be captured using WireShark. This will be useful later during firmware analysis because the library is open source and it will provide the researcher with realtime data produced by the library to compare when reviewing the firmware disassembly. During analysis of the network traffic, any URL or call to an API with references to AUTH, CGI, or ASP functions will be documented and tested for input validation [42]. The HPP vulnerability that affected Apple Cups, a common printing system for UNIX systems, is an example: `hxxp://127.0.0.1:631/admin/?kerberos=onmouseover=alert(1)&kerberos`. By modifying the kerberos parameter, it allowed attackers to trigger a cross-site scripting vulnerability.

4.5 USB Communication Analysis

Recording the data transmitted between the host and the printer or target HID provides necessary information for RTOS modification. In order to maintain the appearance of the serial device and cloned HID, device descriptors and vendor IDs are needed [10], [43]. The information will then be used to modify firmware and/or bootloader configuration to allow setting the new IDs needed for the HID cloning attacks. Masking vendor IDs and descriptors is not absolutely necessary when emulating a HID, but it helps bypass whitelists which limit what devices can connect.

Communication between the host, printer, and target HID will be recorded using WireShark and an Ellisys USB Explorer 200. WireShark is a software based solution and it natively provides support for USB protocol logging and analysis [44]. The Ellisys USB Explorer, however, is a hardware and software solution that allows only USB 2.0 analysis. Since both the printer and HID use the USB 2.0 protocol, the explorer is appropriate. Currently, there is no preference for using either tool because of a certain feature or other reason. In the event that data cannot be logged correctly, the other tool will be used.

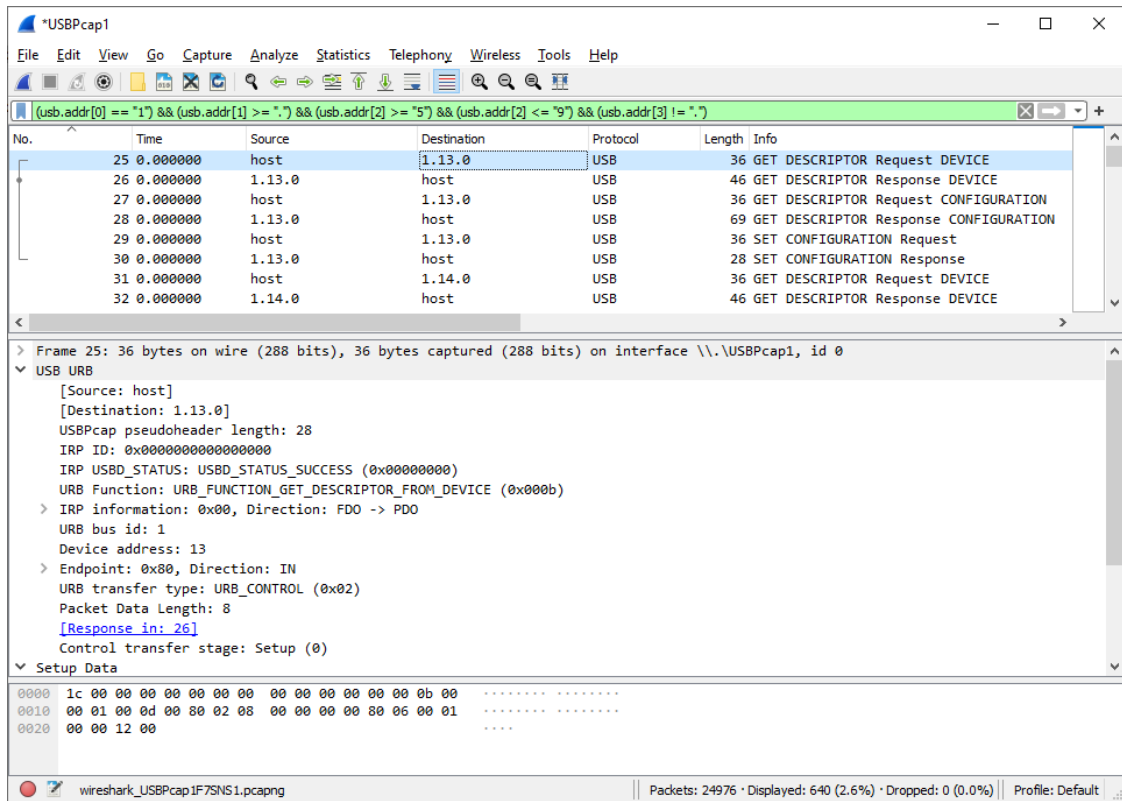


Figure 4.3: USB capture using WireShark

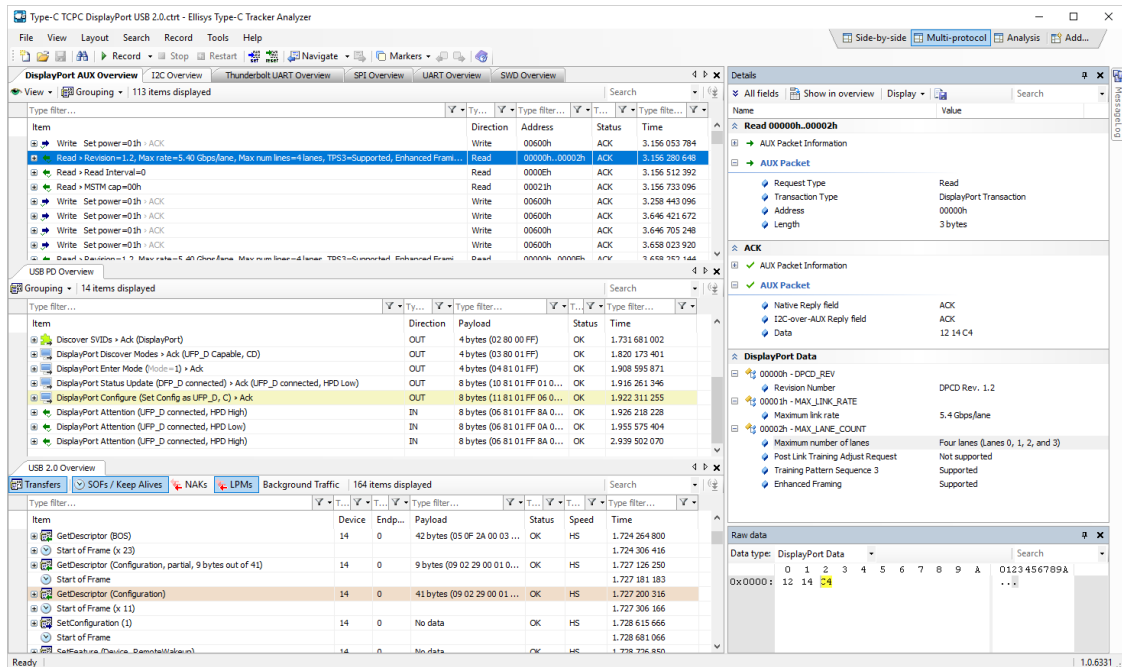


Figure 4.4: Example w/ Ellisys USB Explorer 200

4.6 RTOS Modification

Using the information collected through prior analyses, the firmware will be modified using one of two methods. Either through in-memory exploitation identified through the network and firmware analysis stages or by reflashing firmware manually. Following the Treck vulnerability example, any in-memory modifications would begin through unauthenticated remote code access using a method similar to the heap-based buffer overflow within the HTTP server component. This would allow an attacker to push a payload into memory via the same HTTP server. Depending on the type of payload, the same method used to write into memory could then be used again to trigger the payload. Such a method would require that the payload overwrote a function that is used and exposed by the HTTP server (e.g., CGI/ASP).

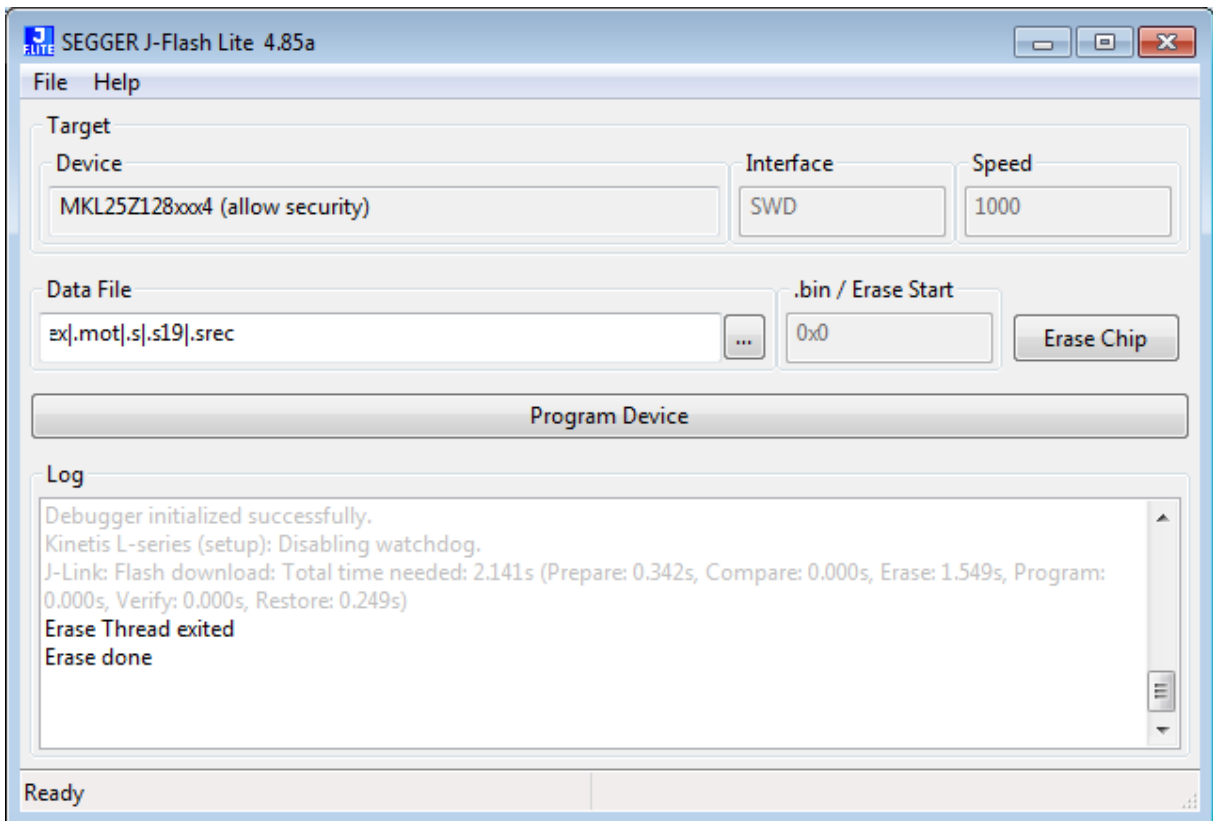


Figure 4.5: Example flashing device using Segger J-Flash [45]

Modification and reflashing of the firmware (RT-Thread) is made easier since it is open source. The print interpreter library (ESC/POS) and HTTP server library (WebNet) are also open source. If there are no identifiable vulnerabilities within the WebNet HTTP server component to enable RCE, rebuilding the firmware is a reliable method and it still fits within the supply chain attack context. Reflashing firmware also assumes that hardware write protections for the flash are not enabled.

Evaluation

Draft: This is the evaluation chapter! Looking at similar papers suggests the following content structure!

- Artifact Objectives
- Data Collection and Implementation
- Reliability and Validity
- Data Analysis

5.1 Artifact Objectives

The artifact produced by this research will be used to demonstrate the potential for supply chain attacks using serial printer devices. There are many potential methods that could be used for assessing weaknesses or attacking a host through a peripheral device, however, time is limited and the scope needs to be definite. As such the research should prove successful through in-memory modifications of the firmware or by manual reflashing. Then the success of either method can be quantified using performance metrics gathered before and after device compromise. Should the firmware modifications exceed the threshold for performance impact or operability, the results will be considered as failing.

5.2 Data Collection and Implementation

Applicability of the data collection and implementation method across other devices is reliant upon the architecture and availability of debug interfaces for the sample device.

The method that will be employed here is specific to Cortex-M3/M4 processors using Serial Wire Viewer (SWV) and kernel-aware (KA) debugging –CITATION–. Using this method should allow greater granularity and realtime collection of the needed metrics. Especially since the data will be collected externally from the hardware and firmware of the sample device, there is no risk that could be imparted from relying on an internal clock to measure the impact of an exploited firmware and/or libraries.

- . ++ Describe in detail what SWV and KA debugging are, how will they be accessed, how will the data be recovered.

5.3 Reliability and Validity

- . ++ Explain reliability of external metrics gathering using hardware debuggers

5.4 Data Analysis

- . ++ Explain and demonstrate how the data analysis will be performed

- . ++ This should be a basic table showing the collected metrics for each pass, as well as the final median values

- . ++ It would likely be best to gather 3 passes targeting ... idle, during print, other functionality (?)

Timeline

	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb
Task	Q1				Q2				Q3			
<i>Review</i>	1.7Wk											
<i>Dissassembly</i>		2 Wks										
<i>Identification</i>		2 Wks										
<i>Analysis</i>			11 Weeks									
<i>Firmware Modification</i>						9 Weeks						
<i>Testing & Evaluation</i>								9 Weeks				
<i>Writing</i>										9 Weeks		

Figure 6.1: Research lifecycle

The timeline for the research proposal is divided into seven parts: review, disassembly, identification, analysis, firmware modification, testing, and writing. The dates provided are rough estimates and will vary as the project progresses. Should any of the tasks take longer than initially estimated, time can be taken from the next or the later writing stage of the dissertation.

The initial phase of the dissertation (e.g., review, disassembly, and identification) is shorter than the rest because the information is readily available and easier to gather. The most difficult step is firmware extraction since it would require manually desoldering the flash chip for retrieval, but that can be completed within a day. If the programming adapter for the component is not already available, then the process could take several more days.

The analysis, modification, evaluation, and writing tasks are equally divided between

nine weeks each. This is not hard set, and it is possible that the analysis or modification stages will need more time. However, each task was initially estimated with that in mind; if more time is needed, it can be borrowed from the evaluation and writing stage.

Research Summary

Securing supply chains for critical infrastructure and any production environment is a growing concern. Third-parties or nation state level attackers have been shown to target employees or infrastructure indirectly to gain access to their target's network. One of the devices being examined to aid this research is the SNBC BTP-S80, a USB/serial connected thermal printer. These devices are made with foreign software and hardware, and they are used off the shelf without any security review. In some instances, the devices implement an MPU/MCU and an FPGA for I/O processing, which creates a potential gap for data to be modified.

Data will be collected by assessing a serial printer and its components, firmware, network stack library, featured capabilities (e.g., intended operations like ESC/POS commands to printed paper over serial), and security protections. Using that information the firmware will be modified in-memory or by reflashing to implement HID cloning for scripted attacks. By demonstrating that the original functionality can be maintained in addition to the attack channel, the research will present a viable supply chain attack that could be used against vendors. The proposed research aims to assess a serial printer for such risks and demonstrate that they could be used as a part of a viable supply chain attack.

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