



PRINTSHOP: SERIAL PRINTER ENVIRONMENTS AND SECURITY

Research Proposal

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Introduction

1.1 Background

Serial printers are devices commonly used for instant reporting of system data for industrial control systems (ICS) and receipts for point-of-sale (POS) systems. These devices are connected to their host using Wi-Fi, bluetooth, ethernet, or USB; in some cases, serial RS232 is an option as well. The goal of this research is to assess what software and hardware protections are enabled, as well as, how configurable the serial printers are for further exploit research.



Figure 1.1: Comparison of common POS systems

Figure 1.1 shows us two similar looking point-of-sale systems, albeit one is much older looking. However, the operating system and required hardware is very different. Typically, unless you have the Square provided terminal, their software/client is installed onto an Android or iOS device and connected to a Square compatible card reader [1]. Whereas, the SurePoS, NCR, or other common EFTPoS system will run a proprietary OS based on Windows or Linux [2]. Furthermore, these PoS tend to require some form of printing receipts as record keeping for the business owner and customer. And these devices also vary in terms of processing capabilities and operating system.

For instance, a common thermal printer seen with PoS systems, integrated with fuel pumps, or other industrial control equipment, is the SNBC BTP-S80 thermal printer [3], [4]. There are multiple versions of the device with support for Bluetooth, USB only, or combination of USB/Serial/Ethernet. The bluetooth hardware is provided over an accessory 25-pin serial connection, with more I/O as a serial connection via RS232C connector and USB Type-B. It has driver support for various platforms: Android, iOS, Windows, Linux, and MacOS. The most interesting aspects are the processor, an Arm Cortex M4 clocked at 3.54MHz, and the operating system, a proprietary version of FreeRTOS. The system architecture is Armv7E-M with JTAG/SWD hardware debugging support [5], [6].

By default, the printer has enough headroom to process ESC/POS commands for printing paper and a webserver for debugging or general diagnostics. In theory, the uncompromised device could be flashed with modified firmware to act as a decoy and human-input-device (HID) against the host PoS. The viability of any vulnerabilities would likely be dependent upon supply chain attacks or physical bait-and-switch tactics [7].

1.2 Significance

According to the Federal Trade Commission (FTC), there were 37,932 reports of credit card fraud in 2012 and 87,451 reports in 2022. This marks an increase of credit card payment fraud by an estimated, 30.5%. By comparison, since 2020, there has been a 14.6% increase in credit card related fraud. Which does not include the millions of other fraud reports the FTC receives every year. In 2022 alone, there were around 5.1 million fraud, identity theft, and miscellaneous reports in total [8], [9]. The statistics for these reports stresses how crucial the security of payment systems are, both physical and online. And, the need to secure them grows every year.

Spyduino is [10] a working example of a programmable BadUSB device using an Arduino to mimic a Human Interface Device (HID). Arduinos are typically more accessible

and easily developed compared to an embedded device whose design is more single purpose. Especially if the goal is to not modify hardware or require hands-on access for exploitation. However, the research shows us that it is possible to create HID clones from scratch if the hardware is compatible.

The Arduino used in their research is powered by an ATmega328P microcontroller with 32KB flash memory, 2KB SRAM, and 1KB EEPROM. Compared to the most likely target device of our proposed research, the SNBC BTP-S80, it features an ARM Cortex M4 microcontroller with 512KB flash memory, 96KB SRAM, 4KB of EEPROM. BadUSBs are a known and tested area of research. The novelty of this proposal comes from the assessment of the printer devices and showing whether one could be used maliciously within their environments (e.g., PoS systems, or ICS).

1.3 Research Goals and Objectives

This research primarily focuses on physical POS systems or terminals and their hardware (serial accessories), rather than online solutions. For instance, not mobile payment apps like Venmo, CashApp, Zelle, or Paypal [11]. There are many reasons, but the types of systems being targeted varies greatly in terms of the hardware and software supported, as well as, how the transactions are handled with the payment processor. Presumably, the host-to-guest communication will not differ greatly between other environments (e.g., ICS). If the printers have demonstrable weaknesses with an Ubuntu host, that will fulfill the testing requirements.

The goal of this research is to further establish academic works in regards to embedded printer devices testing and security. This area is loosely documented within academia and only mentioned vaguely in relation to statistical reports or applied research using entirely different environments. For instance, most researchers limit their analysis of the environment to smartphones and the corresponding payment app, or detection systems

for card skimmers [7]. Through this research we hope to apply gainful conclusions towards the development of an embedded environment for vulnerability assessment, penetration testing, and hardware-to-software interoperability against device hosts. Some examples of how the research could be applied in the future vary: BadUSB/BashBunny [12], JuiceShop [13], DVWA [14], or Webgoat [15]; no such work exists for embedded systems within the point-of-sale or serial printer context.

1.4 Research Questions

The research questions that this proposal seeks to answer are as follows:

- Q1: Can the hardware be reflashed with a modified firmware image (e.g., FreeRTOS, ReconOS, VxWorks)? Testing a version of the original firmware with additional libraries, or an alternative OS, allows us to see if supply chain attacks are a concern. Either by the manufacturer, supplier, or other party.
- Q2: Does the base OS have bandwidth to support HID functionality? In other words, can we maintain operation of standard printer command interpretation and side-channel input attacks without causing crashes or delays? The viability of the attack depends on it going unnoticed by operators or technicians.
- Q3: Besides HID cloning, what other threat areas are exposed (e.g., network stack, web management portal, memory protections)? Are there any identifiable or known exploits when accessing the configuration panel (e.g., HTTP/2)? These provide a non-invasive method for bootstrapping the device.

Each of these goals will be approached individually as prescribed by the methodology.

Related Works

2.1 RTOS: Software and Security

[16] introduces several embedded kernels and discusses their differences in regard to developing a secure mass storage device. For this research, we are primarily interested in RTOS-like kernels because of existing support for a sample device like the SNBC BTP-S80 printer. However, the paper criticizes such operating systems because their "real-time driven design is barely compatible with the overhead produced by security mechanisms." For many applications, there is a trade off with RTOS where performance is the main criteria and security is not a priority. [17] introduces several common RTOS and discusses their security issues. Notably, most RTOS are susceptible to code injection, cryptography inefficiency, unprotected shared memory, priority inversion, denial of service attacks, privilege escalation, and inter-process communication vulnerabilities. Depending on the MPU (microprocessor unit), the vendor has hardware protections like Intel SGX or Arm Trust Zone. These are all areas that can be used for pivoting onto the device, especially shared memory and privilege escalation. If the target device firmware is outdated (or, even libraries used by the firmware) and there are known CVEs that can be repeatedly exploited, persistence mechanisms are not a requirement to gain routine access.

2.2 PoS Attack Patterns

Typically, when discussing attack patterns for PoS systems they are limited to card skimming, fake payment processor requests, or EMV cloning. In rarer cases, they might deliver malware to perform memory scraping within the PoS system or attempt swapping hardware while employees are distracted. None of these attacks include thermal printers at any point during their attack chain or delivery.

Easily the most common and well known type of attack is card skimming. Attackers will place these devices directly on top of the existing equipment to skim, or gather, credit card information at the time of purchases. They can be incredibly difficult to identify because of the sleek and stealthy designs that fraudsters use. But there is plenty of research being presented on how to quickly detect these devices [7], [18].

Without going into too much technical detail, card skimming attacks are accomplished by reading the signals emitted when swiping a magnetic card or by using an NFC reader in proximity to the payment terminal. When the customer goes to pay and uses their card, the nearby skimmer will record the transaction data being transferred. NFC skimmers, however, are not limited to being used near the terminals. Skimmer capabilities vary, and in some cases they have cameras as well or keypads for capturing PIN and zip code data.

In response to the susceptibility of magnetic cards, EMV cards were created. They are able to avoid the issues that magnetic cards and NFC share by using a chip to securely exchange transaction data with the payment terminal using secret authentication codes. The idea is that these codes cannot be tampered with or easily cloned. Despite these security advancements, EMV cards are susceptible to pre-play attacks targeting the "unpredictable number" (UN) algorithm used by ATMs [19].

[11]

Social engineers use payment processor mobile applications to directly target their victims instead of using elaborate and technical attacks against servers or user equipment [20]. The attackers simply send payment requests disguised as payments using their preferred platform. Unwittingly, the victim will accept the request thinking they were receiving money instead.

In some cases, the fraudster sends the victim money but requests a refund shortly after. As a result, the victim is either charged fees for processing the transactions or they have already spent the refunded money. These attacks are much simpler in-terms of delivery compared to the others and the intended outcomes are different. There are

instances where the user device is compromised by malware specifically for exfiltrating banking data or similar PCI, but further discourse is outside the scope of the proposed research [21].

Researchers at Stony Brook University [22], demonstrated a successful introspection-based memory scraping attack against nine commercial PoS applications. Within their environment, it is assumed that the given VM (i.e., Dom0) within the shared virtualization platform (i.e., Xen) is compromised and it has escaped the guest environment. Because the privileges associated with the first VM, it has read access to the others and can perform out-of-VM memory scraping. This exact attack is likely limited to the platform used for the experiment, Xen Hypervisor; attempting something similarly against VMWare, Virtualbox, or QEMU would require further experimentation due to architectural differences. Also, PCI-DSS and PA-DSS requirements were not an obstacle for this attack since the data is not stored to disk and it is read from memory instead.

2.3 BadUSB-like Devices

BadUSB is a well-known and documented attack vector. One of the most popular hacker tools is built-on the concept [12]. However, there are some limitations:

- Precision of attacks is limited since scripts or effects are typically deployed blind. There is no knowledge of the user environment nor ability to interact with functional user interface mechanisms (e.g., a mouse clicking a button).
- Limited to the USB 2.0 standard. Meaning, no support for video adapters like HDMI, DisplayPort, or PowerDelivery like with USB 3.0.
- There are existing methods for limiting USB access from the host, such as GoodUSB [23].

GoodUSB supports the Linux USB stack, so another solution would be required for

Windows systems or RTOS. This all depends on the environment of the connected host, the PoS system. It is entirely possible that the PoS could have software like CrowdStrike Falcon deployed, which would monitor system behavior and mass storage device access [24]. Although the experiment environment will not use such software, it is an important distinction to make.

In [25], they describe several attacks at each of the applicable layers to USB attacks: the human, application, transport, and physical layers. These attacks would typically require some human element for deployment, but that is not the focus of the research (e.g., social engineering versus hardware hacking). Whereas the physical layer could allow signal eavesdropping or injection. This could enable a modified printer to overvolt the host (USBKiller [26]) to cause physical damage or perform other side-channel attacks [27]. Either of those methods would require investigating the device hardware to determine what level of control the bootloader or operating system has over power delivery.

2.4 Summary

As demonstrated by the previous works, vulnerability assessment of an embedded device is a well documented process. However, the extent that a serial thermal printer (e.g., Figure 1.1) can be maliciously expanded through a modified FreeRTOS image, while supporting original functionality, has not. And, given success in the assessment, it could suggest room for continual and improved research.

Proposed Research

3.1 Research Objectives

The goal of this research is to understand the security and threat landscape of serial print device environments; the devices themselves as well as communication between the guest and host. Whether the hardware can support adding unintended functionality at the application and physical layers. And, with what we know about the USB standard and developing real time operating systems, can that functionality be used to create a dual purpose device (e.g., HID clone)?

3.2 Methodology

QUESTION FOR COMMITTEE: Should each of these following areas have their own section w/ more detail?

There are several parts to the methodology of the proposed research. First, technical information and datasheets must be collected for each of the identified devices. Then, device capabilities will be verified before beginning teardown and flash recovery. During the disassembly, each component will be documented and further technical information will be gathered from respective manufacturers. The format for presenting the collected data is described later in section 3.2.2.

Networking traffic will be analyzed according to NIST XYZ (?)...

PARAGRAPH OUTLINE:

- Find exact NIST guideline
- Describe steps as described guideline
- Tools used/needed

- Why is network traffic analysis important?
- How does this pertain to the end goal?

USB host-to-guest communications will be logged with Wireshark. This information will be needed for creation of HID cloning capabilities...

PARAGRAPH OUTLINE:

- Process for USB comm monitoring
- How is this information used for HID cloning?
- What information is needed exactly?
- Tools used?

The firmware will be recovered from flash and reviewed using Ghidra. The guidelines used for the assessment will follow XYZ

PARAGRAPH OUTLINE:

- Why are we reversing the firmware? What information are we looking for?
- How are we reversing the firmware?
- Tools used?

Using the information gathered from the initial analysis of the print device, we will attempt to create a modified version of the operation system with HID cloning and existing functionality. This is to show that the device can either be compromised in the wild or prior as a part of a supply chain attack. HID cloning is then used as a method to demonstrate viable attacks against the host.

3.2.1 Research Approach

For this research, the quantitative approach and case study research will be used [28], [29] to create a design artifact. The goal being to gather and examine, point-in-time, data from a serial printer device as a common sample representative of the affected population. By using quantitative survey research, it is possible to evaluate potential vulnerabilities for the attacks hypothesized, as well as, prototype a modified firmware image to use them against the host environment.

3.2.2 Data Collection Process

The data collection process begins with gathering technical specifications from device manufacturers. Typically, these contain information about the capabilities of the intended device functions. For a printer, this could contain information ranging from hardware specifications (e.g., CPU, architecture, memory) to things like printed pages per minute. This information forms the baseline for the device survey. Afterwards, further specifications will be gathered for components as each device is disassembled and examined.

The next step in the data collection process would be identifying the SoC. In the event that there is no beforehand knowledge, the SoC can be identified by comparing gathered datasheets during the components discovery. This is easily accomplished using an online service like FindChips [30]. The expected type and format for SoCs is described by Figure 3.1.

The process for gathering flash/memory chip specifications is similar; identify serial number and manufacturer, then find the component datasheet. Gathering the pin layouts and format is useful for later stages, should manual flash recovery be needed. The expected format for memory chips can be seen at Figure 3.2.

Specifications	
Architecture	32-bit ARM
Platform	ARM Cortex-M3
Frequency	80-MHz, 100DMIPS performance
Memory	128KB single-cycle Flash memory 64KB single-cycle SRAM
Firmware	Internal ROM loaded with StellarisWare
Advanced Comm. Interfaces	UART, SSI, I2C, I2S, CAN
Debug Interfaces	JTAG, SWD
Package format	100-pin LQFP 108-ball pin BGA

Table 3.1: SoC technical specs example using Stellaris LM3S2793 Microcontroller

The final report will contain each of these tables for the device and their identified core components. Operating system features and protections will be loosely summarized for the device, and there is no set reporting format or requirements. The identified information will aid the final step of the process, creating a design artifact.

Specifications	
Single power supply operation	2.7 to 3.6V
Software Features	SPI Bus Compatible Serial Interface
Memory architecture	Uniform 64KB sectors 256 byte page size
Programming	Page programming (up to 256 bytes) Operations are page-by-page basis Accelerated mode via 9V W#/ACC pin Quad page programming
Erase commands	Bulk erase function Sector erase for 64KB sectors Sub-sector erase for 4KB and 8KB sectors
Protections	W#/ACC pin used with Status Register Bits to protect specified memory regions and configure parts as read-only One time programmable area for permanent and secure identification
Package format	16-pin SO 8-contact WSON 24-ball BGA, 5x5 pin config 24 ball BGA, 6x6 pin config

Table 3.2: Memory specifications example using Infineon Technologies S25FL064P [31]

3.2.3 Hardware Assessment

NIST SP 800-115 [32] provides general guidelines for performing information security testing and assessment, however, there is little information regarding hardware reverse engineering and firmware analysis. Their guidelines are aimed more towards single/multi-tasking operating systems like Windows or Unix-like, those where network logging and listener agents is feasible. For the targeted devices in this research proposal, a different approach is needed that evaluates hardware protections of the SoC and flash memory.

Analysis of device components, once disassembled, requires using a hardware debugger tool with the correct interface. The majority of the targeted devices are expected to use joint test action group (JTAG) or single wire debugging (SWD). By referring to the manufacturer datasheet for a given SoC, it is possible to identify the pin layout for serial debugging access.

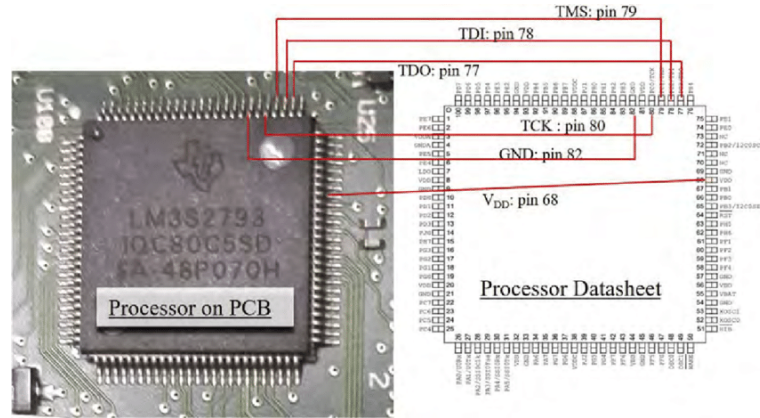


Figure 3.1: JTAG pin out example for Texas Instruments LM3S2793

Figure 3.1 is an example showing what the physical SoC looks like on a PCB compared to the pin layout described in the datasheet. The dot in the top left of the SoC denotes the beginning of the pin layout. Counting in a counter-clockwise method indicates the pin number and the associated functions. For instance, to access the JTAG debug interface on the LM3S2793:

Function	Pin #	Function	Pin #
TDO	77	TDI	78
TMS	79	TCK	80
GND	82	V _{DD}	68

Table 3.3: example JTAG pin-out for the LM3S2793

Using this information, a device like the JTAGULATOR [33] can be connected and enumerate or verify pin layouts as described. Ball joint SoCs require a different process and are much harder to debug if there is no visible header available on the board. Once an interface is connected, if debugger access is not disabled, the researcher can interact with the bootloader to further investigate enabled protections and recover flash storage.

If the JTAG is disabled, the researcher will then attempt to recover flash manually using a device like the Segger J-Link [34]. The Segger has pre-defined and existing support for working with flash memory and flash breakpoints, whereas using OpenOCD with the JTAGULATOR would require time crafting custom configurations. Assuming there are no access protections to the flash memory, the researcher can begin performing firmware analysis to identify the operating system or potential vulnerabilities. Documenting the size and address range of memory regions is a key part of the process.

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