Second Order Type-2 ΔΣ Modulator

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***Abstract* - This paper documents the design process and the experimental results of a second order type-2 ΔΣ modulator. The modulator accepts an analog input signal and produces a binary-valued, PWM-like digital signal with an average voltage equivalent to the input. The modulator uses quantization inside a nonlinear control loop to create an averaging effect on the output signal. A second order type-II loop filter within the control loop contributes noise shaping to reduce noise within the signal bandwidth.**

I. INTRODUCTION

ADC selection depends significantly on circuit application, however desirable traits include a large SNR, especially below the Nyquist frequency and within the signal bandwidth. ΔΣ modulation is a popular choice for ADC applications in low-frequency, high-accuracy measurements [1]. ΔΣ modulators accomplish high SNR by oversampling the input signal and implementing a noise shaping loop filter inside the modulator's nonlinear control loop - this maximizes the SNR within the signal bandwidth and pushes the noise towards high frequencies where it is outside the frequency band of interest. The designed loop filter in this ΔΣ modulator is a second order, type-II filter implemented as a low-pass filter for input signals and high-pass filter for quantization noise. Figure 1 shows the system level block diagram.

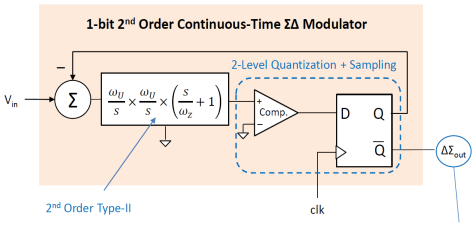


Figure 1: ΔΣ Modulator System Level Diagram [2].

This paper outlines the design process and the experimental results of the ΔΣ modulator starting with circuit derivations and simulations. The circuit was implemented on breadboard block-by-block, and an oscilloscope captured the binary encoded output for various input signals. MATLAB scripts analyzed the output signal with two statistical signal descriptions: the autocorrelation function (ACF) and the power spectral density (PSD).

II. LOOP FILTER

This section outlines two different designs derived for the 2nd-order, type-II loop filter in the ΔΣ modulator control loop. Each filter meets the following specifications [2]:

(1) Natural frequency: $f_n = 5$ kHz
(2) Cutoff frequency: $f_{-3dB} = 2*f_n = 10$ kHz
(3) Unity passband gain: $A_{DC} = 1$

The 2nd order closed-loop transfer function is:

$$H(s) = \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_z}+\frac{s^2}{\omega_u^2}} \quad (1)$$

where $\frac{\omega_z}{\omega_u} = \frac{k}{\sqrt{k^4-2k^2-1}}$, $k = \frac{\omega_{-3dB}}{\omega_u}$ (2)

The first proposed design is a 1st order inverting op-amp in cascade with a 1st order non-inverting op-amp. Figure 2 shows the schematic of the proposed design (see Appendix for design equation and transfer function derivation).

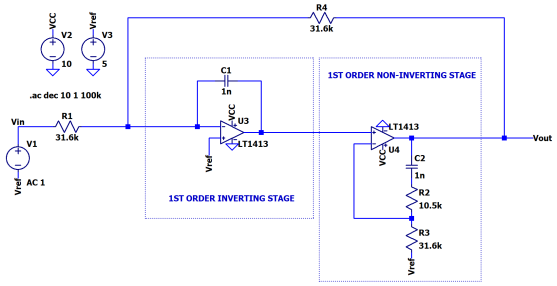


Figure 2: Loop Filter Design #1 Schematic.

The second proposed (and implemented) design is a 2nd order inverting op-amp configuration, as shown in Figure 3. The derivation and transfer function for this design are in the Appendix.

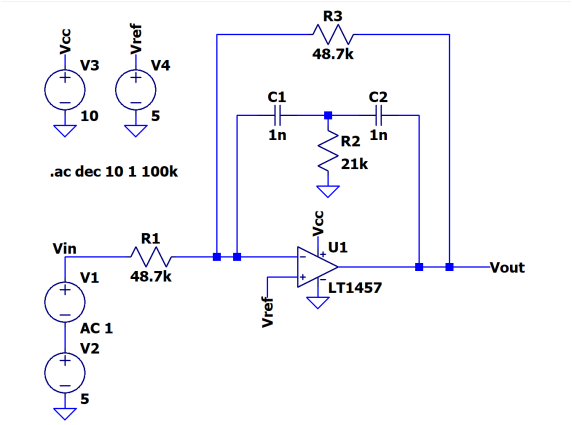


Figure 3: Loop Filter Design #2 Schematic.

Figure 4 shows the simulation results of the second loop filter design. The response is at unity gain for frequencies from DC until 1 kHz and peaks at 2.3dB magnitude at the 5 kHz natural frequency. The stopband rolloff is -40 dB/decade with a -3dB cutoff at ~10.2 kHz - these simulation results meet the design specifications.

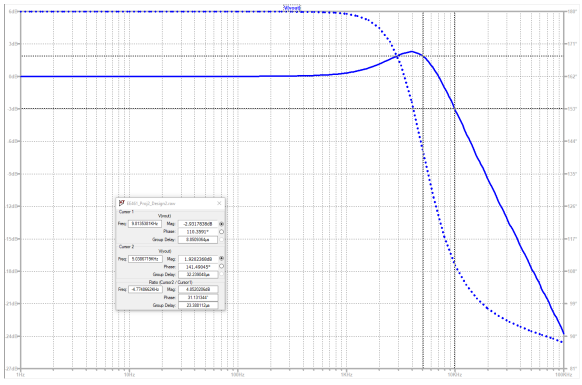


Figure 4: 2nd Order Inverting Loop Filter Simulation.

The implemented ΔΣ modulator uses a single MAX4234 dual op-amp supplied with 0V to 5V rails configured as Design #2. This design requires fewer passive components and only one op-amp, thus justifying the selection. An input $1V_{p-p}$ sinusoidal signal biased at 2.5V DC and a frequency swept between 100Hz-100kHz provided the frequency response shown in Figure 5.

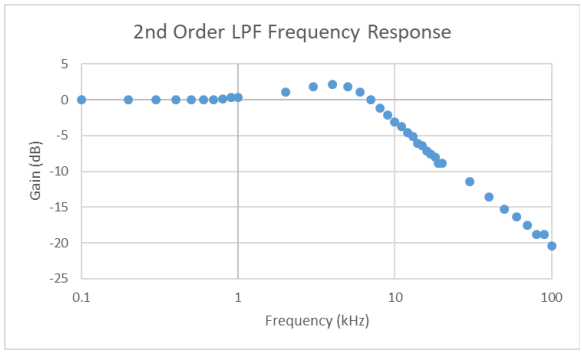


Figure 5: Measured Loop Filter Design #2.

The experimental data confirms that the simulation results yield a unity passband gain, a magnitude peak of 2.2dB at ~5kHz, -3dB cutoff at ~10kHz, and a -40dB/decade stopband rolloff.

III. COMPARATOR & D FLIP-FLOP

The implemented comparator and D flip-flop use LT1712 and CD74HC74M96, respectively. These components provide the quantization and sampling stages in the ΔΣ modulator. Both devices utilize the same 0V-5V rails as the loop filter. Additionally, a 2.5V bias for the input and reference nodes utilize a 100kΩ resistive divider with a 1µF bypass capacitor. This ΔΣ modulator operates on 0V-5V rails instead of ±2.5V because the D flip-flop datasheet specified a recommended operating voltage between 2V-6V [6] whereas the op-amp [4] and comparator [5] operated on either single or split supplies.

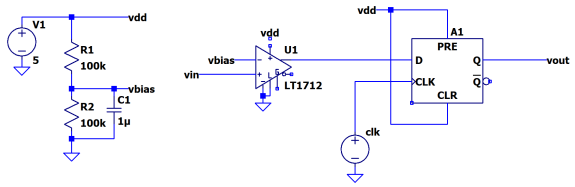


Figure 6: Comparator & D Flip-Flop Schematic [5], [6].

Figure 6 shows the comparator and D flip-flop circuit implemented. First, a function generator supplied a $5V_{p-p}$ sinusoid at 1kHz with $2.5V_{DC}$ offset to the comparator's positive terminal and a $2.5V_{DC}$ bias supplied to the negative terminal. The output (orange waveform) seen in Figure 7 shows the signal driven rail-to-rail when the input crosses the 2.5V threshold. The waveform shows significant glitches in the transition region which is a common characteristic for non-hysteretic comparators.

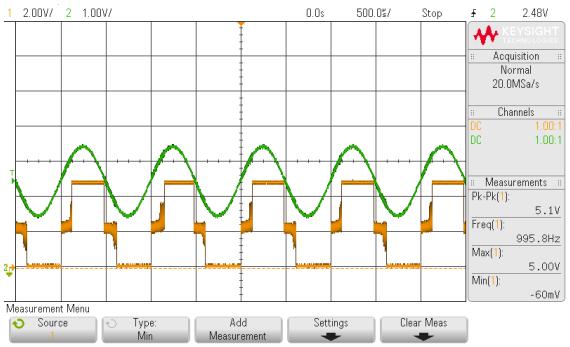


Figure 7: LT1712 Comparator Oscilloscope Capture.

In addition to the sinusoidal input, the function generator supplied a 2 MHz, $5V_{p-p}$ with $2.5V_{DC}$ offset clock signal to the D flip-flop's clock pin. Figure 8 shows the output Q (green) of the D flip-flop and input signal (orange) of the comparator after cascading the D flip-flop. The D flip-flop reduces the transition width, however the component introduces some ringing on the edges of the output waveform.

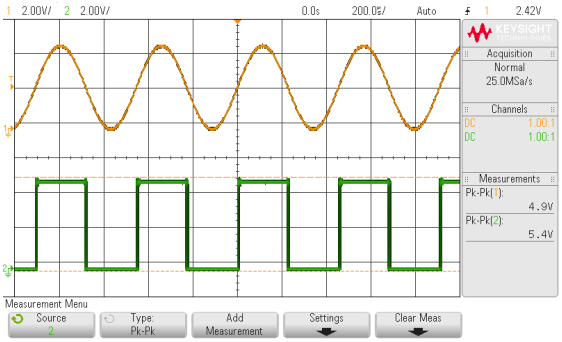


Figure 8: Comparator + DFF Oscilloscope Capture.

IV. ΔΣ Modulator Implementation

Figure 9 shows the complete ΔΣ modulator implemented on a breadboard (see Appendix for full schematics). Two tests validated the ΔΣ modulator: rail-to-rail DC sweep and time-domain measurements for DC and sinusoidal input.

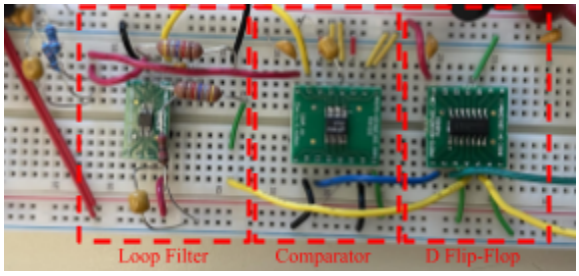


Figure 9: ΔΣ Modulator on Breadboard.

The DC input sweeped from 0V to 5V in 0.5V steps, with the measurements on the oscilloscope taken from fullscreen DC averaging - Figure 11 shows the generated $\Delta\Sigma_{out}$ *vs* V_{in} plot. Figure 12 shows the time-domain output (green) of a $2.5V_{DC}$ input.

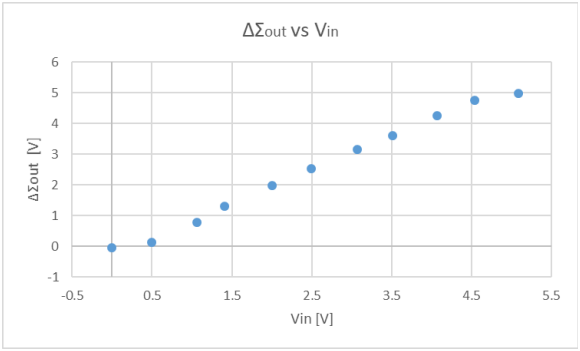


Figure 10: Measured $V_{avg}(\Delta\Sigma_{out})$ vs. V_{in}.

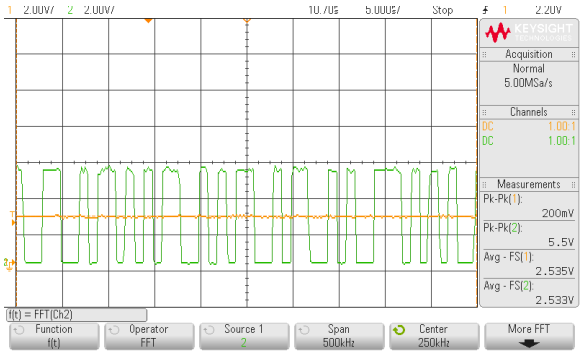


Figure 12: 2.5V DC Input Capture of Input (yellow) and Output (green).

The linear ramping trend with a slope of 1 is expected in Figure 12 - this plot confirms that the ΔΣ modulator average output voltage is equal to the input voltage. When zooming into the time-domain response (Figure 12), the output waveform appears PWM-like as expected due to the negative feedback loop that corrects the output voltage by pulling the output low when the input is above the threshold and pulling the output high when the input is a little below the threshold [3].

The next validation tests include time domain measurements for DC and sinusoidal inputs. Figure 13 and Figure 14 show the PSD and ACF of a $2.5V_{DC}$ input to the ΔΣ modulator. Note that the design is on 0V to 5V rails - the input $2.5V_{DC}$ is equivalent to 0V on a ±2.5V rail system. The MATLAB processed data normalized the data around 0V with ±2.5V rails.

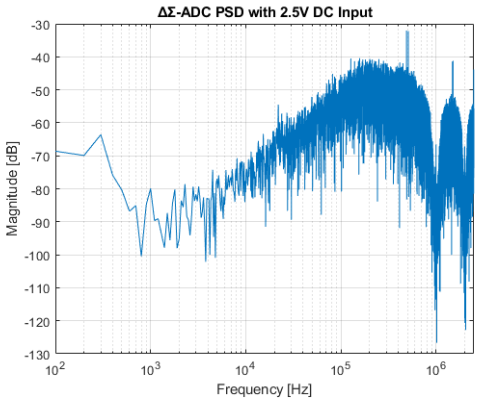


Figure 13: $\Delta\Sigma_{out}$ PSD with 2.5V DC Input.

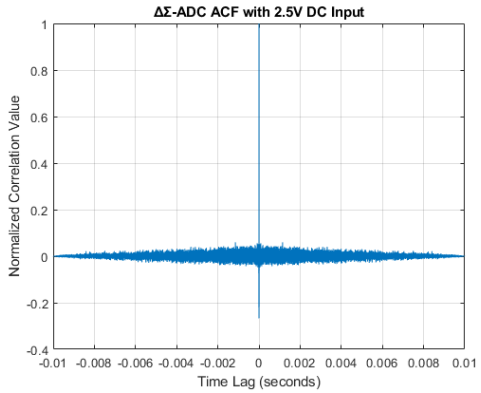


Figure 14: $\Delta\Sigma_{out}$ ACF with 2.5V DC Input.

The output PSD shows the desired noise shaping response where the ΔΣ modulator pushes noise towards higher frequencies away from the desired passband region. The slope is approximately +40dB/dec as expected for 2nd-order filters. The slope begins at ~10kHz (the same 10kHz cutoff frequency set by the loop filter). The output PSD shows a high-pass filter response since the loop filter is a low-pass filter for input signals and a high-pass filter for quantization noise. The normalized ACF (Figure 14) has a peak correlation value at zero lag and nearly zero correlation for all other sample times - this is equivalent to white noise.

The second test case inputted a $2V_{p\text{-}p}$ 1kHz sine wave with $2.5V_{DC}$ offset. Figures 15 and 16 show the output PSD and ACF, respectively. The output PSD shows the desired noise shaping characteristic similar to the DC input test case. However, the 1kHz sinusoidal input contributes a frequency peak on the PSD at ~1kHz since it is within the passband. The passband also has >60dBc SNR with the 1kHz signal which is significantly higher than the potential 25dBc if the high frequency noise were considered the noise floor without the ΔΣ modulator noise shaping.

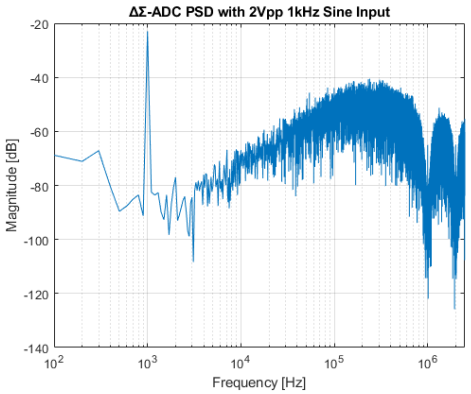


Figure 15: $\Delta\Sigma_{out}$ PSD with $2V_{pp}$, $2.5V_{DC}$ 1kHz Sine Input.

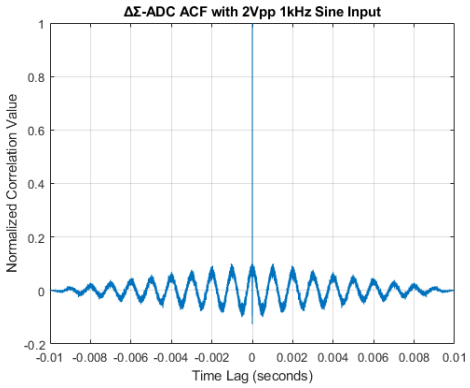


Figure 16: $\Delta\Sigma_{out}$ ACF with $2V_{pp}$ $2.5V_{DC}$ 1kHz Sine Input.

The normalized ACF shown in Figure 16 has higher autocorrelation values and a periodic correlation compared to the DC input signal (Figure 14). The input signal's periodicity results in peak correlation values at consistent intervals matching the signal frequency whereas white noise has ideally zero correlation outside zero lag values. The period of the ACF in Figure 16 matches the period of the input signal at 1ms. The ends of the ACF in Figure 14 and Figure 16 taper off due to the limited number of samples collected.

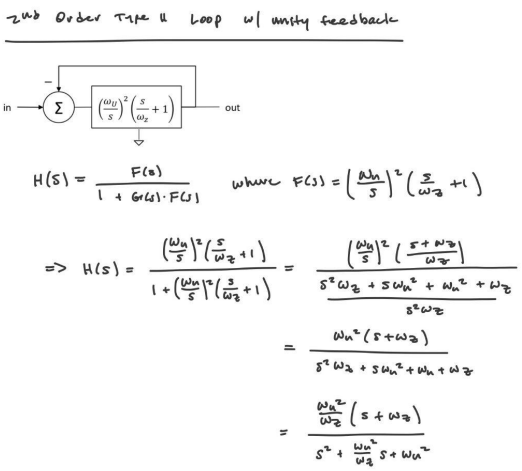
V. CONCLUSION

The experimental results of the ΔΣ modulator demonstrated that the implemented circuit meets the following design requirement: +40dB/dec noise shaping for high frequencies starting at 10kHz. The ΔΣ modulator also improves the SNR up to 60dBc with a signal input within the passband. In addition, the experimental results demonstrated successful input signal encoding as a PWM-like signal.

VI. APPENDIX

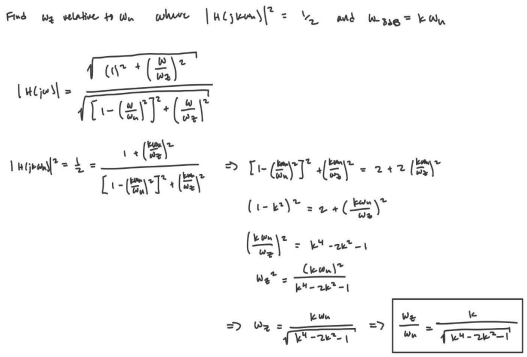
This appendix lists the key project deliverables and additional derivations and screen captures to implement the ΔΣ modulator.

1. Expression for the TF of a 2nd Order Type-II Loop under Unity Feedback



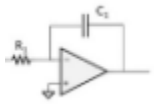
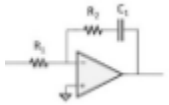
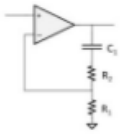
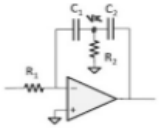
$$H(s) = \frac{1+\frac{s}{\omega_z}}{1+\frac{1}{\omega_z}s+\frac{1}{\omega_u^2}s^2}$$

2. Value of ω_Z (relative to ω_U) that yields close loop 3dB cutoff $\omega_{-3dB} = k\omega_U$



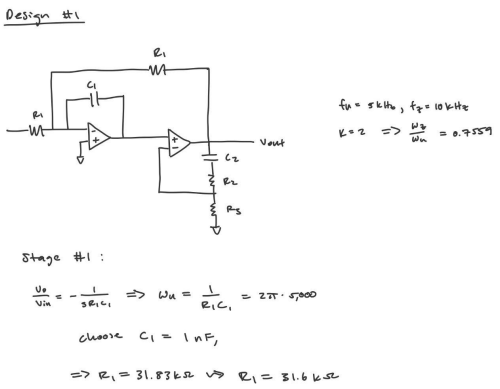
$$\frac{\omega_z}{\omega_u} = \frac{k}{\sqrt{k^4-2k^2-1}}$$

3. Table that lists the TF of the four op amp based 'integrator' structures:

Schematic	Transfer Function
 1st Order Inverting Integrator	$\frac{Vo}{Vin} = -\frac{1}{sR_1C}$ $\omega_u = \frac{1}{R_1C}$
 1st Order Inverting Integrator	$\frac{Vo}{Vin} = -\frac{[1+sR_2C_1]}{sR_1C_1}$ $\omega_u = \frac{1}{R_1C_1}$ $\omega_z = \frac{1}{R_2C_1}$
 1st Order Non-Inverting Integrator	$\frac{Vo}{Vin} = \frac{1+sC_1[R_1+R_2]}{sR_1C_1}$ $\omega_u = \frac{1}{R_1C_1}$ $\omega_z = \frac{1}{(R_1+R_2)C_1}$
 2nd Order Inverting Integrator	$\frac{Vo}{Vin} = -\frac{[1+s(R_2C_1+R_2C_2)]}{s^2R_1C_1R_2C_2}$ $\omega_u = \frac{1}{\sqrt{R_1C_1R_2C_2}}$ $\omega_z = \frac{1}{R_2(C_1+C_2)}$

4. Two designs of loop filter implementing LP close-loop response with f_n=5kHz, f_{-3dB}=10kHz, and A_{DC}=1.

   The first design is a cascade of one inverting integrator and one non-inverting first order integrator.



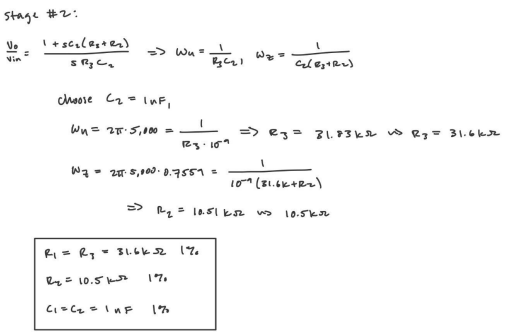


Figure 17 shows the completed design with specified resistor and capacitor values. The resistors are 1% tolerance and capacitors are 5% tolerance. Figure 18 shows the LTSpice simulation for frequency response.

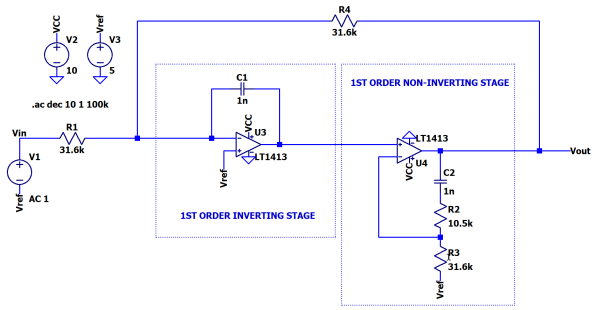


Figure 17: Loop Filter Design #1 Schematic.

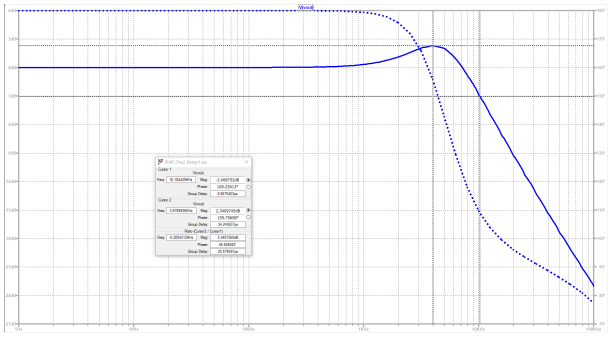
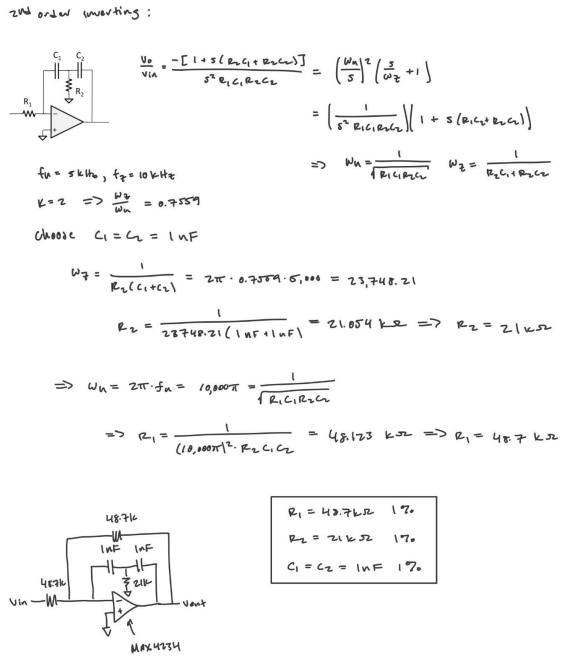


Figure 18: Loop Filter Design #1 Frequency Response Simulation.

The frequency response in Figure 18 shows the desired natural frequency at ~5kHz and the -3dB cutoff frequency at ~10kHz. There is also unity passband gain up until ~1kHz where the magnitude begins to peak which is characteristic of 2nd order filters. Compared to the design implemented, the frequency response is identical, however there are more components used including an additional op-amp.

The second design, shown in Figure 3, derives from the following analysis:



The resistors are 1% tolerance and capacitors are 5% tolerance. The selected op-amp is MAX4234 which is a dual package component so either design #1 or design #2 can be implemented.

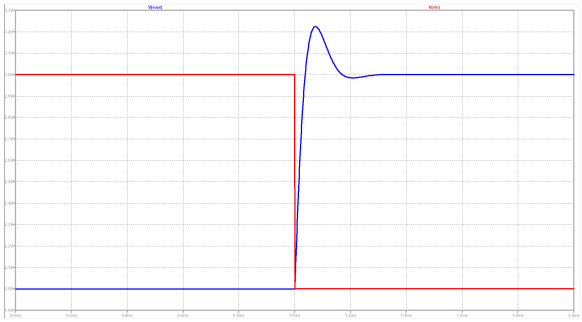


Figure 19: Simulated Loop Filter Design #2 Step Response.

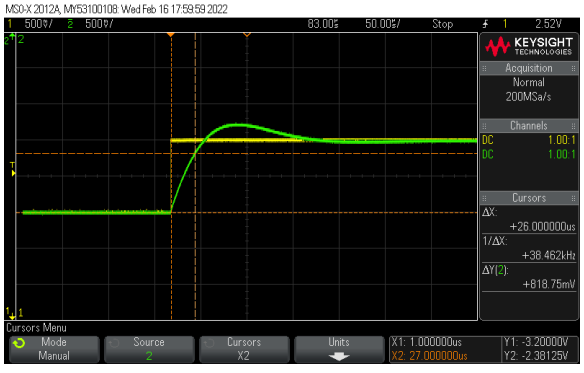


Figure 20: Measured Loop Filter Design #2 Step Response.

Figures 19 and 20 demonstrate a step response to the implemented loop filter. The experimental waveform has a

similar underdamped response to the simulation result, however they vary slightly due to the op-amp model differing from the actual component used.

The choice to run the supply 0V to 5V is a result of the CD74HC74M96 datasheet specifying an optimal operating range between 2V and 6V whereas the remaining ICs operate in either split or single supply. As a result, the input signal required biasing at 2.5V. The data captured did not AC couple the signal which caused errors in MATLAB analysis for the ACF, as shown in Figure 19. However removing the input bias in post processing corrected the ACF as seen in Figures 14 and 16.

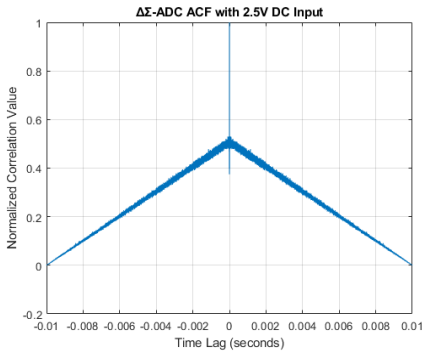


Figure 19: 2.5V DC Input ACF with No AC Coupling.

The complete circuit schematic is shown in Figure 20. All resistor values are 1% tolerance and all capacitor values are 5% tolerance.

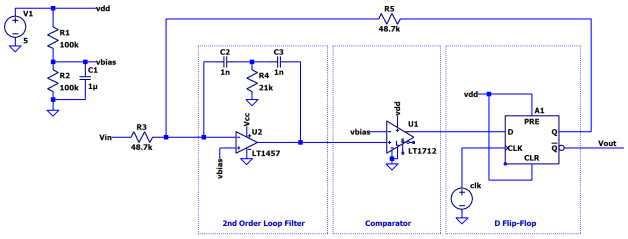


Figure 20: ΔΣ Modulator System Schematic.

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Category	Results	Goal
Passive voice	1 (0%)	Less than 10%
Wordiness	3 (2%)	Less than 2%
Sentences	0 (0%)	Less than 2%
Transitions	18 (16%)	More than 10%
Academic Style	3 (0%)	Less than 1%
Grammar	0	0 errors
Nominalizations	58 (4%)	Less than 6%
Eggcorns	0	0 errors