# LM4811 Boomer® Audio Power Amplifier Series Dual 105mW Headphone Amplifier with Digital Volume Control and Shutdown Mode

**Check for Samples: LM4811**

## FEATURES

- **Digital Volume Control Range from +12dB to −33dB**
- **WSON and VSSOP Surface Mount Packaging**
- **"Click and Pop" Suppression Circuitry**
- **No Bootstrap Capacitors Required**
- **Low Shutdown Current**

## APPLICATIONS

- **Cellular Phones**
- **MP3, CD, DVD Players**
- **PDA's**
- **Portable Electronics**

## KEY SPECIFICATIONS

- **THD+N at 1kHz, 105mW Continuous Average Output Power into 16Ω 0.1 % (typ)**
- **THD+N at 1kHz, 70mW Continuous Average Power into 32Ω 0.1 % (typ)**
- **Shutdown Current 0.3 µA (typ)**

## DESCRIPTION

The LM4811 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4811 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4811 features a digital volume control that sets the amplifier's gain from +12dB to −33dB in 16 discrete steps using a two−wire interface.

The unity-gain stable LM4811 also features an externally controlled, active-high, micropower consumption shutdown mode. It also has an internal thermal shutdown protection mechanism.

## Connection Diagrams

**Top View**

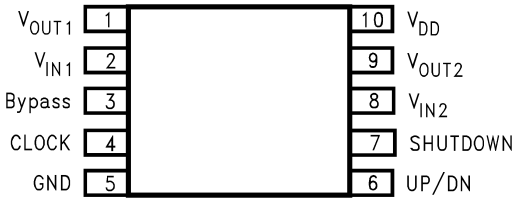



**Figure 1. VSSOP Package**
**See Package Number DGS0010A**

**Top View**

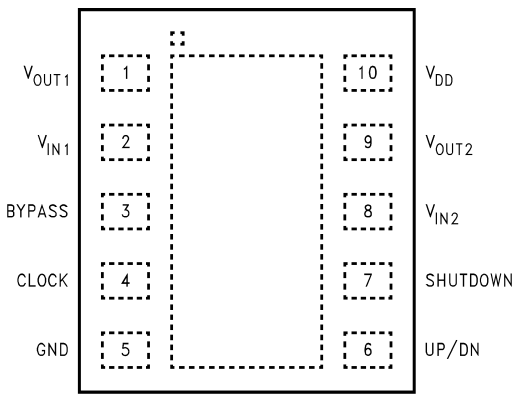



**Figure 2. WSON Package**
**See Package Number NGY0010A**

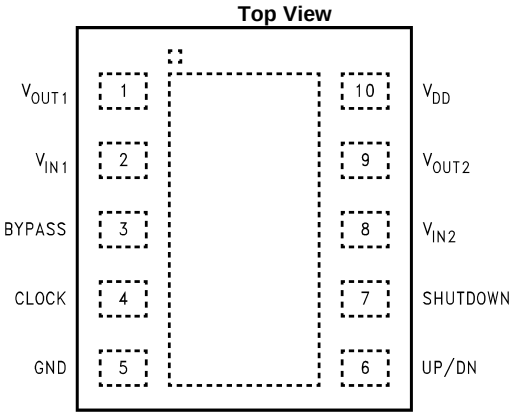
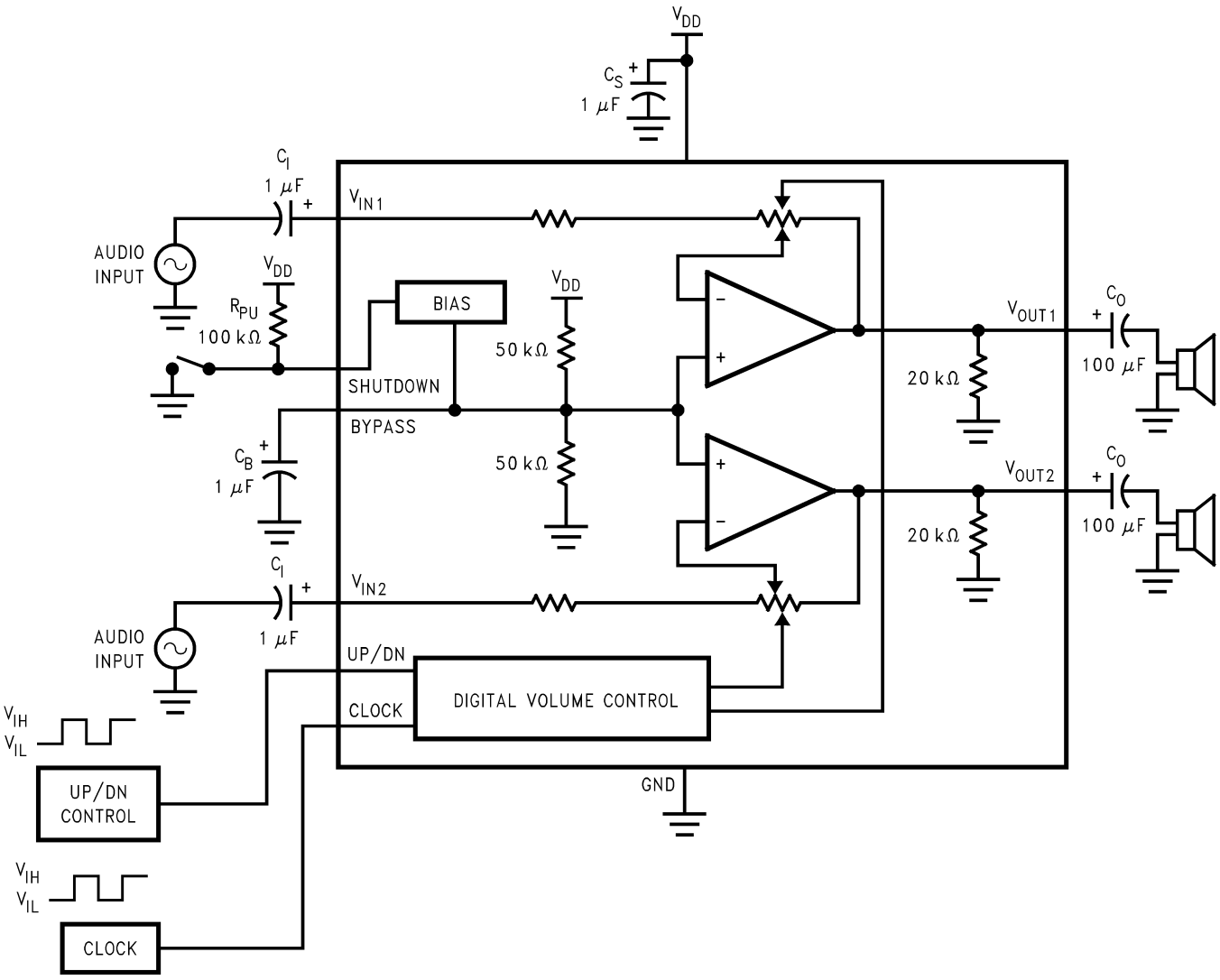



**Figure 3. SON Package**
**See Package Number NHD0010A**

## Typical Application




*Refer to Application Information for information concerning proper selection of the input and output coupling capacitors.

**Figure 4. Typical Audio Amplifier Application Circuit**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)(2)

| | | | |
|---|---|---|---|
| Supply Voltage | | | 6.0V |
| Storage Temperature | | | −65°C to +150°C |
| ESD Susceptibility (3) | | | 2.5kV |
| ESD Susceptibility Machine model (4) | | | 200V |
| Junction Temperature ($T_J$) | | | 150°C |
| Soldering Information | DGS0010A Package | Vapor Phase (60 sec.) | 215°C |
| | | Infrared (15 sec.) | 220°C |
| Thermal Resistance | $\theta_{JA}$ DGS0010A | | 194°C/W |
| | $\theta_{JC}$ DGS0010A | | 52°C/W |
| | $\theta_{JA}$ NGY0010A (5) | | 63°C/W |
| | $\theta_{JC}$ NGY0010A (5) | | 12°C/W |
| | $\theta_{JA}$ NHD0010A (5) | | 63°C/W |
| | $\theta_{JC}$ NHD0010A (5) | | 12°C/W |

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50 Ohms).
(5) The NGY0010A or NHD0010A package has its Exposed−DAP soldered to an exposed $2in^2$ area of 1oz printed circuit board copper.

## Operating Ratings

| | | |
|---|---|---|
| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ | −40°C ≤ $T_A$ ≤ 85°C |
| Supply Voltage | | 2.0V ≤ $V_{CC}$ ≤ 5.5V |

## Electrical Characteristics (1)(2)

The following specifications apply for $V_{DD}$ = 5V unless otherwise specified, limits apply to $T_A$ = 25°C.

| Parameter | | Test Conditions | LM4811 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typ (3) | Limit (4) | |
| $V_{DD}$ | Supply Voltage | | | 2.0<br>5.5 | V (min)<br>V (max) |
| $I_{DD}$ | Supply Current | $V_{IN}$ = 0V, $I_O$ = 0A | 1.3 | 3.0 | mA |
| $I_{SD}$ | Shutdown Current | $V_{IN}$ = 0V | 0.3 | | µA |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V | 4.0 | 50 | mV |
| $P_O$ | Output Power | 0.1% THD+N; f = 1kHz | | | |
| | | $R_L$ = 16Ω | 105 | | mW |
| | | $R_L$ = 32Ω | 70 | | mW |
| THD+N | Total Harmonic Distortion | $P_O$ = 50mW, $R_L$ = 32Ω<br>f = 20Hz to 20kHz | 0.3 | | % |
| Crosstalk | Channel Separation | $R_L$ = 32Ω; f = 1kHz;<br>$P_O$ = 70mW | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $C_B$ = 1.0µF, $V_{RIPPLE}$ = 100m$V_{PP}$<br>f = 217Hz | 60 | | dB |
| $V_{IH}$ | (CLOCK, UP/DN, SHUTDOWN)<br>Input Voltage High | | | 1.4 | V (min) |

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

## Electrical Characteristics [1][2] (continued)

The following specifications apply for $V_{DD}$ = 5V unless otherwise specified, limits apply to $T_A$ = 25°C.

| Parameter | | Test Conditions | LM4811 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typ[3] | Limit [4] | |
| $V_{IL}$ | (CLOCK, UP/DN, SHUTDOWN) Input Voltage Low | | | 0.4 | V (max) |
| | Digital Volume Range | Input referred minimum gain | −33 | | dB |
| | | Input referred maximum gain | +12 | | dB |
| | Digital Volume Stepsize | All 16 discrete steps | 3.0 | | dB |
| | Stepsize Error | All 16 discrete steps | ±0.3 | | dB |
| | Channel−to−Channel Volume Tracking Error | All gain settings from −33dB to +12dB | 0.15 | | dB |
| | Shutdown Attenuation | Shutdown mode active | −100 | | dB |

## Electrical Characteristics [1][2]

The following specifications apply for $V_{DD}$ = 3.3V unless otherwise specified, limits apply to $T_A$ = 25°C.

| Parameter | | Test Conditions | LM4811 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typ[3] | Limit [4] | |
| $I_{DD}$ | Supply Current | $V_{IN}$ = 0V, $I_O$ = 0A | 1.1 | | mA |
| $I_{SD}$ | Shutdown Current | $V_{IN}$ = 0V | 0.3 | | µA |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V | 4.0 | | mV |
| $P_o$ | Output Power | 0.1% THD+N; f = 1kHz | | | |
| | | $R_L$ = 16Ω | 40 | | mW |
| | | $R_L$ = 32Ω | 28 | | mW |
| THD+N | Total Harmonic Distortion | $P_O$ = 25mW, $R_L$ = 32Ω f = 20Hz to 20kHz | 0.5 | | % |
| PSRR | Power Supply Rejection Ratio | $C_B$ = 1.0µF, $V_{RIPPLE}$ = 100m$V_{PP}$ f = 217Hz | 60 | | dB |
| $V_{IH}$ | (CLOCK, UP/DN, SHUTDOWN) Input Voltage High | | 1.4 | | V (min) |
| $V_{IL}$ | (CLOCK, UP/DN, SHUTDOWN) Input Voltage Low | | 0.4 | | V (max) |
| | Digital Volume Range | Input referred minimum gain | −33 | | dB |
| | | Input referred maximum gain | +12 | | dB |
| | Digital Volume Stepsize | All 16 discrete steps | 3.0 | | dB |
| | Stepsize Error | All 16 discrete steps | ±0.3 | | dB |
| | Channel−to−Channel Volume Tracking Error | All gain settings from −33dB to +12dB | 0.15 | | dB |
| | Shutdown Attenuation | Shutdown mode active | −100 | | dB |

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

## Electrical Characteristics (1)(2)

The following specifications apply for $V_{DD}$ = 2.6V unless otherwise specified, limits apply to $T_A$ = 25°C.

| Parameter | | Test Conditions | LM4811 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typ(3) | Limit (4) | |
| $I_{DD}$ | Supply Current | $V_{IN}$ = 0V, $I_O$ = 0A | 1.0 | | mA |
| $I_{SD}$ | Shutdown Current | $V_{IN}$ = 0V | 0.3 | | µA |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V | 4.0 | | mV |
| $P_o$ | Output Power | 0.1% THD+N; f = 1kHz | | | |
| | | $R_L$ = 16Ω | 20 | | mW |
| | | $R_L$ = 32Ω | 16 | | mW |
| THD+N | Total Harmonic Distortion | $P_O$ = 15mW, $R_L$ = 32Ω<br>f = 20Hz to 20kHz | 0.6 | | % |
| PSRR | Power Supply Rejection Ratio | $C_B$ = 1.0µF, $V_{RIPPLE}$ = 100m$V_{PP}$<br>f = 217Hz | 60 | | dB |
| $V_{IH}$ | (CLOCK, UP/DN, SHUTDOWN)<br>Input Voltage High | | 1.4 | | V (min) |
| $V_{IL}$ | (CLOCK, UP/DN, SHUTDOWN)<br>Input Voltage Low | | 0.4 | | V (max) |
| | Digital Volume Range | Input referred minimum gain | −33 | | dB |
| | | Input referred maximum gain | +12 | | dB |
| | Digital Volume Stepsize | All 16 discrete steps | 3.0 | | dB |
| | Stepsize Error | All 16 discrete steps | ±0.3 | | dB |
| | Channel−to−Channel Volume Tracking Error | All gain settings from<br>−33dB to +12dB | 0.15 | | dB |
| | Shutdown Attenuation | Shutdown mode active | −75 | | dB |

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

## External Components Description

| Components | Functional Description (See Figure 4) |
|---|---|
| 1. $C_i$ | This is the input coupling capacitor. It blocks the DC voltage at, and couples the input signal to, the amplifier's input terminals. $C_i$ also creates a highpass filter with the internal input resistor, $R_i$, at $f_c = 1/(2\pi R_i C_i)$. The minimum value of $R_i$ is 33kΩ. Refer to PROPER SELECTION OF EXTERNAL COMPONENTS for an explanation of how to determine the value of $C_i$. |
| 2. $C_S$ | This is the supply bypass capacitor. It provides power supply filtering. Refer to Application Information for proper placement and selection of the supply bypass capacitor. |
| 3. $C_B$ | This is the BYPASS pin capacitor. It provides half-supply filtering. Refer to PROPER SELECTION OF EXTERNAL COMPONENTS for information concerning proper placement and selection of $C_B$. |
| 4. $C_O$ | This is the output coupling capacitor. It blocks the DC voltage at the amplifier's output and it forms a high pass filter with $R_L$ at $f_O = 1/(2\pi R_L C_O)$ |

## Typical Performance Characteristics

**THD+N vs Frequency**

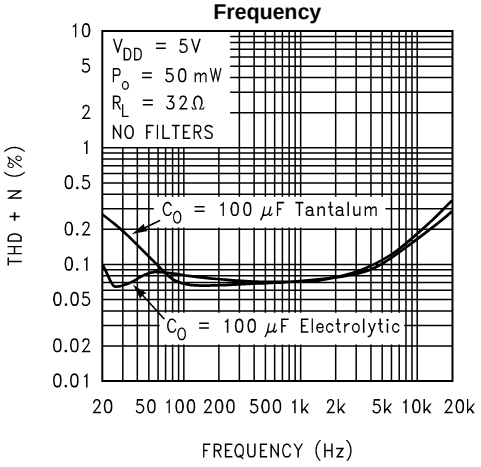



**Figure 5.**

**THD+N vs Frequency**

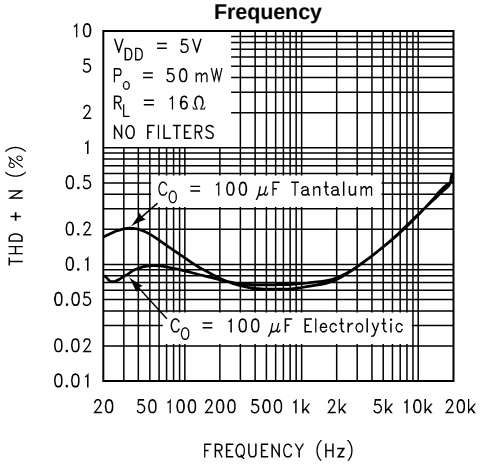



**Figure 6.**

**THD+N vs Frequency**

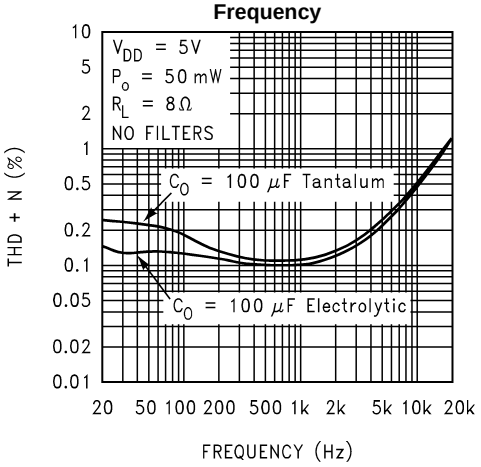



**Figure 7.**

**THD+N vs Frequency**

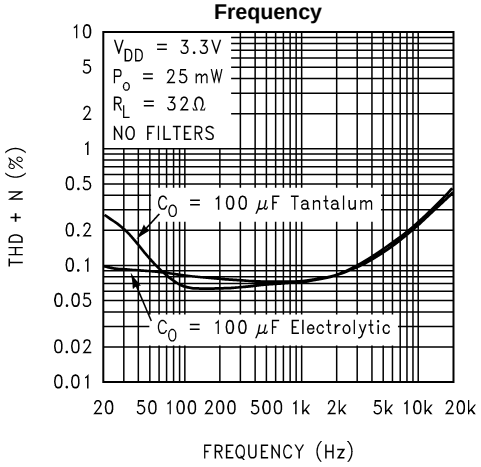



**Figure 8.**

**THD+N vs Frequency**

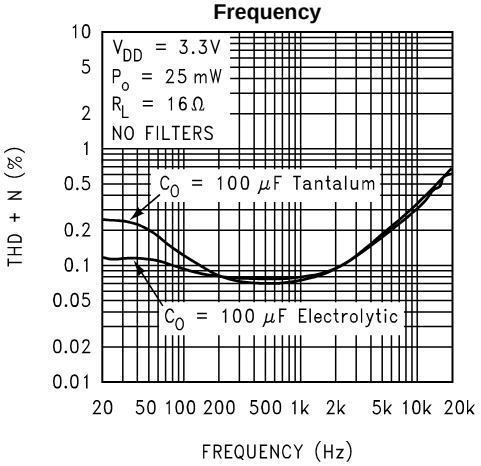



**Figure 9.**

**THD+N vs Frequency**

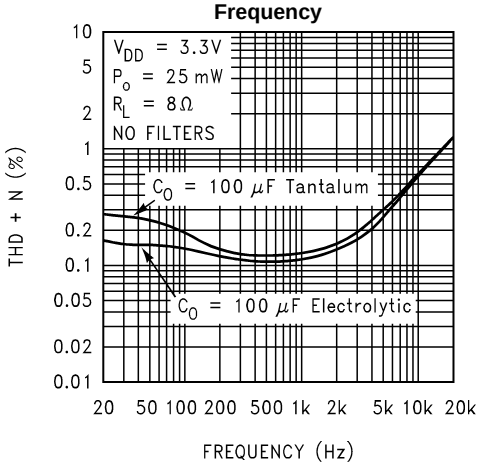



**Figure 10.**

## Typical Performance Characteristics (continued)

**THD+N vs Frequency**

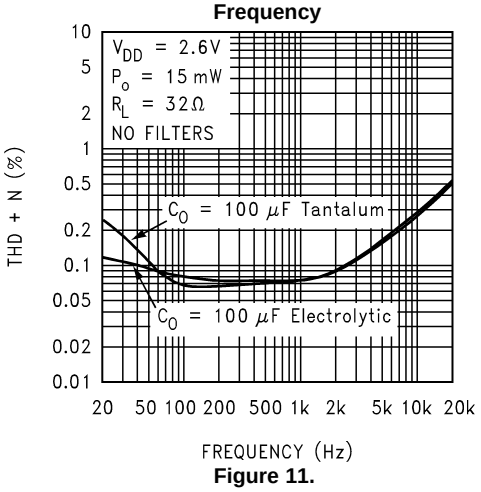



**Figure 11.**

**THD+N vs Frequency**

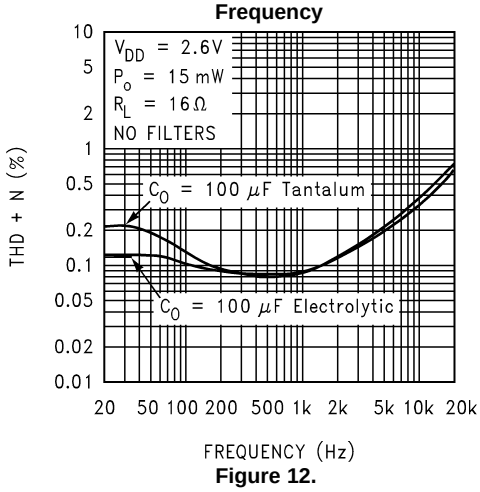



**Figure 12.**

**THD+N vs Frequency**

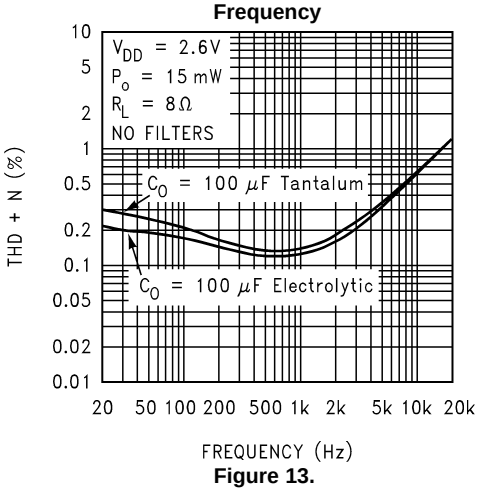



**Figure 13.**

**THD+N vs Output Power**

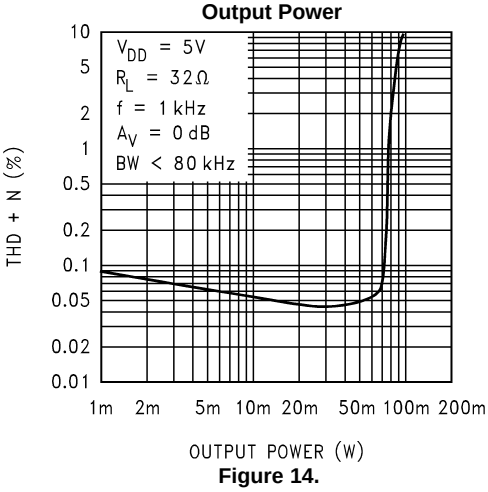



**Figure 14.**

**THD+N vs Output Power**

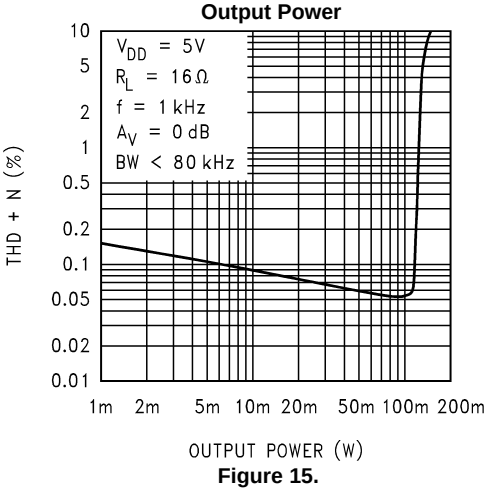



**Figure 15.**

**THD+N vs Output Power**

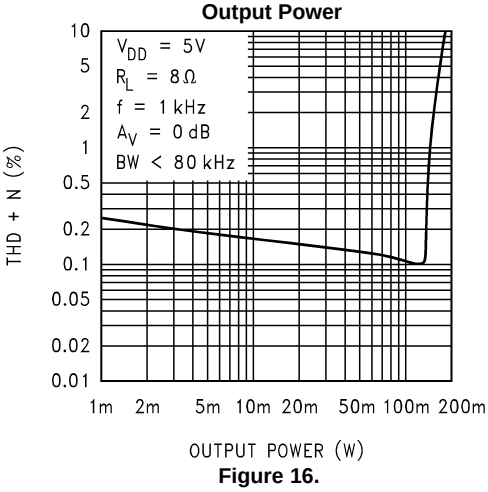



**Figure 16.**

## Typical Performance Characteristics (continued)

**THD+N vs Output Power**

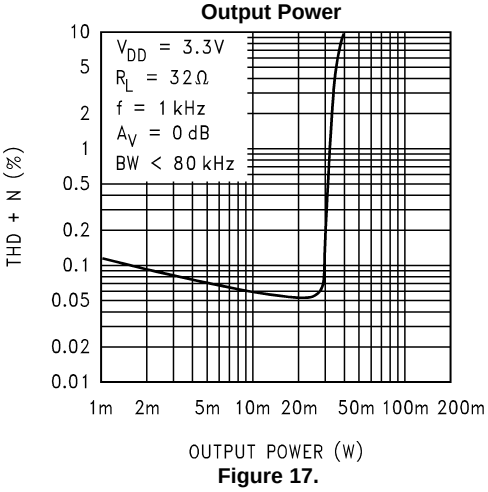



**Figure 17.**

**THD+N vs Output Power**

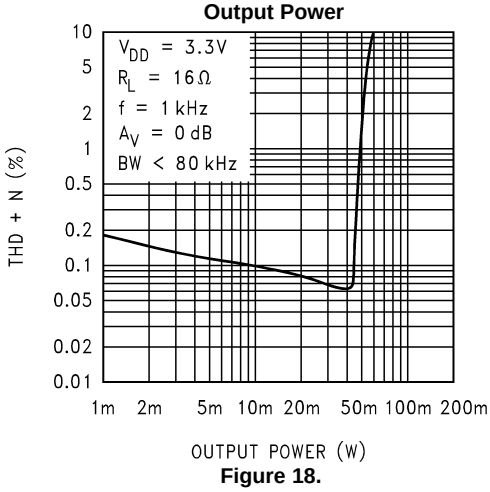



**Figure 18.**

**THD+N vs Output Power**

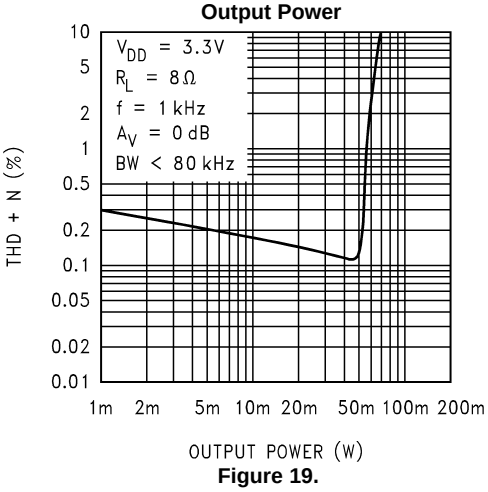



**Figure 19.**

**THD+N vs Output Power**

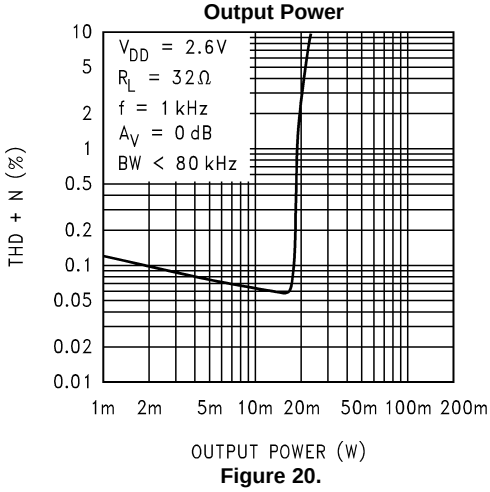



**Figure 20.**

**THD+N vs Output Power**

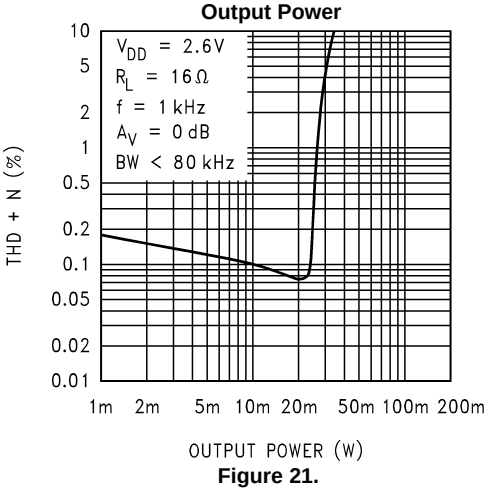



**Figure 21.**

**THD+N vs Output Power**

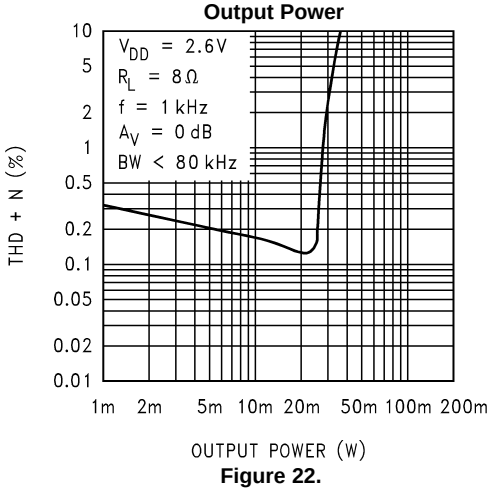



**Figure 22.**

## Typical Performance Characteristics (continued)

**Output Power vs Load Resistance**

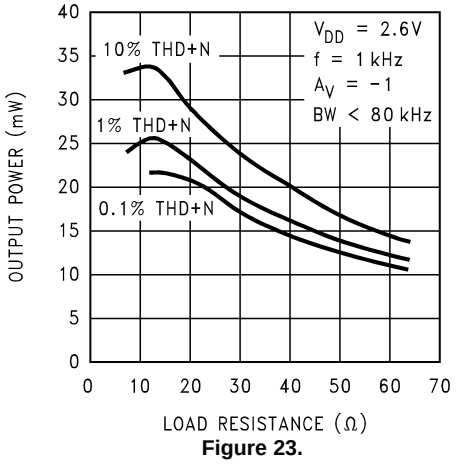



**Figure 23.**

**Output Power vs Load Resistance**

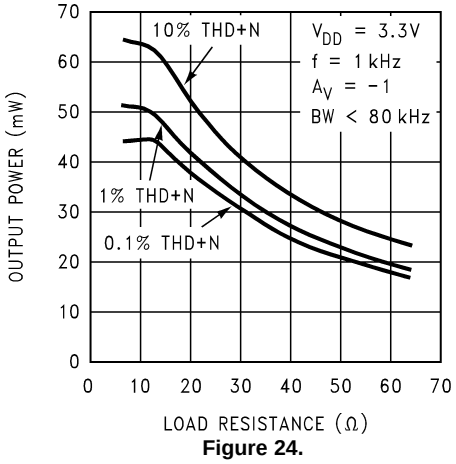



**Figure 24.**

**Output Power vs Load Resistance**

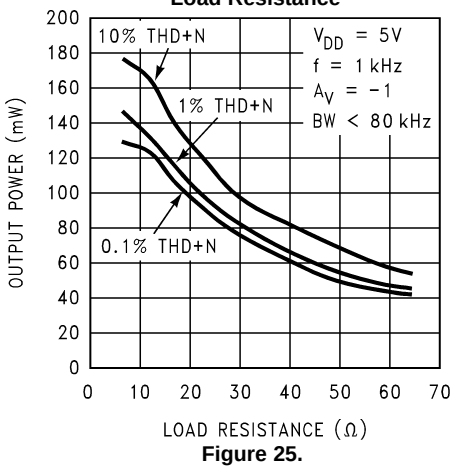



**Figure 25.**

**Output Power vs Supply Voltage**

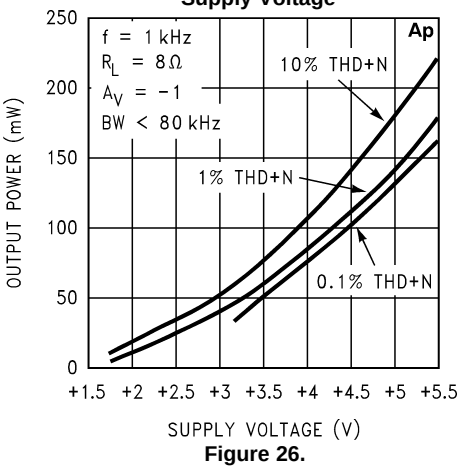



**Figure 26.**

**Output Power vs Power Supply**

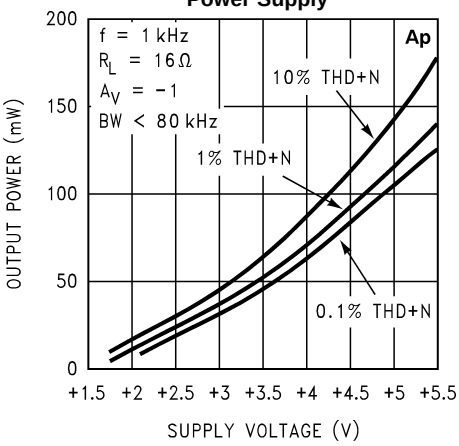



**Figure 27.**

**Output Power vs Power Supply**

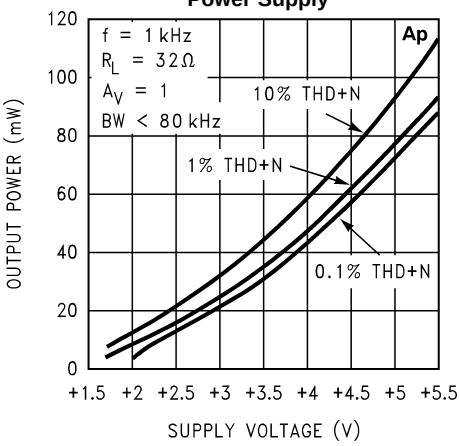



**Figure 28.**

## Typical Performance Characteristics (continued)

**Dropout Voltage vs Supply Voltage**

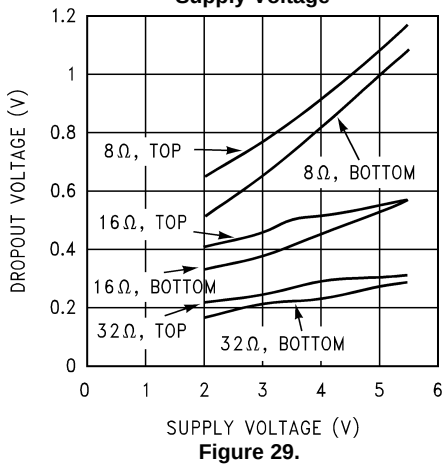



**Figure 29.**

**Power Dissipation vs Output Power**

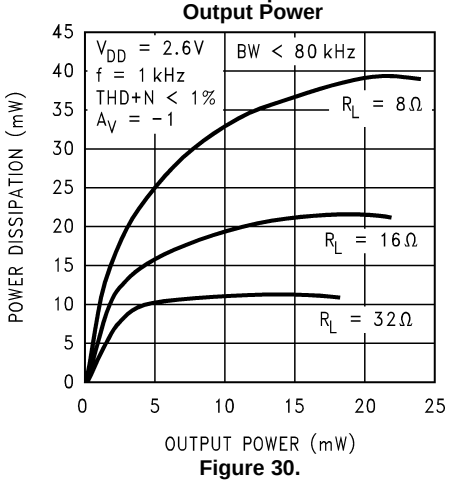



**Figure 30.**

**Power Dissipation vs Output Power**

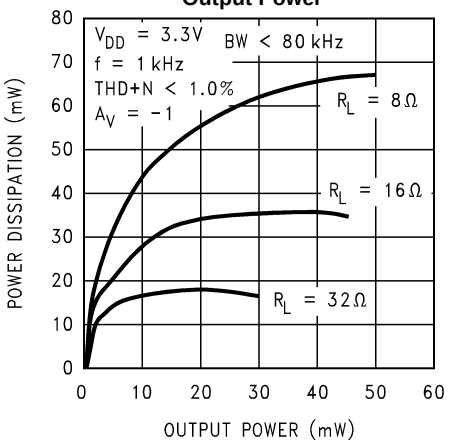



**Figure 31.**

**Power Dissipation vs Output Power**

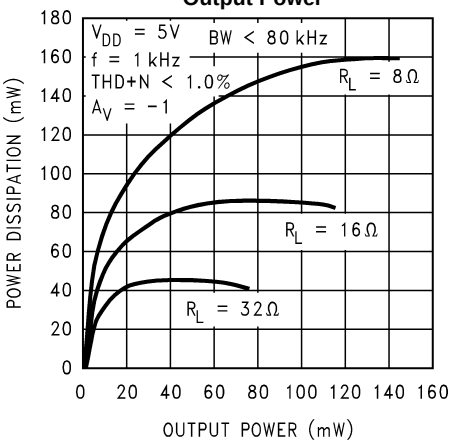



**Figure 32.**

**Channel Separation**

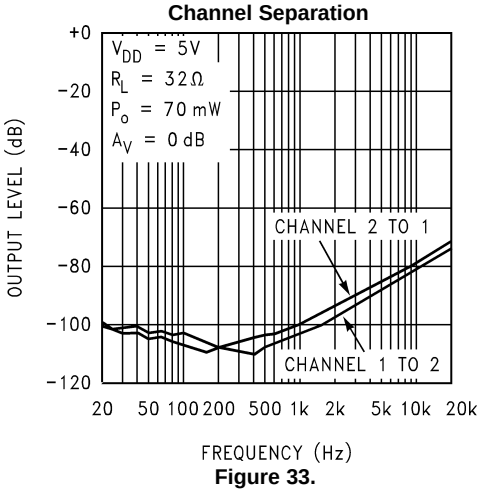



**Figure 33.**

**Channel Separation**

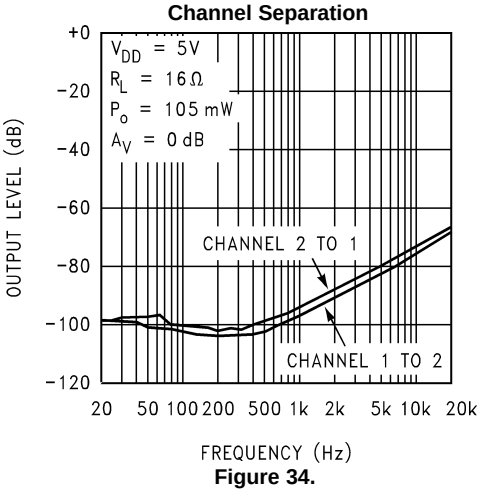



**Figure 34.**

## Typical Performance Characteristics (continued)

**Noise Floor**

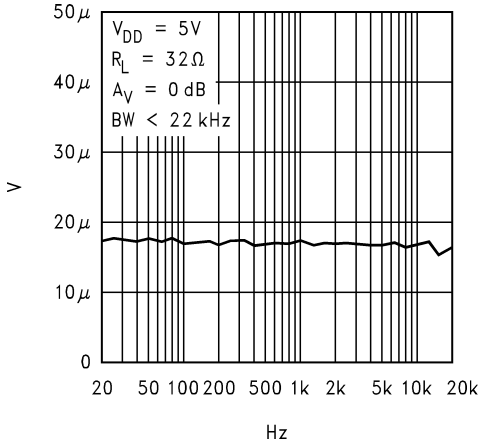



**Figure 35.**

**Power Supply Rejection Ratio**

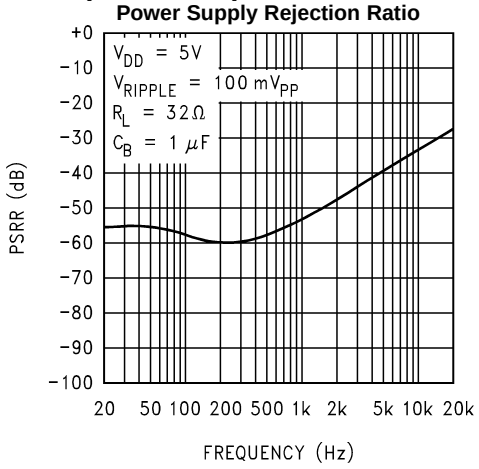



**Figure 36.**

**Power Supply Rejection Ratio**

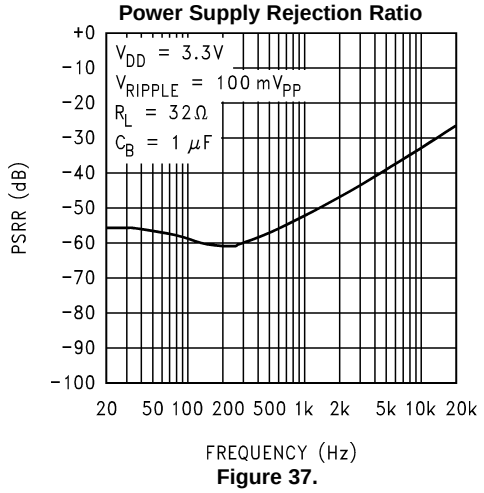



**Figure 37.**

**Power Supply Rejection Ratio**

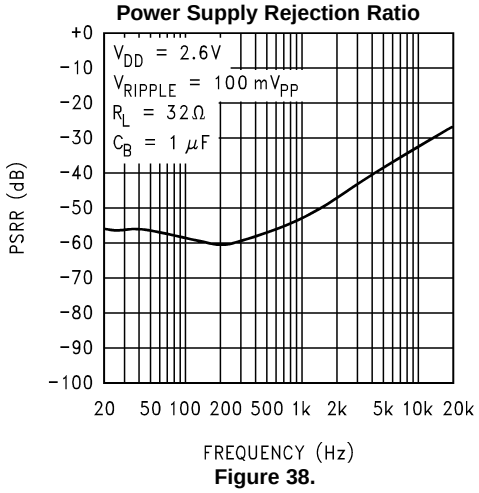



**Figure 38.**

**Frequency Response**

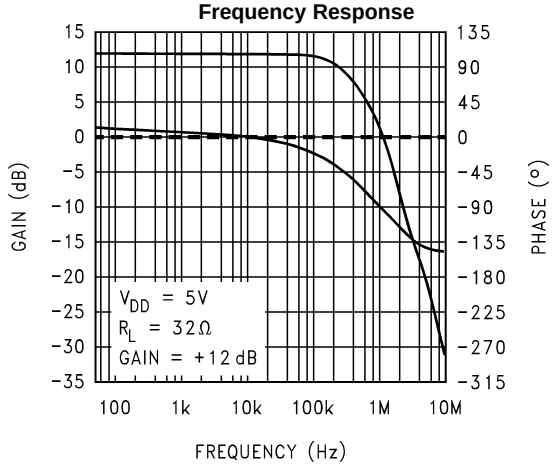



**Figure 39.**

**Supply Current vs Supply Voltage**

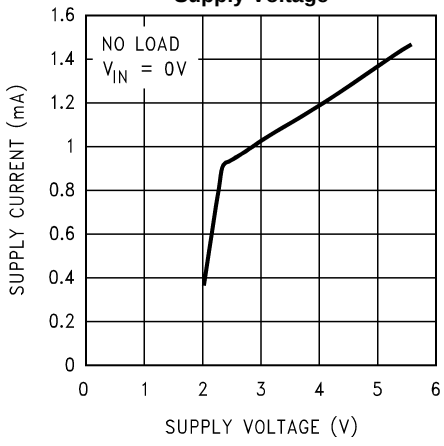



**Figure 40.**

## APPLICATION INFORMATION

### DIGITAL VOLUME CONTROL

The LM4811's gain is controlled by the signals applied to the CLOCK and UP/DN inputs. An external clock is required to drive the CLOCK pin. At each rising edge of the clock signal, the gain will either increase or decrease by a 3dB step depending on the logic voltage level applied to the UP/DN pin. A logic high voltage level applied to the UP/DN pin causes the gain to increase by 3dB at each rising edge of the clock signal. Conversely, a logic low voltage level applied to the UP/DN pin causes the gain to decrease 3dB at each rising edge of the clock signal. For both the CLOCK and UP/DN inputs, the trigger point is 1.4V minimum for a logic high level, and 0.4V maximum for a logic low level.

There are 16 discrete gain settings ranging from +12dB maximum to −33dB minimum. Upon device power on, the amplifier's gain is set to a default value of 0dB. However, when coming out of shutdown mode, the LM4811 will revert back to its previous gain setting.

The LM4811's CLOCK and UP/DN pins should be debounced in order to avoid unwanted state changes during transitions between $V_{IL}$ and $V_{IH}$. This will ensure correct operation of the digital volume control. A microcontroller or microprocessor output is recommended to drive the CLOCK and UP/DN pins.

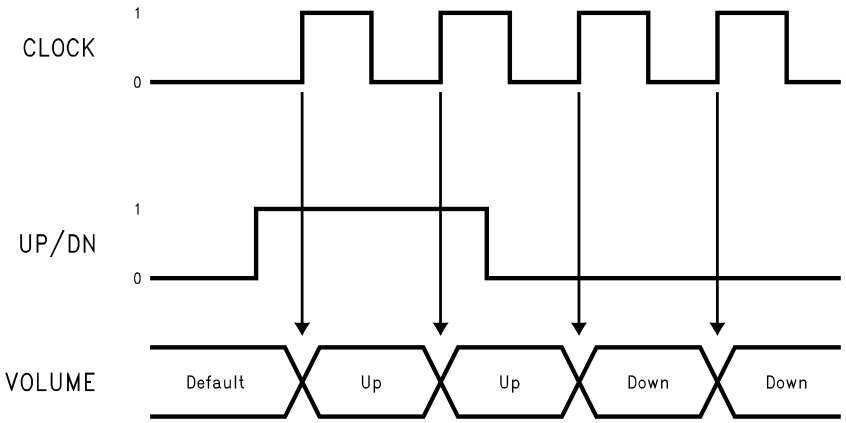



**Figure 41. Timing Diagram**

### POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4811 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. Even with the large internal power dissipation, the LM4811 does not require heat sinking over a large range of ambient temperature. From Equation 1, assuming a 5V power supply and a 32Ω load, the maximum power dissipation point is 40mW per amplifier. Thus the maximum package dissipation point is 80mW. The maximum power dissipation point obtained must not be greater than the power dissipation predicted by Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (2)$$

For the VSSOP package, $\theta_{JA}$ = 194°C/W, and for the WSON/SON package, $\theta_{JA}$ = 63°C/W. $T_{JMAX}$ = 150°C for the LM4811. For a given ambient temperature, $T_A$, of the system surroundings, Equation 1 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased, the load impedance increased, or $T_A$ reduced. For the VSSOP package in a typical application of a 5V power supply and a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 134.5°C. This assumes the device operates at maximum power dissipation and uses surface mount packaging. Internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, operation at higher ambient temperatures is possible. Refer to Typical Performance Characteristics for power dissipation information for lower output power levels.

## EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4811's exposed-dap (die attach paddle) package (WSON/SON) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The WSON/SON package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area.

However, since the LM4811 is designed for headphone applications, connecting a copper plane to the DAP's PCB copper pad is not required. Figure 32 in Typical Performance Characteristics shows that the maximum power dissipated is just 45mW per amplifier with a 5V power supply and a 32Ω load.

Further detailed and specific information concerning PCB layout, fabrication, and mounting an WSON/SON package is available from Texas Instruments' Package Engineering Group under application note AN1187.

## POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The value of the bypass capacitor directly affects the LM4811's half-supply voltage stability and PSRR. The stability and supply rejection increase as the bypass capacitor's value increases. Typical applications employ a 5V regulator with 10µF and a 0.1µF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4811. The selection of bypass capacitors, especially $C_B$, is thus dependent upon desired low frequency PSRR, click and pop performance, (explained in PROPER SELECTION OF EXTERNAL COMPONENTS), system cost, and size constraints.

## SHUTDOWN FUNCTION

In order to reduce power consumption while not is use, the LM4811 features amplifier bias circuitry shutdown. This shutdown function is activated by applying a logic high to the SHUTDOWN pin. The trigger point is 1.4V minimum for a logic high level, and 0.4V maximum for a logic low level. It is best to switch between ground and $V_{DD}$ to ensure optimal shutdown operation. By switching the SHUTDOWN pin to $V_{DD}$, the LM4811 supply current draw will be minimized in idle mode. Whereas the device will be disabled with shutdown voltages less than $V_{DD}$, the idle current may be greater than the typical value of 0.3µA. In either case, the SHUTDOWN pin should be tied to a fixed voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry. This provides a quick, smooth shutdown transition. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the SHUTDOWN pin is connected to ground and enables the amplifier. If the switch is open, the external pull-up resistor, $R_{PU}$, will disable the LM4811. This scheme ensures that the SHUTDOWN pin will not float, thus preventing unwanted state changes.

## PROPER SELECTION OF EXTERNAL COMPONENTS

Selection of external components when using integrated power amplifiers is critical for optimum device and system performance. While the LM4811 is tolerant of external component combinations, consideration must be given to the external component values that maximize overall system quality.

The LM4811's unity-gain stability allows a designer to maximize system performance. Low gain settings maximize signal-to-noise performance and minimizes THD+N. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to AUDIO POWER AMPLIFIER DESIGN for a more complete explanation of proper gain selection.

### Selection of Input and Output Capacitor Size

Besides gain, one of the major considerations is the closed loop bandwidth of the amplifier. To a large extent, the bandwidth is dicated by the choice of external components shown in Figure 4. Both the input coupling capacitor, $C_i$, and the output coupling capacitor, $C_o$, form first order high pass filters which limit low frequency response. These values should be based on the desired frequency response weighed against the following:

Large value input and output capacitors are both expensive and space consuming for portable designs. Clearly a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Thus large input and output capacitors may not increase system performance.

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, $C_i$. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 $V_{DD}$). This charge comes from the output via the feedback and is apt to create pops upon device enable. Turn on pops can be minimized by reducing $C_i$ value based on necessary low frequency response.

Besides minimizing the input and output capacitor values, careful consideration should be paid to the bypass capacitor value. Bypass capacitor $C_B$ is the most critical component to minimize turn on pops since it determines how fast the LM4811 turns on. The slower the LM4811's outputs ramp to their quiescent DC voltage (nominally 1/2 $V_{DD}$), the smaller the turn on pop. While the device will function properly, (no oscillations or motorboating), with $C_B$ equal to 1µF, the device will be much more susceptible to turn on clicks and pops. Thus, a value of $C_B$ equal to 1µF or larger is recommended in all but the most cost sensitive designs.

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance.

## AUDIO POWER AMPLIFIER DESIGN

### Design a Dual 70mW/32Ω Audio Amplifier

| Given: | |
|---|---|
| Power Output | 70mW |
| Load Impedance | 32Ω |
| Input Level | 1Vrms (max) |
| Input Impedance | 33kΩ (min) |
| Bandwidth | 100 Hz–20 kHz ± 0.50dB |

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from Figure 26 in Typical Performance Characteristics, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required $V_{OPEAK}$ using Equation 3 and add the dropout voltage. For a single-ended application, the minimum supply voltage can be approximated by ($2V_{OPEAK}$ + ($V_{ODTOP}$ + $V_{ODBOT}$)), where $V_{ODBOT}$ and $V_{ODTOP}$ are extrapolated from Figure 29 in Typical Performance Characteristics.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (3)$$

Using Figure 28 for a 32Ω load, the minimum supply rail is 4.8V. Since 5V is a standard supply voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4811 to reproduce peaks in excess of 70mW without clipping the signal. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in POWER DISSIPATION. Remember that the maximum power dissipation point from Equation 1 must be multiplied by two since there are two independent amplifiers inside the package.

The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response assuming a single pole roll-off. As stated in External Components Description, $C_i$ and $C_o$ create first order highpass filters. Thus to obtain the desired frequency low response of 100Hz within ±0.5dB, both poles must be taken into consideration. The combination of two single order filters at the same frequency forms a second order response. This results in a signal which is down 0.34dB at five times away from the single order filter −3dB point. Thus, a frequency of 20Hz is used in the following equations to ensure that the response is better than 0.5dB down at 100Hz.

$$C_i \geq 1 / (2\pi * 33\ k\Omega * 20\ Hz) = 0.241\mu F; \text{ use } 0.39\mu F. \quad (4)$$

$$C_o \geq 1 / (2\pi * 32\Omega * 20\ Hz) = 249\mu F; \text{ use } 330\mu F. \quad (5)$$

The high frequency pole is determined by the product of the desired high frequency pole, $f_H$, and the closed-loop gain, $A_V$. With a closed-loop gain of 3.98 or +12dB and $f_H$ = 100kHz, the resulting GBWP = 398kHz which is much smaller than the LM4811 GBWP of 1MHz. This figure displays that at the maximum gain setting of 3.98 or +12dB, the LM4811 can be used without running into bandwidth limitations.

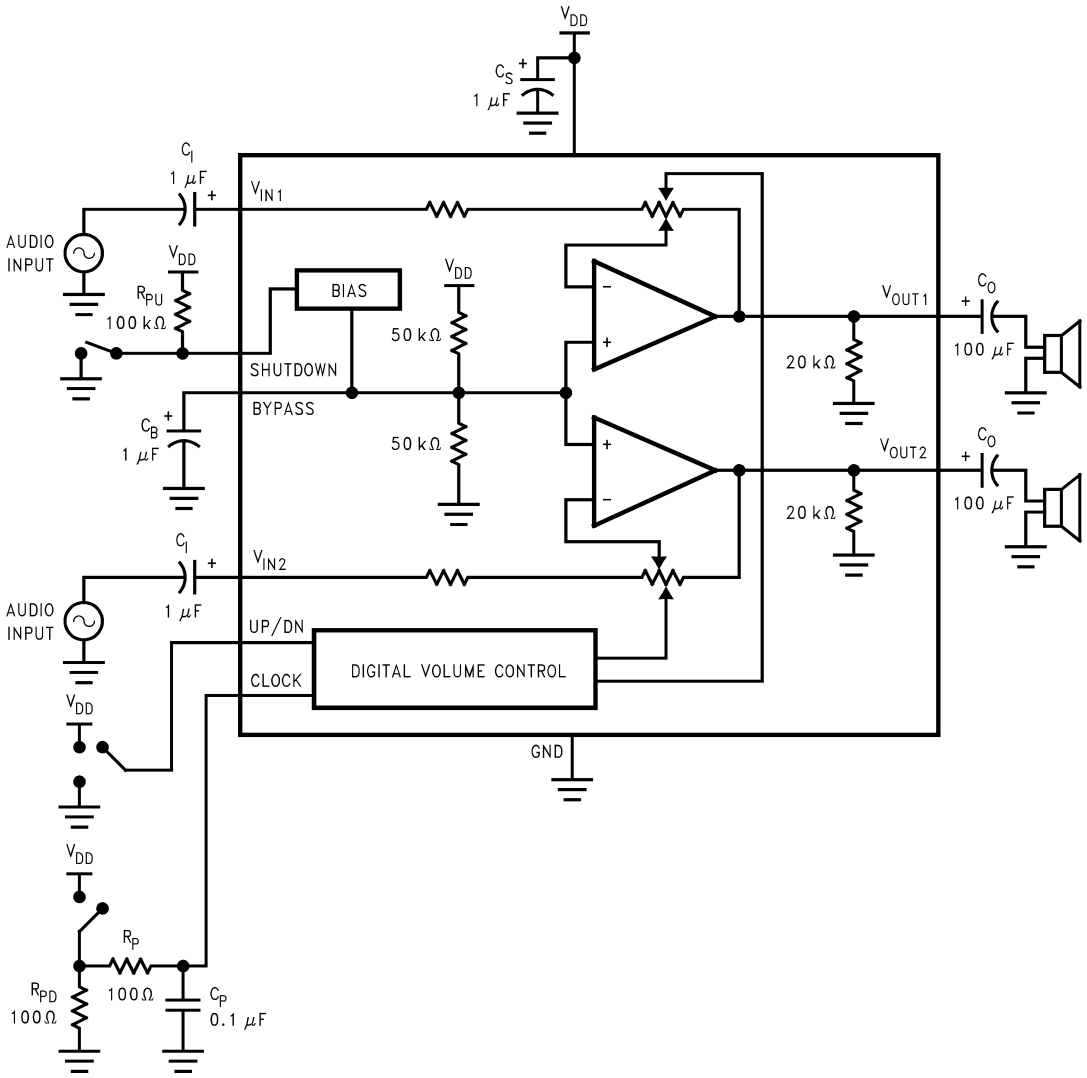



**Figure 42. Demo Board Schematic**

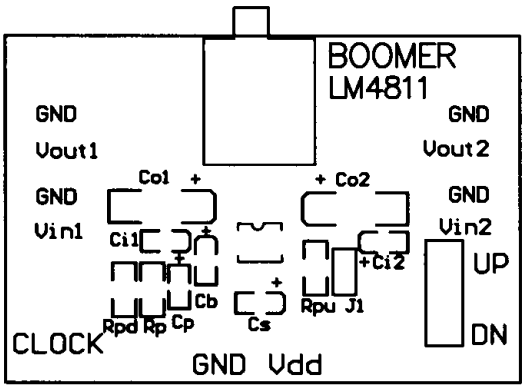



**Figure 43. Recommended VSSOP PC Board Layout: TOP Silk Screen**

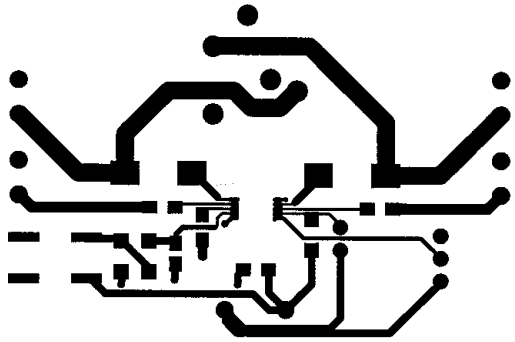


**Figure 44. Recommended VSSOP PC Board Layout: TOP Top Layer**

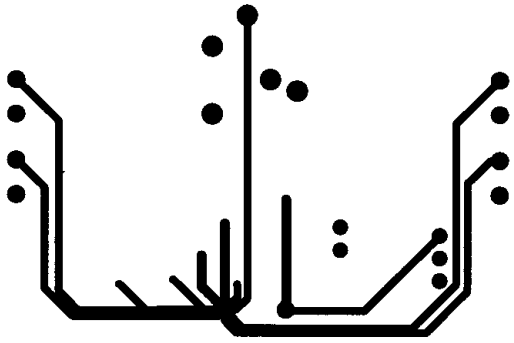


**Figure 45. Recommended VSSOP PC Board Layout: Bottom Layer**

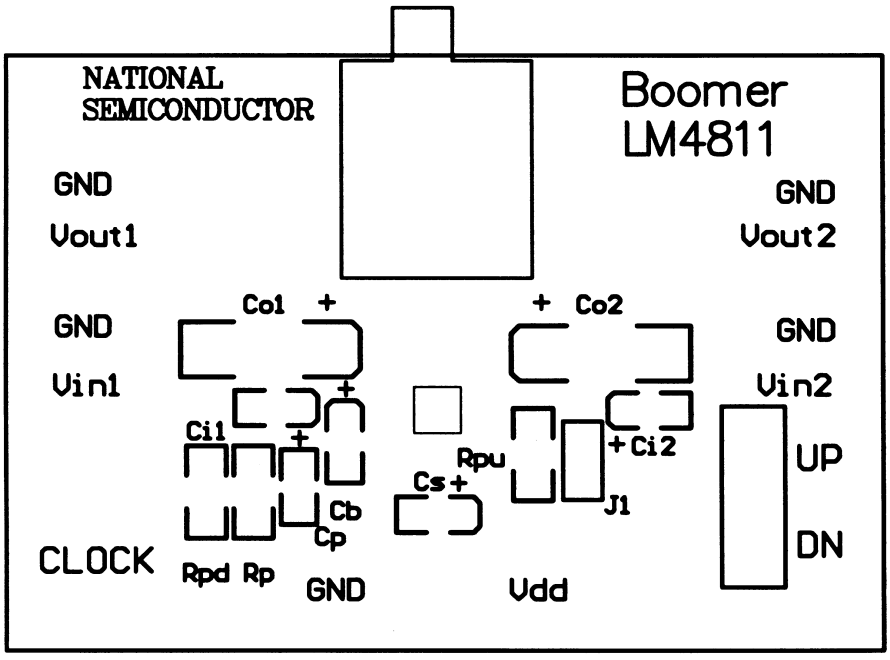



**Figure 46. Recommended WSON/SON PC Board Layout: TOP Silk Screen**

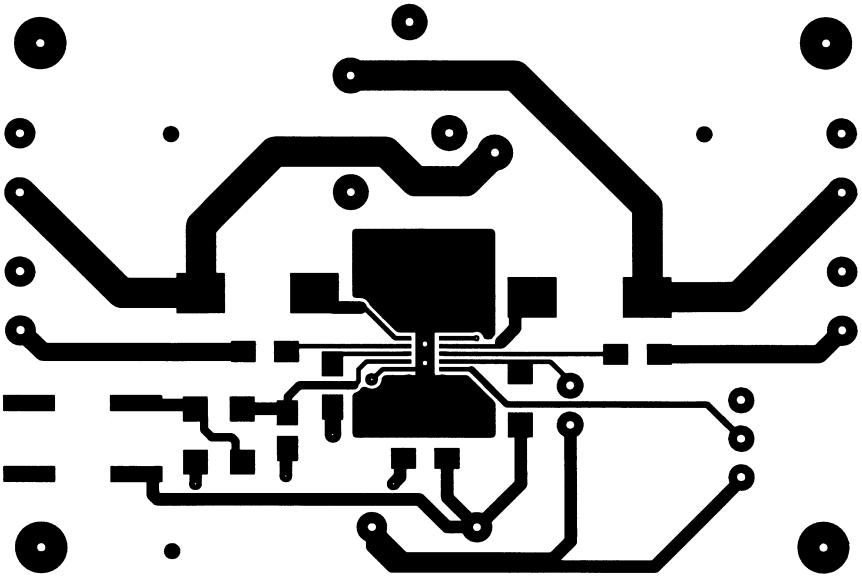


**Figure 47. Recommended WSON/SON PC Board Layout: TOP Top Layer**

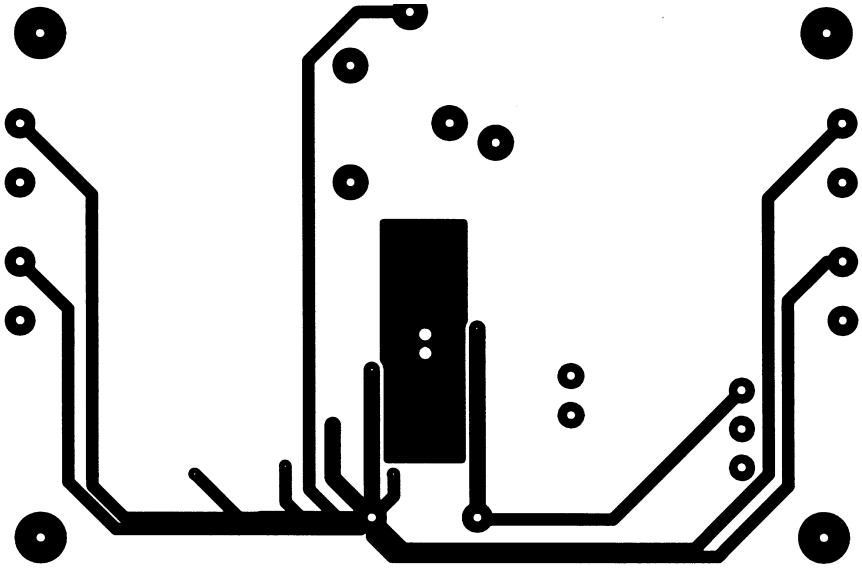


**Figure 48. Recommended WSON/SON PC Board Layout: Bottom Layer**

## REVISION HISTORY

| Rev | Date | Description |
|---|---|---|
| 0.1 | 04/06/06 | Added NHD0010A Package and markings, then re-released D/S to the WEB (per Alvin F.). |
| D | 04/05/13 | Changed layout of National Data Sheet to TI format. |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM4811MM/NOPB | ACTIVE | VSSOP | DGS | 10 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | G11 | Samples |
| LM4811MMX/NOPB | ACTIVE | VSSOP | DGS | 10 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | G11 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

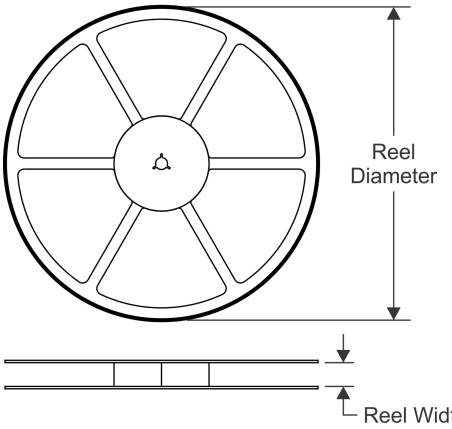
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

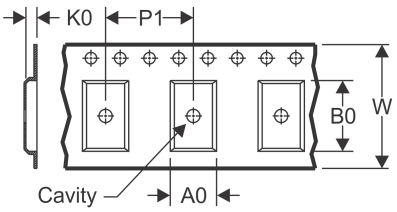
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

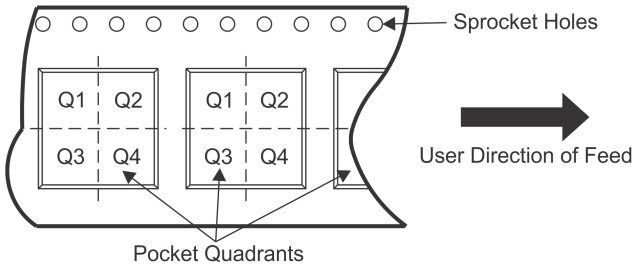



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

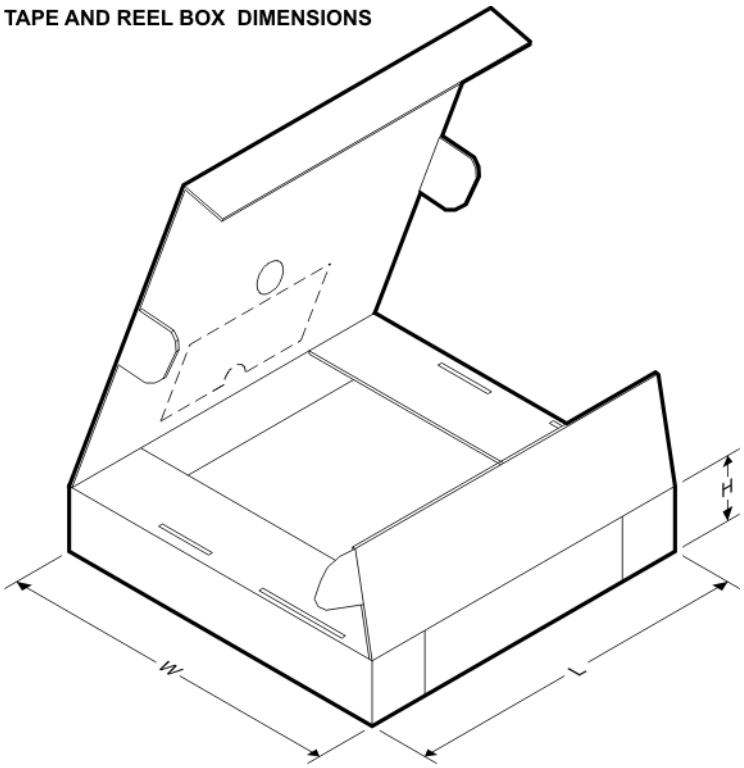
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM4811MM/NOPB | VSSOP | DGS | 10 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM4811MMX/NOPB | VSSOP | DGS | 10 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

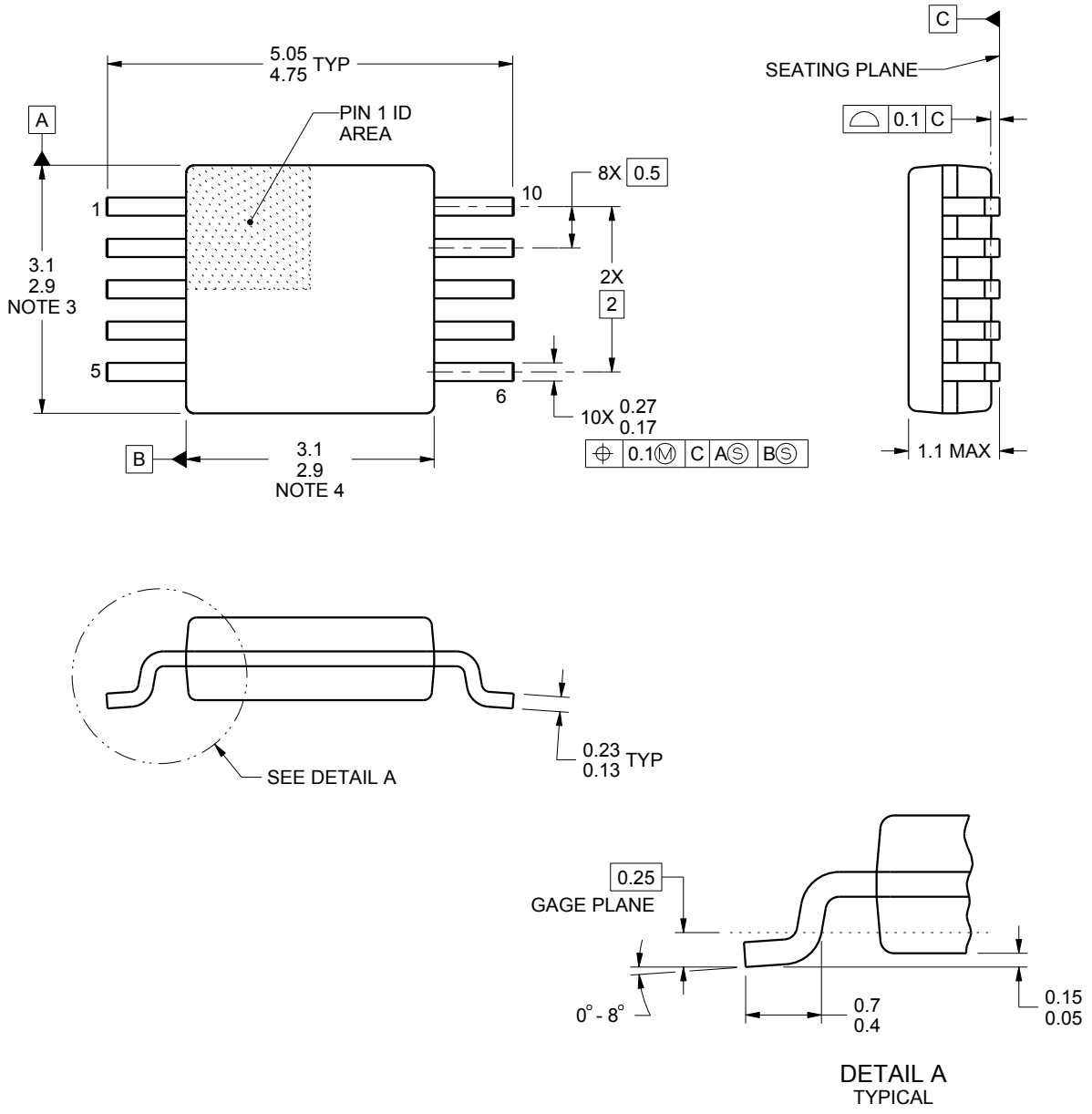
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM4811MM/NOPB | VSSOP | DGS | 10 | 1000 | 210.0 | 185.0 | 35.0 |
| LM4811MMX/NOPB | VSSOP | DGS | 10 | 3500 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## DGS0010A

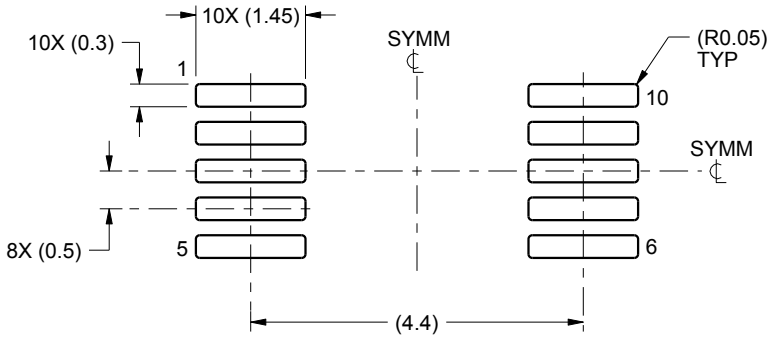
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

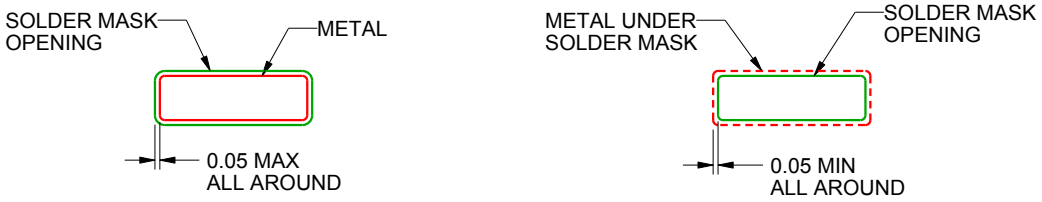



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
NOT TO SCALE

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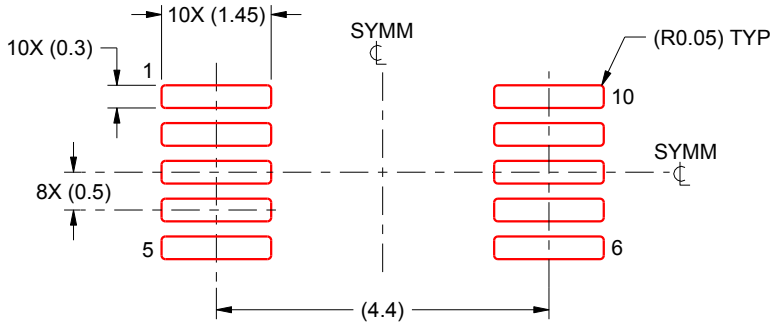
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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