

Main Pinball controller for Fan-Tas-Tic		
* TI TIVA C brain		
* 4 Solenoid drivers with PWM control		
* 8 Solenoid drivers (On / Off only)		
* 8 x 8 Switch Matrix		
* 4 x I2C Bus for extension		
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File: fan_tas_tic.sch		
Title:		
Size: A3	Date:	Rev:
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Warning, configure PB0 and PB1 as open drain output with external pullup

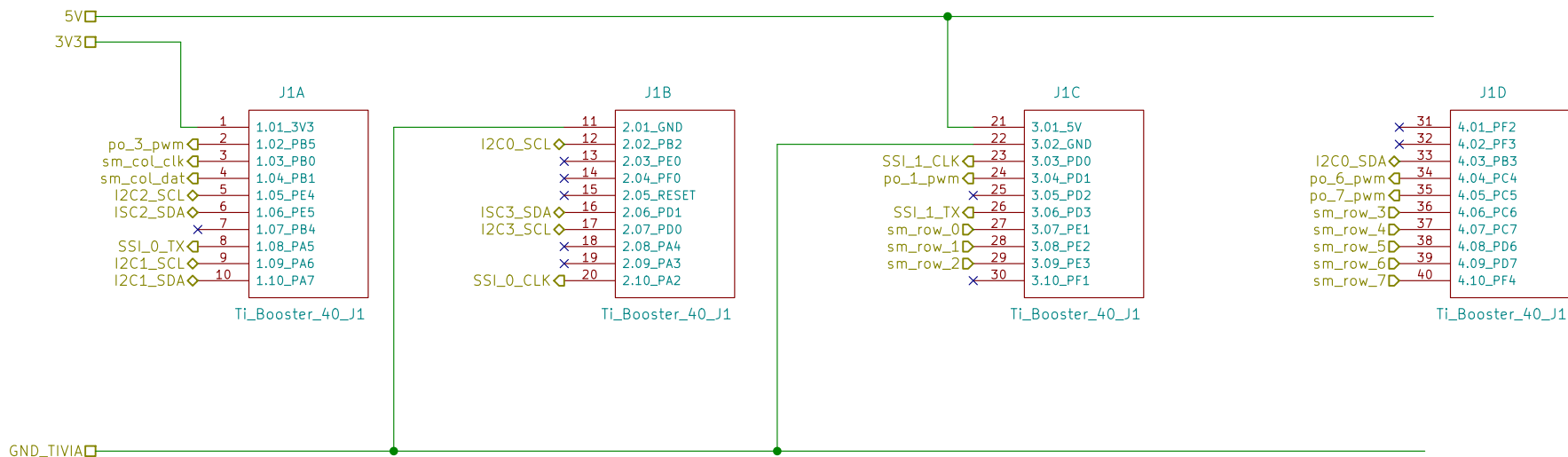


Table 2-3. J1 Connector⁽¹⁾

J1 Pin	GPIO	Analog Function GPIO AMSEL	On-Board Function	Tiva C Series MCU Pin	GPIOCTL Register Setting									
					1	2	3	4	5	6	7	8	9	10
1.01					3.3 V									
1.02	PB5	AN11	57	SSOPIN										
1.03	PB0	US0B0	40	UTIN										
1.04	PB1	US0B0VUS	46	UTIN										
1.05	PB1	AN0	58	US0B0										
1.06	PE4	AN6	60	US0B0										
1.07	PB4	AN10	58	SSOPIN										
1.08	PA5	AN10	58	SSOPIN										
1.09	PA6	AN10	58	SSOPIN										
1.10	PA7	AN10	58	SSOPIN										

⁽¹⁾ Shaded cells indicate configuration for compatibility with the MSP430 LaunchPad.

Table 2-5. J3 Connector⁽¹⁾

J3 Pin	GPIO	Analog Function GPIO AMSEL	On-board Function	Tiva C Series MCU Pin	GPIOCTL Register Setting									
					1	2	3	4	5	6	7	8	9	10
GND														
3.01	ANT	1	SSOPIN	SSOPIN										
3.02	PB0	AN12	57	SSOPIN										
3.03	PB1	AN12	57	SSOPIN										
3.04	AN6	60	SSOPIN	SSOPIN										
3.05	PB7	AN10	58	SSOPIN										
3.06	PB2	AN10	58	SSOPIN										
3.07	PE1	AN10	58	SSOPIN										
3.08	PE2	AN10	58	SSOPIN										
3.09	PE3	AN10	58	SSOPIN										
3.10	PFI1	AN10	58	SSOPIN										

⁽¹⁾ Shaded cells indicate configuration for compatibility with the MSP430 LaunchPad.

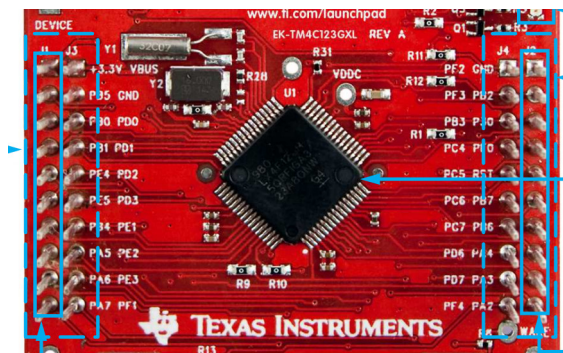
Table 2-4. J2 Connector⁽¹⁾

J2 Pin	GPIO	Analog Function GPIO AMSEL	On-board Function	Tiva C Series MCU Pin	GPIOCTL Register Setting										
					1	2	3	4	5	6	7	8	9	14	15
2.01					GND										
2.02	PB2	—	47	—	SSOPIN	—	—	—	—	—	—	—	TACCP0	—	—
2.03	PB0	AN10	58	UTIN	—	—	—	—	—	—	—	—	—	—	—
2.04	PB1	—	36	UHTS	SSOIN	CANIN	—	—	MPWMAI	PA5IO	TACCP0	NMI	On	—	—
2.05					RESET										
2.06	PB1	AN10	Connected to GPIO Compatibility (W)	62	SSOIN	SSOIN	—	MPWMAI	—	MPWMAI	—	—	TACCP0	—	—
	PB1	AN10	Connected to GPIO Compatibility (W)	62	SSOIN	SSOIN	OC3B0A	MPWMAI	MPWMAI	—	—	—	WTACCP0	—	—
2.07	PB1	—	—	—	SSOIN	—	—	MPWMAI	—	—	—	—	TACCP0	—	—
	PB0	AN10	Connected to GPIO Compatibility (W)	61	SSOIN	SSOIN	OC3SEL	MPWMAI	MPWMAI	—	—	—	WTACCP0	—	—
2.08	PA5	—	23	—	SSOIN	—	—	—	—	—	—	—	—	—	—
2.09	PA3	—	20	—	SSOIN	—	—	—	—	—	—	—	—	—	—
2.10	PA2	—	19	—	SSOIN	—	—	—	—	—	—	—	—	—	—

⁽¹⁾ Shaded cells indicate configuration for compatibility with the MSP430 LaunchPad.

Table 2-6. J4 Connector

J4 Pin	GPIO	Analog Function GPIO AMSEL	On-board Function	Tiva C Series MCU Pin	GPIOCTL Register Setting									
					1	2	3	4	5	6	7	8	9	10
4.01	PFI2	Blue LED (R13)	30	SSOPIN										
4.02	PFI3	Green LED (R13)	31	SSOPIN										
4.03	PB3	AN10	58	SSOPIN										
4.04	PC4	AN10	58	SSOPIN										
4.05	PC5	AN10	58	SSOPIN										
4.06	PC6	AN10	58	SSOPIN										
4.07	PC7	AN10	58	SSOPIN										
4.08	PC8	AN10	58	SSOPIN										
4.09	PC9	AN10	58	SSOPIN										
4.10	PFI4	AN10	58	SSOPIN										

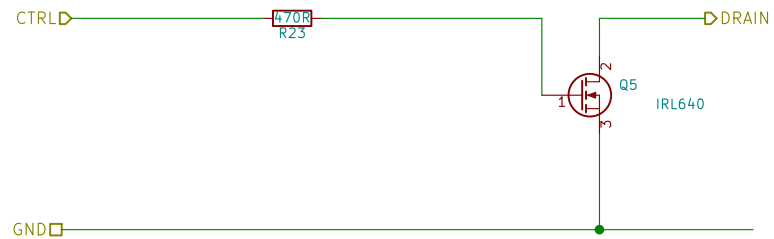


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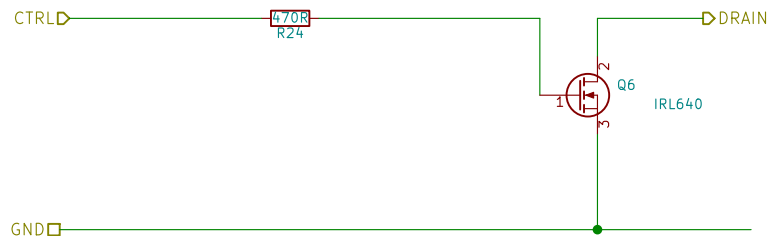
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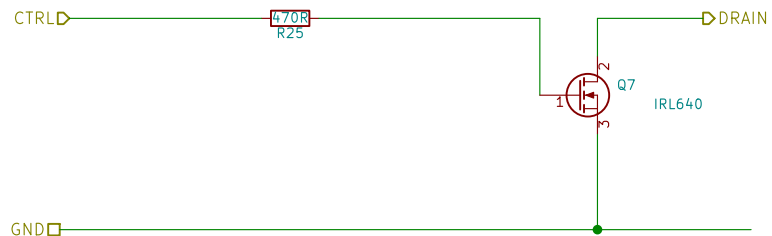
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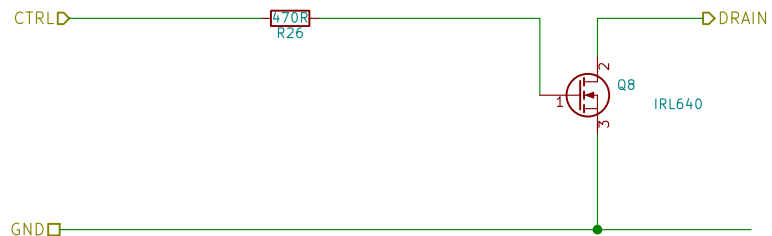
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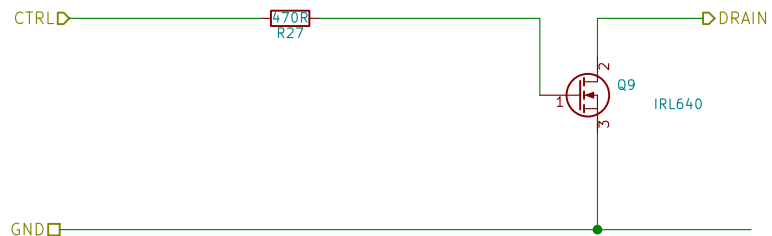
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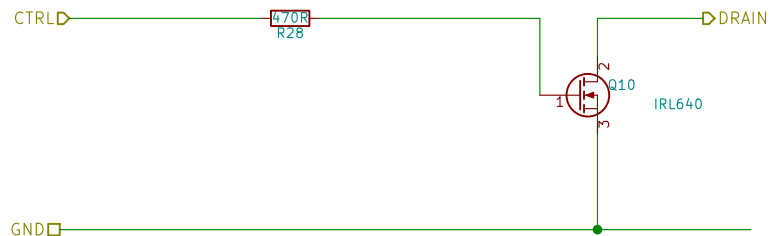
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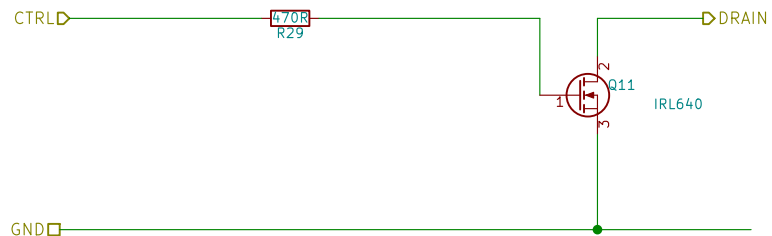
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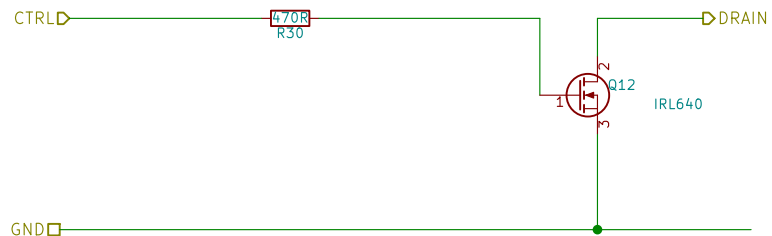
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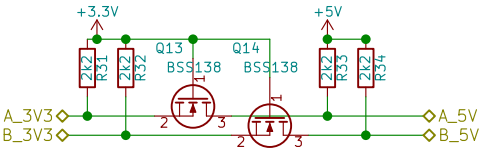
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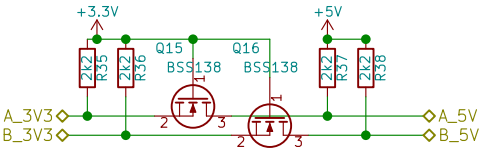
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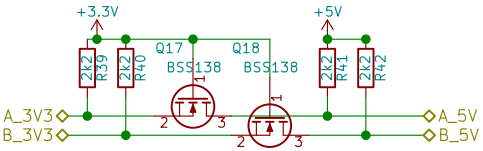
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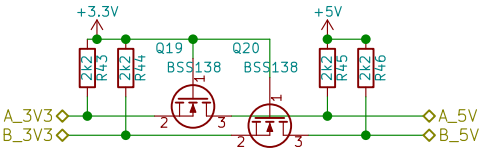
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