1 Student Statement

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I wrote the RAM Control Block module. I used the pix_word_cache module prebuilt, but had to redesign the RAM FSM to enable RAM timings. I also wrote two functions into the project pack to tidy up the code for readability, and made some very minor modifications to DB, which was simply to correct Synplify warnings and add some aliases, again for readability.

I attempted to optimise the module by performing cache write operations to RAM in parallel with draw/clear operations.

I created the ModelSim projects and accompanying .do files, and also created the initial Synplify project files. I tested my module against behavioural and against my partner's module using both the initial test set and the final test sets written by us.

I'm happy that the work was split evenly at 50%, because my partner and I worked very closely together throughout the project, on both the initial modules and all of the accompanying testing, design planning, and debugging.