# 1 Student Statement

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I wrote the Draw Block module, using the draw_any_octant module prebuilt. I designed the module by carefully planning a state machine to exactly meet the specifications, before writing the module itself. I later corrected Synplify warnings, such as latches and lack of variables in sensitivity lists, again in Draw Block.

I performed the final synthesis and post-synthesis tests. I also wrote all of our custom tests, and performed all of the tests on the pre-synthesis and post-synthesis modules. I completed the write-up for the test sets, describing their purpose and the hardware coverage of each, and I performed all the tests on the behavioural module to copy the correct output.

I think the work was even between the two of us, so I did 50% of the work.