ECE/CS 250 Midterm Exam #2, Spring 2016

Name: _____

Duke students are bound by an academic integrity standard:

1. I will not lie, cheat, or steal in my academic endeavors, nor will I accept the actions of those who do.

2. I will conduct myself responsibly and honorably in all my activities as a Duke student.

Please sign your name below to acknowledge that you follow this standard:

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1) [5 points] Write the truth table for the output of the following Boolean expression that has 4 inputs (a, b, c, d). Please keep the truth table rows in the standard order.

$$\boldsymbol{output = c(ab + ad) + \overline{d(a + bc)}}$$

2) [5 points] Convert the following truth table into a Boolean expression in sum-of-products format. Note that there are 3 inputs (a,b,c) and one output. Do NOT simplify or optimize in any way.

a	b	c	Output
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

3) [15 points] You have a 4-bit integer adder with 4-bit inputs x ($x_3x_2x_1x_0$) and y ($y_3y_2y_1y_0$). The carry-in to the least significant bit position (bit position 0) is always zero. Write the equation for the carry-in into bit position 2 (which is the same as the carry-out from bit position 1) as a Boolean function of the bits of x and y. Logic minimization is not necessary.

4) You must make a finite state machine with no inputs (other than the clock) and a 1-bit output. The output should be 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, etc. (output is a repeated pattern of four 0s and one 1).

[10 points] Draw the state transition diagram for the FSM.

5) [10 points] Write the truth table for the FSM in the previous question.

6) [10 points – each question is worth 1 point] Circle the correct answer. Unclear circles will be marked as incorrect.

a) **An exception is an instruction in the ISA.**

TRUE FALSE

b) **In a 32-bit machine with word-aligned instructions, the least significant bits of the PC must be 11_2.**

TRUE FALSE

c) **In a 32-bit architecture, each memory address is 32 bits long.**

TRUE FALSE

d) **A load instruction (like MIPS's lw) writes to the register file.**

TRUE FALSE

e) **In a core that executes one instruction per clock cycle, the clock frequency is determined by the instruction that can be done in the least amount of time.**

TRUE FALSE

f) **In a 64-bit architecture, addresses are represented using 2s complement.**

TRUE FALSE

g) **A load instruction accesses the memory hierarchy twice.**

TRUE FALSE

h) **Some instructions in an ISA can only be executed by the operating system.**

TRUE FALSE

i) **In a 64-bit architecture, there are 64 registers in the processor core.**

TRUE FALSE

j) **A processor's datapath includes the ALU.**

TRUE FALSE