LC29T (AA)
Hardware Design

GNSS Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service, or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety precautions by incorporating them into all product manuals. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Ensure that the product may be used in the country and the required environment, as well as that it conforms to the local safety and environmental regulations.
	Keep away from explosive and flammable materials. The use of electronic products in extreme power supply conditions and locations with potentially explosive atmospheres may cause fire and explosion accidents.
	The product must be powered by a stable voltage source, and the wiring shall conform to security precautions and fire prevention regulations.
	Proper ESD handling procedures must be followed throughout the mounting, handling and operation of any devices and equipment that incorporate the module to avoid ESD damages.

About the Document

Document Information	
Title	**LC29T (AA) Hardware Design**
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Revision History

Version	Date	Description
-	2022-06-25	Creation of the document
1.0	2023-10-18	First official release
1.1	2024-04-16	1. Deleted the I2C interface and reserved pins 18 and 19 (*Chapters 1.1*, *1.2*, *1.4*, *2* and *4.1.1*). 2. Updated the warm start of TTFF (with AGNSS) (*Table 3*). 3. Added the typical value and updated the minimum value of TXD high-level output voltage (*Table 6* and *Table 12*). 4. Moved the C/N_0 information in Antenna Selection Guide and Coexistence with Cellular Systems to Quectel_GNSS_Antenna_Application_Note.
1.2	2024-08-22	1. Updated the tolerances of module's length and width (*Table 2* and *Figure 19*). 2. Updated the horizontal position accuracy (*Table 3*). 3. Deleted the phase center offset and phase center variation and added the out-of-band rejection (*Table 9*). 4. Updated the R3 resistance of active antenna reference design with status detection (*Figure 17*). 5. Added the notes specifying that mercury-containing materials and corrosive gases should be avoided for module processing (*Chapter 8.3*).

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1 Product Description

1.1. Overview

The Quectel LC29T (AA) module supports multiple global positioning and navigation systems: GPS, GLONASS, Galileo, BDS and QZSS. The module also supports SBAS (including WAAS, EGNOS, MSAS and GAGAN) and AGNSS function.

Key features:

- High precision timing, single-band and multi-constellation GNSS module featuring a high-performance, high reliability positioning engine, which facilitates fast and precise GNSS positioning.
- Serial communication interface: UART.
- Supports 10 MHz frequency output.
- Embedded flash memory provides the capacity for storing user-specific configurations and future firmware updates.

The Quectel LC29T (AA) module is an SMD module type with a compact form factor of 12.2 mm × 16.0 mm × 3.1 mm. It can be embedded in your applications through 24 LCC pins.

The module is fully compliant with the EU RoHS Directive.

1.1.1. Special Mark

Table 1: Special Mark

Mark	Definition
●	The symbol indicates that a function or technology is supported by the module(s).

1.2. Features

Table 2: Product Features

Features		LC29T (AA)
Grade	Industrial	●
	Automotive	-
Category	Standard Precision GNSS	●
	High Precision GNSS	-
	DR	-
	RTK	-
	Timing	●
	10 MHz Frequency Output	●
VCC Voltage	3.0–3.6 V, Typ. 3.3 V	●
V_BCKP Voltage	2.1–3.6 V, Typ. 3.3 V	●
I/O Voltage	Following VCC	●
Communication Interfaces	UART	●
	I2C	-
	SPI	-
	CAN	-
	USB	-
Integrated Features	Additional LNA	-
	Additional Filter	●
	RTC Crystal	●
	TCXO Oscillator	●
	6-axis IMU	-
Constellations and	Number of Concurrent GNSS	4 + QZSS

Features			LC29T (AA)
Frequency Bands	GPS	L1 C/A	●
		L5	-
		L2C	-
	GLONASS	L1	●
		L2	-
	Galileo	E1	●
		E5a	-
		E5b	-
	BDS	B1I	●
		B1C	-
		B2a	-
		B2I	-
	QZSS	L1 C/A	●
		L5	-
		L2C	-
	NavIC	L5	-
SBAS		L1	●
Temperature Range	Operating Temperature Range: -40 °C to +85 °C Storage Temperature Range: -40 °C to +90 °C		
Physical Characteristics	Size: (12.2 +0.30/-0.15) mm × (16.0 +0.30/-0.15) mm × (3.1 ±0.20) mm Weight: Approx. 1.1 g		

NOTE

For more information about GNSS constellation configuration, see *document [1] protocol specification*.

1.3. Performance

Table 3: Product Performance

Parameter	Specification	LC29T (AA)
Power Consumption [1] (GPS + GLONASS + Galileo + BDS + QZSS)	Acquisition	222 mA (732.6 mW)
	Tracking	232 mA (765.6 mW)
	Backup Mode	55 μA (181.5 μW)
Sensitivity [2] (GPS + GLONASS + Galileo + BDS + QZSS)	Acquisition	-145 dBm
	Reacquisition	-153 dBm
	Tracking	-161 dBm
TTFF [1] (without AGNSS)	Cold Start	35 s
	Warm Start	24 s
	Hot Start	2 s
TTFF [3] (with AGNSS)	Warm Start	5 s
Horizontal Position Accuracy [4]	Autonomous	1.5 m
Update Rate	1 Hz (Max. 10 Hz)	
1PPS Timing Accuracy [1]	< 13.6 (± 6.8) ns @1σ	
1PPS Jitter [1]	±6.5 ns	
Frequency Reference [3]	10 MHz ±0.05ppm	
Velocity Accuracy [1]	Without Aid: 0.1 m/s	
Acceleration Accuracy [1]	Without Aid: 0.1 m/s²	
Dynamic Performance [1]	Maximum Altitude: 18000 m	
	Maximum Velocity: 515 m/s	
	Maximum Acceleration: 4g	

[1] Default constellation, room temperature, all satellites at -130 dBm.
[2] Test with two external LNAs with 16.5 dB gain and 0.85 dB noise figure.
[3] Open-sky, active high precision GNSS antenna.
[4] CEP, 50 %, 24 hours static, -130 dBm, more than 6 SVs.

1.4. Block Diagram

A block diagram of the module includes a front-end section consisting of an additional SAW filter, a GNSS engine section consisting of a GNSS IC with an internal PMU and application Flash memory.

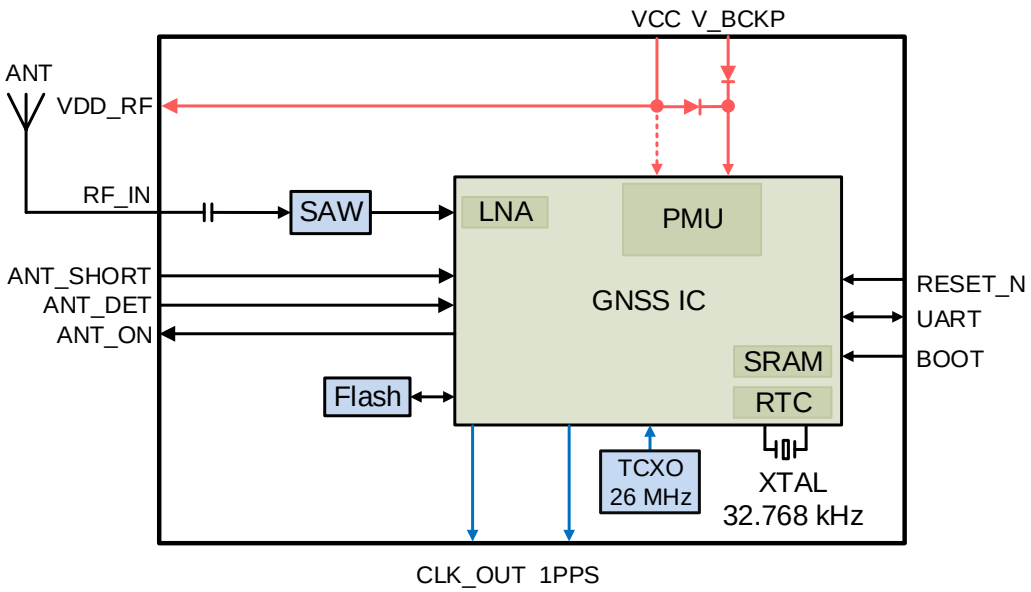


Figure 1: Block Diagram

1.5. GNSS Constellations and Frequency Bands

The module is a single-band concurrent GNSS receiver that can receive and track multiple GNSS systems. Owing to its RF front-end architecture, it can track the following GNSS constellations: GPS, GLONASS, Galileo, BDS, and QZSS, plus SBAS satellites. If low power consumption is a key factor, then the module can be configured for a subset of GNSS constellations.

QZSS is a regional navigation satellite system that transmits signals compatible with the GPS L1 C/A, L1C, L2C and L5 signals for the Pacific region covering Japan and Australia. The module can detect and track QZSS L1 C/A signal concurrently with GPS signals, leading to better availability especially under challenging conditions, e.g., in urban canyons.

Table 4: GNSS Constellations and Frequency Bands

System	Signals
GPS	L1 C/A: 1575.42 MHz
GLONASS	L1: 1602 MHz + K × 562.5 kHz, K= (-7 to +6, integer)
Galileo	E1: 1575.42 MHz
BDS	B1I: 1561.098 MHz
QZSS	L1 C/A: 1575.42 MHz

1.6. Augmentation System

1.6.1. SBAS

The module supports SBAS signal reception. By augmenting primary GNSS constellations with additional satellite-broadcast messages, the system improves the accuracy and reliability of GNSS information by correcting signal measurement errors and providing information about signal accuracy, integrity, continuity, and availability. SBAS transmits signals for ranging or distance measurement, thus further improving availability. Supported SBAS systems: WAAS, EGNOS, MSAS, and GAGAN.

1.7. AGNSS

The module supports the AGNSS feature that significantly reduces the module's TTFF, especially under lower signal conditions. To implement the AGNSS feature, the module should get the assistance data including the current time and rough position.

1.8. Firmware Upgrade

The module is delivered with preprogrammed firmware. Quectel may release firmware versions that contain bug fixes or performance optimizations. It's highly important that you implement a firmware upgrade mechanism in your system. A firmware upgrade is a process of transferring a binary file image to the receiver and storing it in non-volatile flash. For more information, see *document [2] firmware upgrade guide*.

2 Pin Assignment

The module is equipped with 24 LCC pins by which the module can be mounted on your PCB.

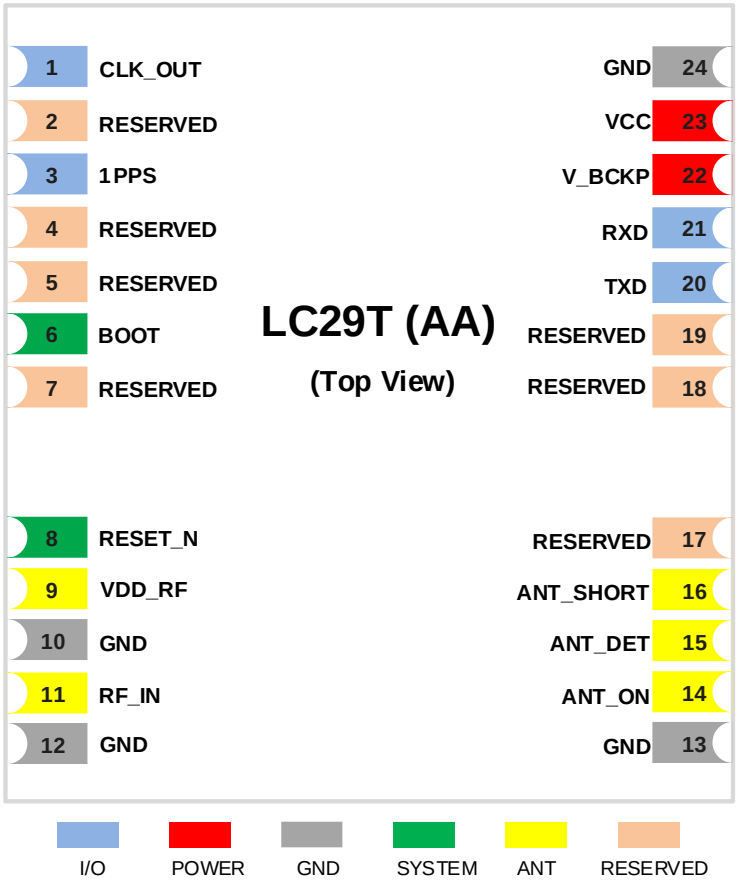


Figure 2: Pin Assignment

Table 5: I/O Parameter Definition

Type	Description
AI	Analog Input
DI	Digital Input
DO	Digital Output

Type	Description
PI	Power Input
PO	Power Output

Table 6: Pin Description

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
Power	VCC	23	PI	Main power supply	$V_I$min = 3.0 V $V_I$max = 3.6 V $V_I$nom= 3.3 V	Requires clean and steady voltage.
	V_BCKP	22	PI	Backup power supply for backup domain	$V_I$min = 2.1 V $V_I$max = 3.6 V $V_I$nom= 3.3 V	V_BCKP must be connected to supply power for startup, and it should always be powered if hot (warm) start is needed.
I/O	TXD	20	DO	Transmits data	V_{OL}max = 0.4 V V_{OH}min = VCC - 0.7 V V_{OH}nom = 2.8 V	UART interface supports standard NMEA message, PSTM message and firmware upgrade.
	RXD	21	DI	Receives data	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V	
	CLK_OUT	1	DO	Time pulse signal	V_{OH}min = VCC - 0.4 V V_{OL}max = 0.4 V	Clock source output.
	1PPS	3	DO	One pulse per second	V_{OH}min = VCC - 0.4 V V_{OL}max = 0.4 V	Synchronized on rising edge. If unused, leave the pin N/C.
ANT	ANT_DET	15	DI	Open circuit detection of active antenna	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V	If unused, leave the pin N/C.
	ANT_SHORT	16	DI	Short circuit detection of active antenna		If unused, leave the pin N/C.
	ANT_ON	14	DO	Controls external LNA and active antenna power	V_{OH}min = VCC - 0.4 V V_{OL}max = 0.4 V	In Continuous mode, the pin is at high level. In power saving mode, the pin is at low level. If unused, leave the pin N/C.

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
	RF_IN	11	AI	GNSS antenna interface	-	50 Ω characteristic impedance.
	VDD_RF	9	PO	Supplies power for external RF components	$V_O$nom = VCC	VDD_RF = VCC, the output current capacity depends on VCC. It is typically used to supply power for an external active antenna or LNA. If unused, leave the pin N/C.
System	RESET_N	8	DI	Resets the module	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V	Active low.
	BOOT	6	DI	Controls module startup mode	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V	Pulled down internally by default. If the pin is kept at high level for about 50 ms during startup, the module enters Boot download mode.
GND	GND	10, 12, 13, 24	-	Ground	-	Ensure a good GND connection for all module GND pins, preferably with a large ground plane.
RESERVED	RESERVED	2, 4, 5, 7, 17, 18, 19	-	Reserved	-	These pins must be left N/C and cannot be connected to power or GND.

NOTE

Leave RESERVED and unused pins N/C.

3 Power Management

The module features a power optimized architecture with built-in autonomous energy saving capabilities to minimize power consumption at any given time. The receiver can be used in two operating modes: Backup mode for optimum power consumption, and Continuous mode for optimum performance.

3.1. Power Unit

VCC is the supply voltage pin of the module. It supplies the PMU which in turn supplies the entire system. The load current of the VCC pin varies according to VCC voltage level, processor load, and satellite acquisition. It is important to supply sufficient current and make sure the power supply is clean and stable.

The V_BCKP pin supplies the backup domain, which includes RTC and SRAM. To achieve quick startup and improve TTFF, the backup domain power supply should be valid at all times during Backup mode. If the VCC is not valid, the V_BCKP supplies power for SRAM that contains all the necessary GNSS data and some of the user configuration variables.

VDD_RF is an output pin, equal in voltage to the VCC input. In the Continuous mode, VDD_RF supplies the external active antenna or the LNA. Only if VCC is turned off, VDD_RF is turned off.

The module's internal power supply is shown below:

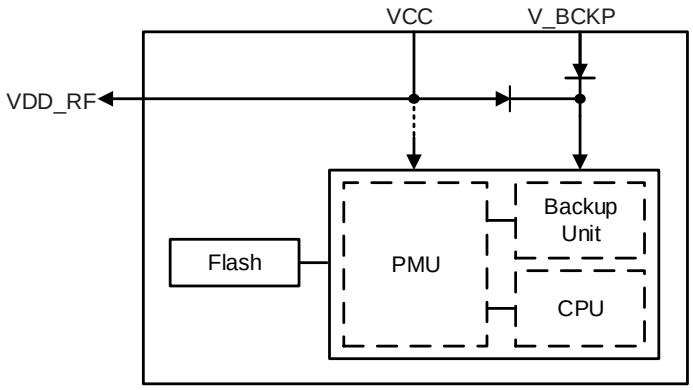


Figure 3: Internal Power Supply

3.2. Power Supply

3.2.1. VCC

The VCC is the supply voltage pin that supplies BB and RF.

Module power consumption may vary by several orders of magnitude, especially when power saving mode is enabled. Therefore, it is important for the power supply to be able to sustain peak power for a short time, ensuring that the load current does not exceed the rated value. When the module starts up or switches from the Backup mode to the Continuous mode, VCC must charge the internal capacitors in the core domain. In some cases, this can lead to a significant current drain.

For low-power applications using power saving mode, it is important for the LDO at the power supply or module input to be able to provide sufficient current when the module is switched from Backup mode to Continuous mode. An LDO with a high PSRR should be chosen for good performance. In addition, a TVS, and a combination of a 10 µF, a 100 nF and a 33 pF decoupling capacitor should be added near the VCC pin. The minimum value capacitor should be the closest to the VCC pin.

It is recommended to use a fast-discharging LDO voltage regulator, which can ensure a quick voltage drop when the VCC power is cut off.

It is not recommended to use a switching DC-DC converter.

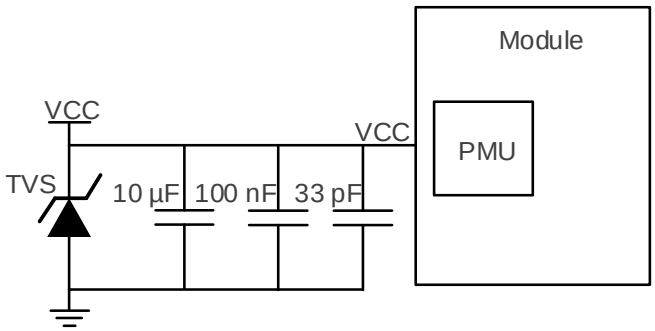


Figure 4: VCC Input Reference Circuit

NOTE

Ensure the module VCC is controlled by MCU to save power, or restart the module if it enters an abnormal state.

3.2.2. V_BCKP

The V_BCKP pin supplies power for the backup domain. Use of valid time and GNSS orbit data at startup, allows GNSS hot (warm) start. V_BCKP must be connected to power supply for startup, and it should always be powered if hot (warm) start is needed.

If there is a constant power supply in your system, it can be used to provide a suitable voltage to power V_BCKP.

It is recommended to place a battery with a TVS and a combination of a 4.7 μF, a 100 nF and a 33 pF capacitor near the V_BCKP pin. The reference charging circuit is illustrated below.

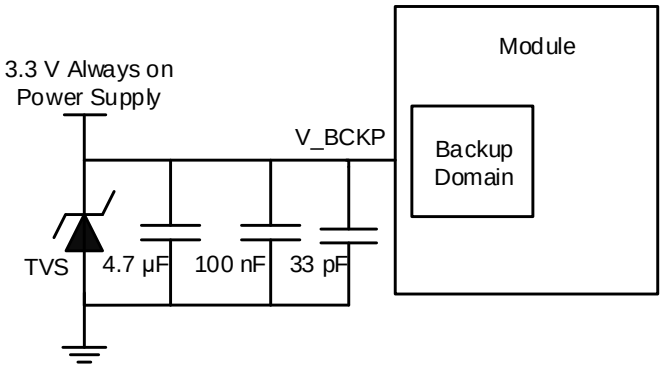


Figure 5: Backup Domain Input Reference Circuit

V_BCKP can also be powered by a 3.7 V lithium battery. It is recommended to control the enable pin of LDO via MCU, as shown below.

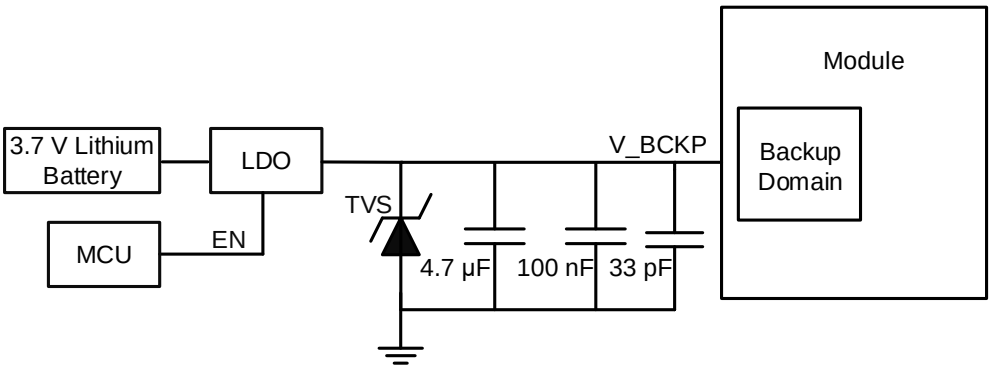


Figure 6: Reference Power Supply Circuit with 3.7 V Lithium Battery

NOTE

1. If V_BCKP is below the minimum value of the recommended operating voltage, the module cannot work normally.
2. It is recommended to control the V_BCKP of the module via MCU to restart the module if the module enters an abnormal state.

3.3. Power Modes

3.3.1. Feature Comparison

The module features supported in different modes are listed in the table below.

Table 7: Feature Comparison in Different Power Modes

Features	Continuous	Backup
NMEA from UART	●	-
1PPS	●	-
RF	●	-
Acquisition & Tracking	●	-
Power Consumption	High	Low
Position Accuracy	High	-

3.3.2. Continuous Mode

If VCC and V_BCKP are powered on, the module automatically enters the Continuous mode that comprises acquisition mode and tracking mode. In acquisition mode, the module initiates a satellite search to determine visible satellites, coarse frequency, as well as the code phase of satellite signals. Once the acquisition is completed, the module automatically switches to tracking mode. In tracking mode, the module tracks satellites and demodulates the navigation data from specific satellites.

3.3.3. Backup Mode

For power-sensitive applications, the module supports a Backup mode to reduce power consumption. Only backup domain is active in Backup mode and it keeps track of time.

- To enter Backup mode: Cut off the power supply of VCC for at least 1 s and keep V_BCKP powered.
- To exit Backup mode: Restore the VCC power supply.

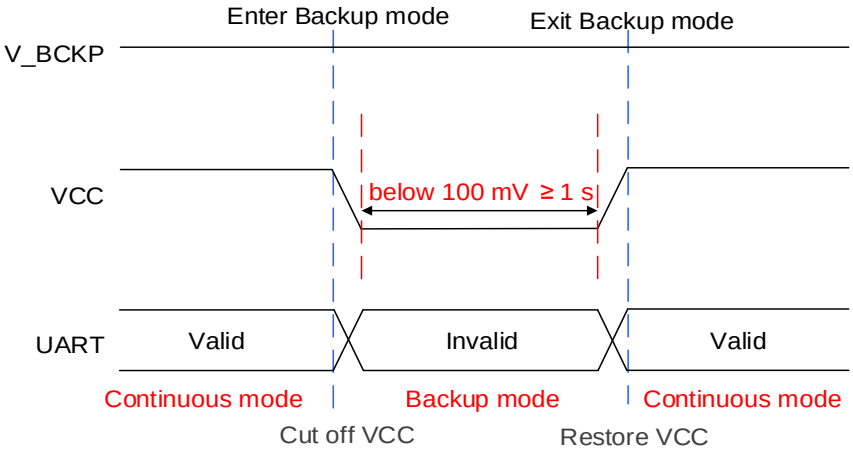


Figure 7: Enter/Exit Backup Mode Sequence

NOTE

Ensure a stable V_BCKP voltage without a rush or drop when the VCC is switched on or off.

3.4. Power-up Sequence

Once the VCC and V_BCKP are powered up, the module starts up automatically and the voltage should rise rapidly in less than 50 ms.

To ensure the correct power-up sequence, the backup unit should start up no later than the PMU. Hence, the V_BCKP must be powered simultaneously with the VCC or before it.

Ensure that the VCC and V_BCKP have no rush or drop during rising time, and then keep them stable. The recommended ripple is less than 50 mV.

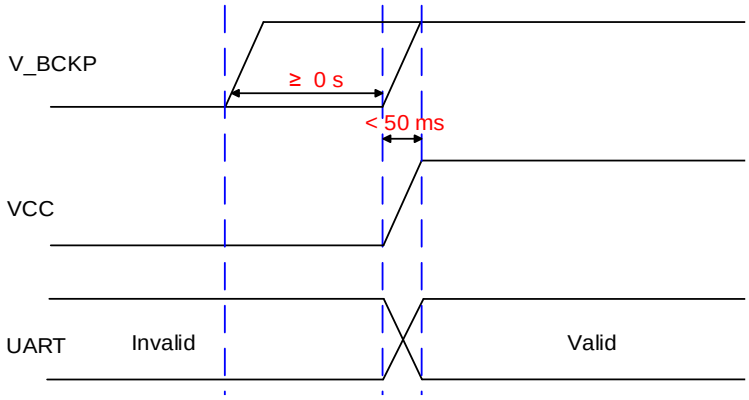


Figure 8: Power-up Sequence

3.5. Power-down Sequence

Once the VCC and V_BCKP are shut down, the module turns off automatically and voltage should drop quickly within less than 50 ms. It is recommended to use a voltage regulator that supports fast discharging.

To avoid abnormal voltage condition, if VCC and V_BCKP fall below the minimum specified value, the system must initiate a power-on restart by lowering VCC and V_BCKP to less than 100 mV for at least 1 s.

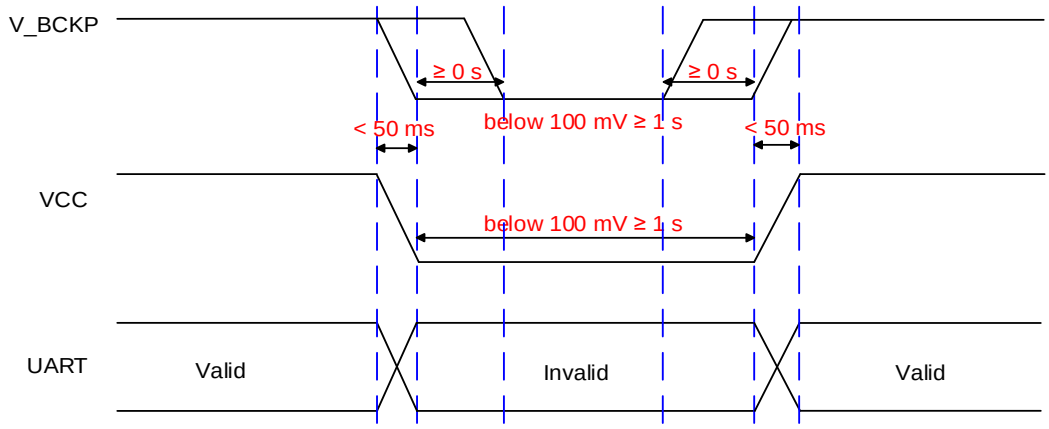


Figure 9: Power-down and Power-on Restart Sequence

4 Application Interfaces

4.1. I/O Pins

4.1.1. Communication Interfaces

The following interfaces can be used for data reception and transmission.

4.1.1.1. UART Interface

The module provides one UART interface with the following features:

- Supports standard NMEA message, PSTM message, and firmware upgrade.
- Supported baud rates: 115200 bps, 230400 bps, 460800 bps, and 921600 bps.
- Hardware flow control and synchronous operation are not supported.

For more information, see *document [1] protocol specification*.

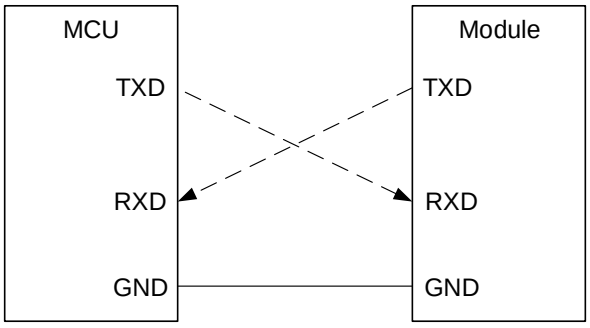


Figure 10: UART Interface Reference Design

A reference design is shown in the figure above. For more information, see *document [3] reference design*.

NOTE

1. UART interface default settings may vary depending on software version. See specific software versions for details.
2. If the I/O voltage of MCU is not matched with the module, a level-shifting circuit must be used.

4.1.2. CLK_OUT

The CLK_OUT output pin generates 10 million pulses per second periodic signals. It may be used as a high frequency reference signal. Maintaining high accuracy of CLK_OUT requires visible satellites in an open sky environment and powered VCC.

4.1.3. 1PPS

The 1PPS can be used for time pulse signals or timing feature, it generates one pulse per second periodic signal, synchronized to GNSS time grid with intervals. Maintaining high accuracy of 1PPS requires visible satellites in an open sky environment and powered VCC. See *Table 3: Product Performance* for details about pulse accuracy.

4.2. System Pins

4.2.1. RESET_N

RESET_N is an input pin. The module can be reset by driving RESET_N low for at least 100 ms and then releasing it.

By default, the RESET_N pin is internally pulled up to V_BCKP with a 10 kΩ resistor, thus no external pull-up circuit is allowed for this pin.

An OC driver circuit as shown below is recommended to control the RESET_N pin.

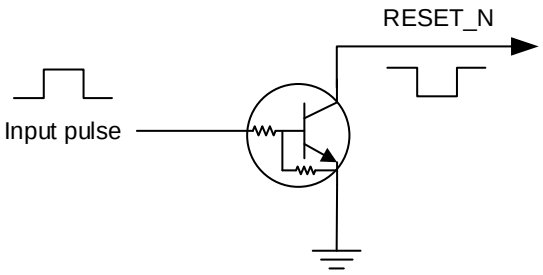


Figure 11: Reference OC Circuit for Module Reset

The following figure shows the reset sequence of the module.

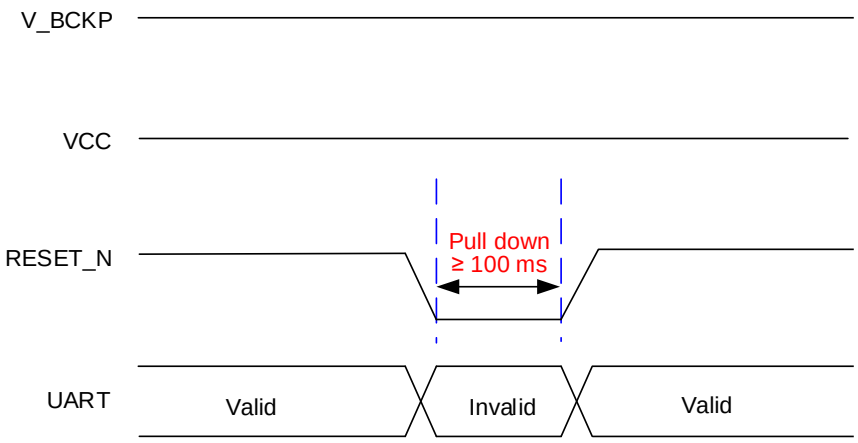


Figure 12: Reset Sequence

NOTE

RESET_N must be connected so that it can be used to reset the module if the module enters an abnormal state.

4.2.2. BOOT

The BOOT pin can be used to set the module to Boot download mode. It is pulled down internally by default. If the pin is kept at high level for about 50 ms during startup, the module enters Boot download mode. For more information about the reference circuit design, see *document [3] reference design*.

The BOOT pin voltage level is checked automatically to identify the operating mode when the module is powered on.

Table 8: Operating Modes

Voltage Level	Operating Mode	Comment
Low	Normal	BOOT pin is pulled down internally by default.
High	Boot download	If the pin is kept at high level for about 50 ms during startup, the module enters Boot download mode.

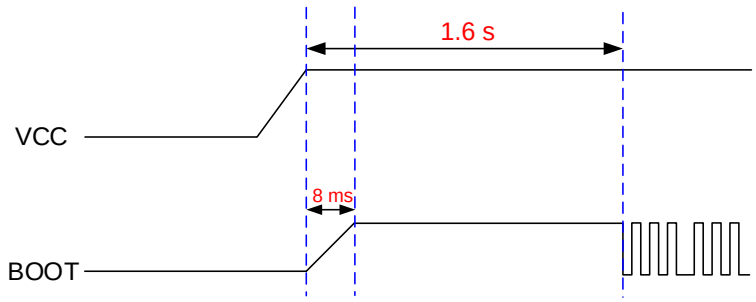


Figure 13: BOOT Pin State (Normal Operating Mode)

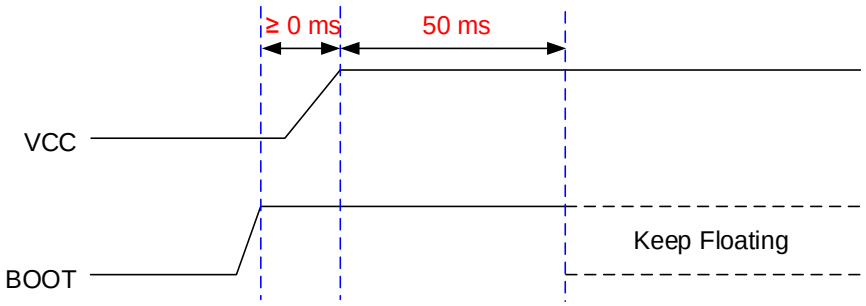


Figure 14: BOOT Pin Control Sequence (Boot Download Mode)

4.3. Avoiding Current Leakage on I/O Pins

This chapter provides important design considerations for the module's current leakage in Backup mode and the complete power-off state of the module, which are defined as follows:

- In Backup mode, the module's VCC power pin is disconnected while the V_BCKP pin is still powered.
- In the complete power-off state, all power pins (V_BCKP and VCC) of the module are powered off.

In the above two power states, when there is an external voltage on the module's I/O pins, the power consumption in Backup mode will increase, and there will be residual voltage on VCC pin, whereas the external voltage can cause parasitic leakage current to flow through the modules in the completely powered-off state, leading to energy loss. To prevent current leakage and parasitic leakage current, no external voltage is allowed on the module's I/O pins. Two ways to accomplish this are:

1. Pull down all I/O pins connected to the module when it enters Backup mode or is completely powered off, while the host is still working.

2. Use components that prevent backflow current from passing through when power is turned off, specifically designed for power-off applications. The noninverting buffer with output-enable (OE) control is recommended to play an isolation role. When the OE of the enable pin is low, the output end of the noninverting buffer exhibits a high resistance state. A recommended design of the UART communication between the module and host is as follows:

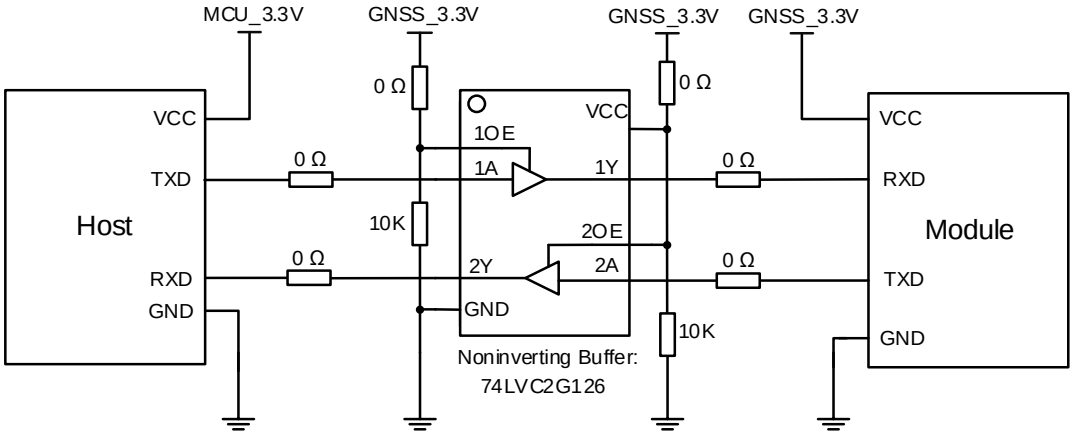


Figure 15: Noninverting Buffer Circuit Between Module and Host

5 Design

This chapter explains the reference design of RF section and recommended footprint of the module. A GNSS receiver could be vulnerable to environmental interference. To learn the details about interference and ensuring interference immunity, see *document [4] GNSS antenna application note*.

5.1. Antenna Reference Design

5.1.1. Antenna Specifications

The module can be connected to a dedicated active GNSS antenna to receive GNSS satellite signals. The recommended antenna specifications are given in the table below.

Table 9: Recommended Antenna Specifications

Antenna Type	Specifications
Active Antenna	Frequency Range: 1559–1606 MHz Polarization: RHCP VSWR: < 2 (Typ.) Passive Antenna Gain: > 3 dBi Active Antenna Noise Figure: < 2.5 dB Active Antenna Total Gain: 23–33 dB [5] Axial Ratio: < 3 dB -3 dB Beamwidth: > 90° Out-of-band Rejection: > 30 dB

NOTE

For recommended antenna selection and design, see *document [4] GNSS antenna application note* or contact Quectel Technical Support (support@quectel.com).

[5] Total antenna gain equals internal LNA gain minus total insertion loss of cables and components inside the antenna.

5.2. Active Antenna Reference Design

To mitigate the impact of out-of-band signals on the GNSS module in a complex electromagnetic environment, a SAW filter circuit must be added to the antenna design. The SAW filter circuit has a stable suppression effect on all out-of-band signals. The recommended SAW filter is B39162B2651P810 from RF360. In the actual layout, the circuit should be placed close to RF_IN pin. The SAW filter circuit should be selected according to the use case.

If the active antenna is powered by VDD_RF, it is important to consider the operating voltage range of the antenna and the voltage drop on the power supply circuit. The voltage drop is caused by the inductor on the VDD_RF internal circuit, the resistor (R2) and the inductor (L1), MOSFET (Q1 which only is used in active antenna reference design with status detection) in the external power supply circuit.

To further mitigate the impact of out-of-band signals on GNSS module performance, you must choose the active antenna whose SAW filter is placed in front of the LNA in the internal framework. **DO NOT** place the LNA in the front. The minimum operating voltage of the selected active antenna must meet the circuit design characteristics.

See *Figure 16: Active Antenna Reference Design Without Status Detection* and *Figure 17: Active Antenna Reference Design with Status Detection* for more details.

5.2.1. Active Antenna Reference Design Without Status Detection

The following figure is a typical reference design of an active antenna without status detection.

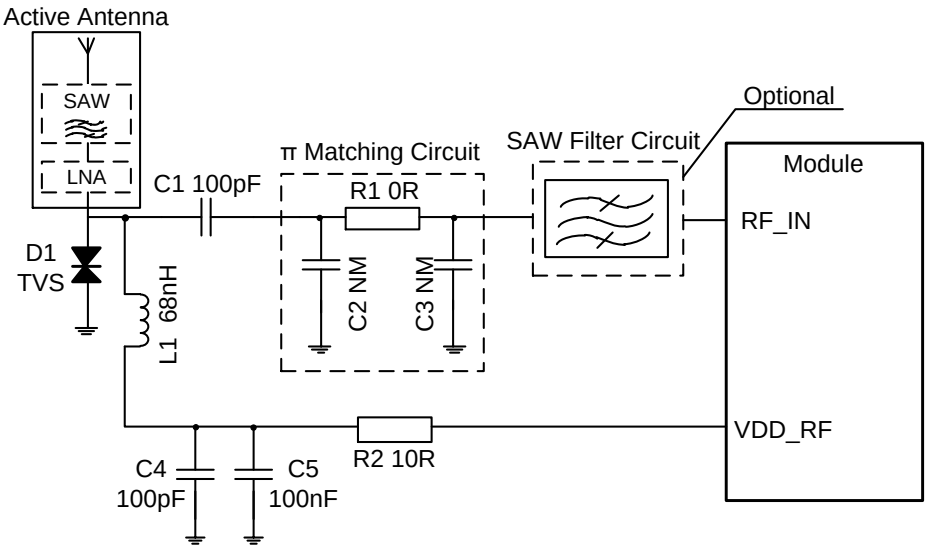


Figure 16: Active Antenna Reference Design Without Status Detection

C1 is used for blocking DC from VDD_RF. C2, R1 and C3 components are reserved for matching antenna impedance. By default, C1 is 100 pF, R1 is 0 Ω, while C2 and C3 are not mounted. These components are placed close to the antenna in the layout. D1 is an electrostatic discharge (ESD) protection device to prevent the RF components inside the module from being broken down by static electricity introduced into the antenna interface, so it must be mounted. The junction capacitance of D1 cannot be more than 0.6 pF and a transient voltage suppressor is recommended.

L1 inductor is used to prevent the RF signal from leaking into the VDD_RF and to prevent noise propagation from the VDD_RF to the antenna. The L1 inductor routes the bias voltage to the active antenna without losses. Place L1, C4 and C5 close to the antenna interface and route the proximal end of L1 pad on the RF trace. The recommended value of L1 should be at least 68 nH. The R2 resistor should be mounted to protect the module in case the active antenna is short-circuited to the ground plane. RF trace impedance should be controlled to 50 Ω and trace length should be kept as short as possible. For more information, see *document [5] RF layout application note*.

5.2.2. Active Antenna Reference Design with Antenna Status Detection

The active antenna status detection circuit includes two detection pins (ANT_DET and ANT_SHORT) and one control pin (ANT_ON), as shown below.

5.2.2.1. ANT_DET

The ANT_DET is a digital input pin for detecting external active antenna status. Through the antenna detection circuit, the pin can be used to assess whether the antenna is in an open circuit state. See *Table 10: Active Antenna Detection Circuit Control Logic* for details on active antenna status detection.

5.2.2.2. ANT_SHORT

The ANT_SHORT is a digital input pin for detecting external active antenna status. Through the antenna detection circuit, the pin can be used to assess whether the antenna is in a short circuit state. See *Table 10: Active Antenna Detection Circuit Control Logic* for details on active antenna status detection.

5.2.2.3. ANT_ON

The ANT_ON pin controls the on-off of the active antenna power supply circuit via Q1 and Q2 to reduce the power consumption in power saving mode. The control logic is shown in *Table 10: Active Antenna Detection Circuit Control Logic*.

The following figure is a typical reference design of an active antenna with antenna status detection. In this design, antenna short circuit/open circuit can be detected. Upon detection of a short circuit, the antenna power supply will be immediately shut down.

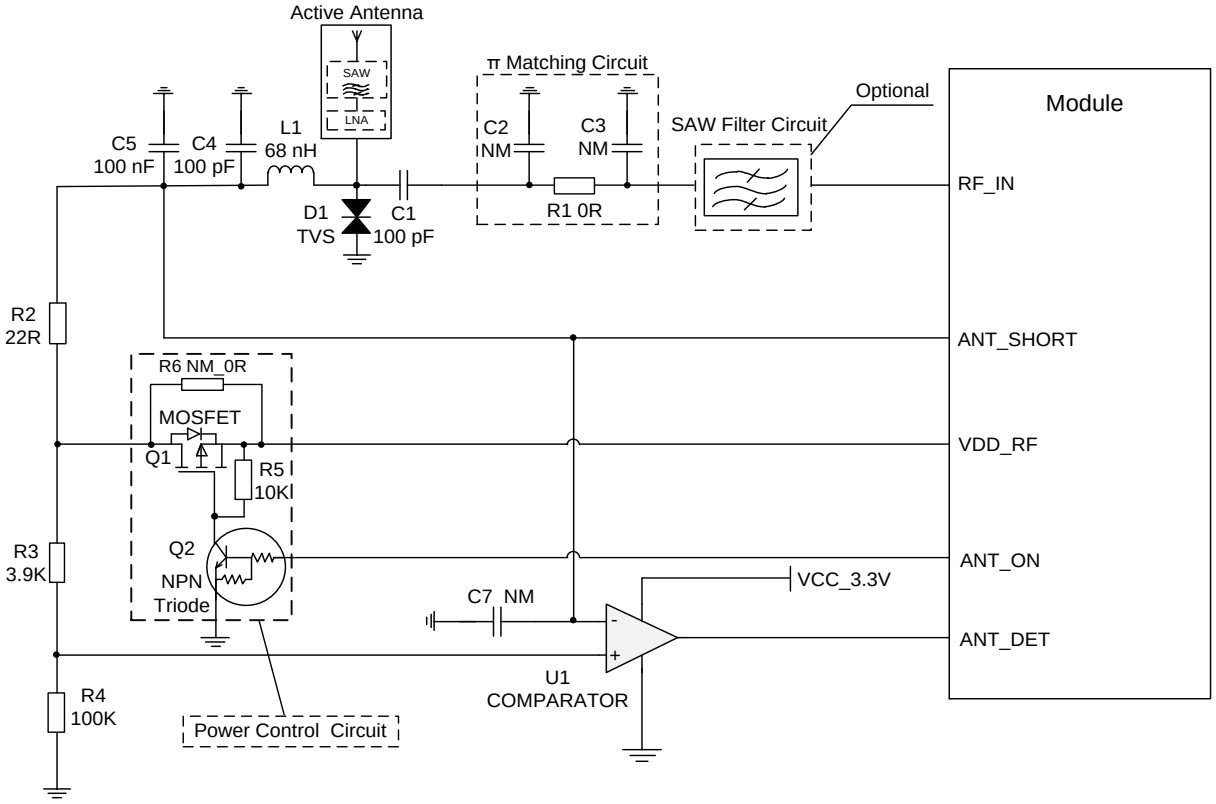


Figure 17: Active Antenna Reference Design with Status Detection

Table 10: Active Antenna Detection Circuit Control Logic

Detection Pin		Control Pin	Antenna Status
ANT_SHORT	ANT_DET	ANT_ON	
1	1	1	Normal
1	0	1	Open circuit
0	-	0	Short circuit

NOTE

1. R2 in the *Figure 17: Active Antenna Reference Design with Status Detection* is a must, otherwise the module may be damaged permanently through potential short-circuiting of the active antenna.
2. VDD_RF can be used to supply the active antenna. Its voltage range is from 3.0 to 3.6 V (VDD_RF = VCC), and the typical value is 3.3 V. If VDD_RF cannot meet the antenna's power supply requirements, an external power supply is required.
3. After the antenna is short circuited, it must be reset manually to work normally.

5.3. Recommended Footprint

A module footprint is illustrated in the figure below. These are recommendations, not specifications.

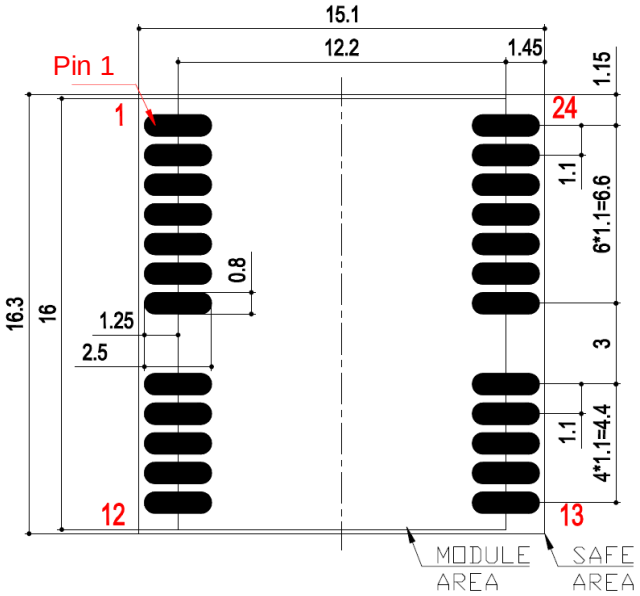


Figure 18: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6 Electrical Specification

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital pins of the module are listed in table below.

Table 11: Absolute Maximum Ratings

Parameter	Description	Min.	Max.	Unit
VCC	Main Power Supply Voltage	-0.3	3.6	V
V_BCKP	Backup Supply Voltage	-0.3	3.6	V
V_{IN}_IO	Input Voltage at I/O Pins	-0.3	VCC + 0.3	V
P_{RF_IN}	Input Power at RF_IN	-	0	dBm
T_storage	Storage Temperature	-40	90	°C

NOTE

Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. The product is not protected against over-voltage or reversed voltage. Therefore, it is necessary to use appropriate protection diodes to keep voltage spikes within the parameters given in the table above.

6.2. Recommended Operating Conditions

All specifications are at an ambient temperature of +25 °C. Extreme operating temperatures can significantly impact the specified values. Applications operating near the temperature limits should be tested to ensure specification validity.

Table 12: Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Main Power Supply Voltage	3.0	3.3	3.6	V
V_BCKP	Backup Supply Voltage	2.1	3.3	3.6	V
IO_Domain	Digital I/O Pin Voltage Domain	-	VCC	-	V
V_{IL}	Digital I/O Pin Low-level Input Voltage	-0.3	-	0.8	V
V_{IH}	Digital I/O Pin High-level Input Voltage	2.0	-	3.6	V
V_{OL}	Digital I/O Pin Low-level Output Voltage	-	-	0.4	V
V_{OH}	Digital I/O Pin High-level Output Voltage	VCC - 0.4	-	-	V
TXD	TXD Low-level Output Voltage	-	-	0.4	V
	TXD High-level Output Voltage	VCC - 0.7	2.8	-	V
VDD_RF	VDD_RF Output Voltage	-	VCC	-	V
I_{VDD_RF}	VDD_RF Output Current	-	-	110	mA
T_operating	Operating Temperature	-40	25	+85	°C

NOTE

1. Operation beyond the “Operating Conditions” is not recommended. Extended exposure beyond the “Operating Conditions” may affect device reliability.
2. Digital I/O Pin in the table above refers to all digital pins specified in *Table 6: Pin Description* except TXD.

6.3. Supply Current Requirement

The following table lists the supply current values of the total system that may be applied. Actual power requirements may vary depending on processor load, external circuits, firmware version, the number of satellites tracked, signal strength, startup type, test time and conditions.

Table 13: Supply Current

Parameter	Description	Condition	$I_{Typ.}$ [6]	I_{PEAK} [6]
I_{VCC} [7]	Current at VCC	Acquisition	222 mA	320 mA
		Tracking	232 mA	320 mA
I_{V_BCKP} [8]	Current at V_BCKP	Continuous mode	140 μA	160 μA
		Backup mode	55 μA	86 μA

6.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly, and testing of the module; add ESD protective components to the ESD sensitive interfaces and points in the product design.

Measures to ensure protection against ESD damage when handling the module:

- When mounting the module onto a motherboard, make sure to connect the GND first, and then the RF_IN pin.
- When handling the RF_IN pin, do not come into contact with any charged capacitors or materials that may easily generate or store charges (such as patch antenna, coaxial cable and soldering iron).
- When soldering the RF_IN pin, make sure to use an ESD safe soldering iron (tip).

[6] Room temperature, measurements are taken with typical voltage.
[7] Used to determine maximum current capability of power supply.
[8] Used to determine required battery current capability.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are in millimeters (mm). The dimensional tolerances are ±0.20 mm, unless otherwise specified.

7.1. Top, Side and Bottom View Dimensions

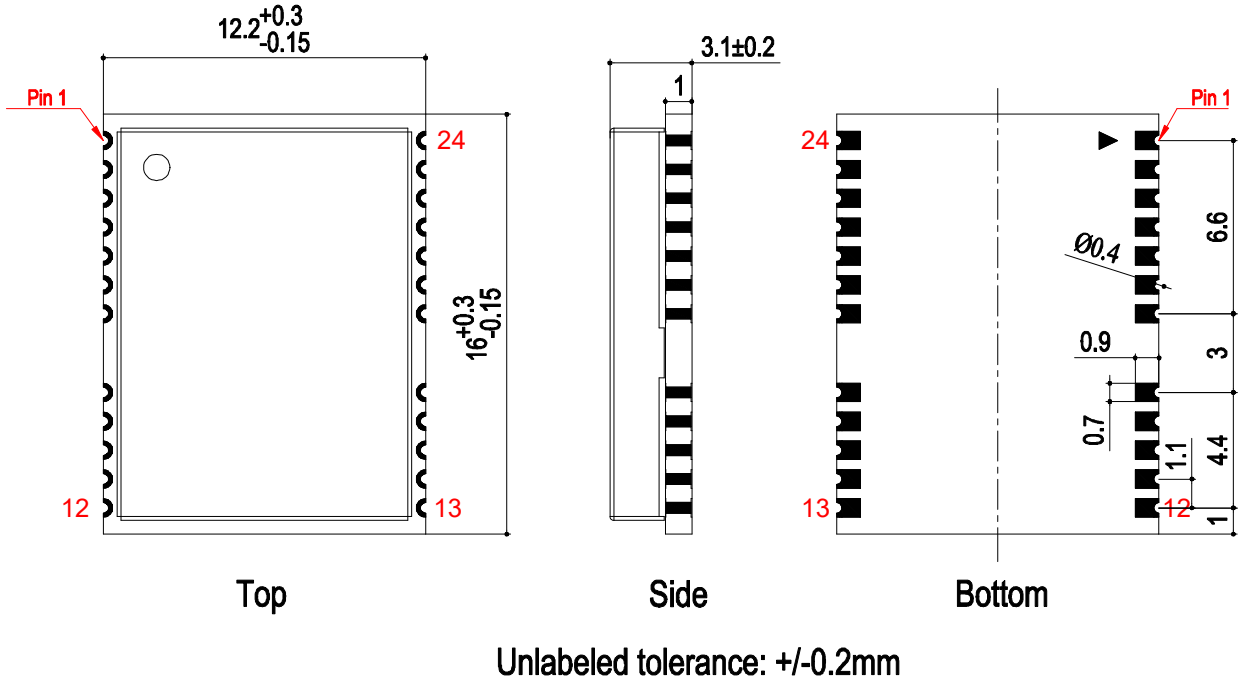


Figure 19: Top, Side and Bottom View Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Top and Bottom Views

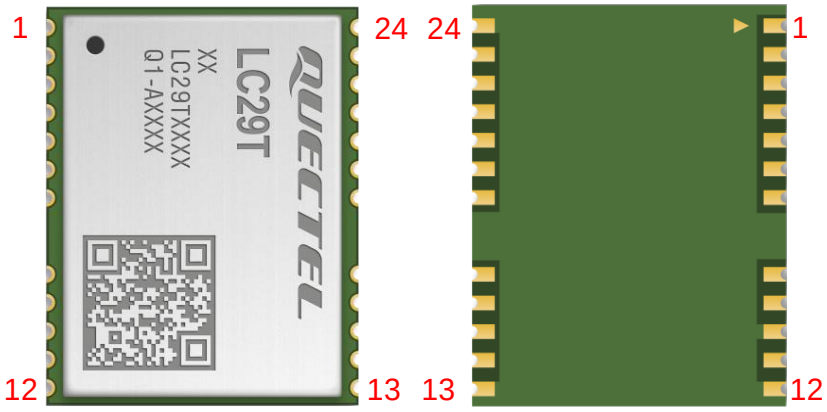


Figure 20: Top and Bottom Module Views

NOTE

The images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, see the module received from Quectel.

8 Product Handling

8.1. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The module adopts carrier tape packaging and details are as follows.

8.1.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

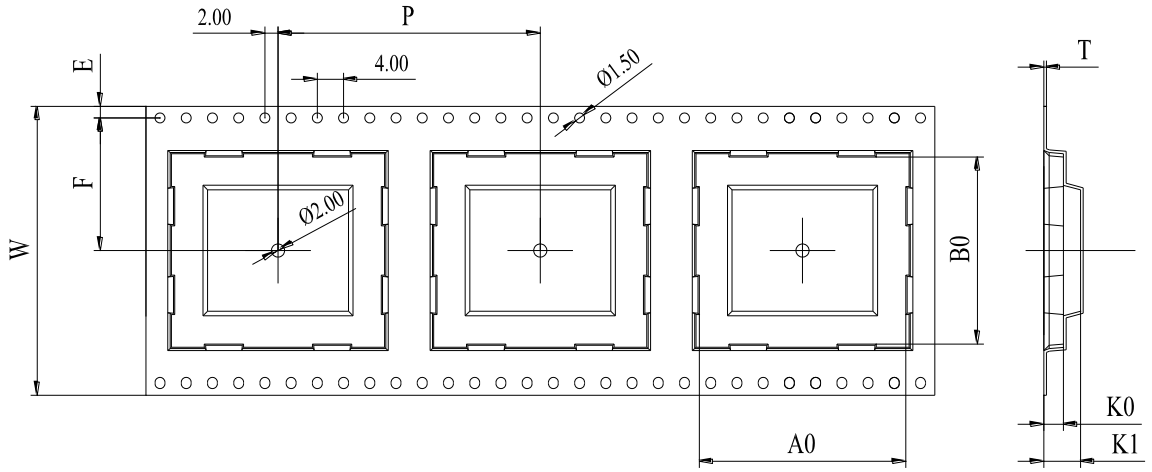


Figure 21: Carrier Tape Dimension Drawing (Unit: mm)

Table 14: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	20	0.4	12.6	16.4	3.6	5.7	14.2	1.75

8.1.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

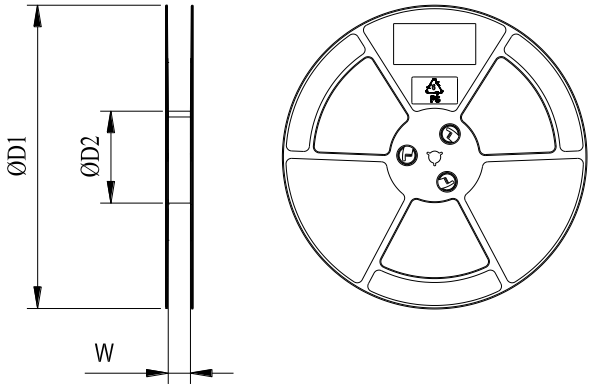


Figure 22: Plastic Reel Dimension Drawing

Table 15: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.1.3. Mounting Direction

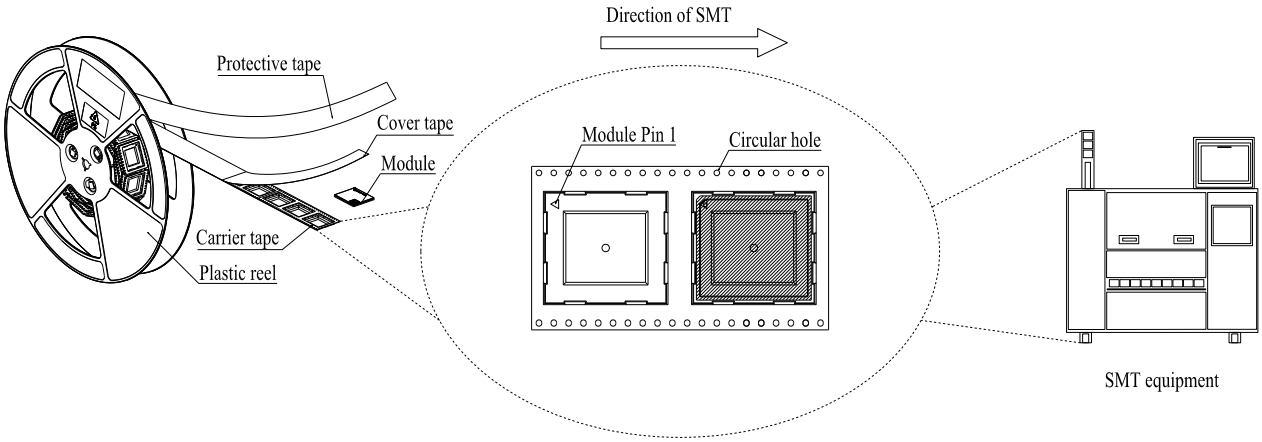
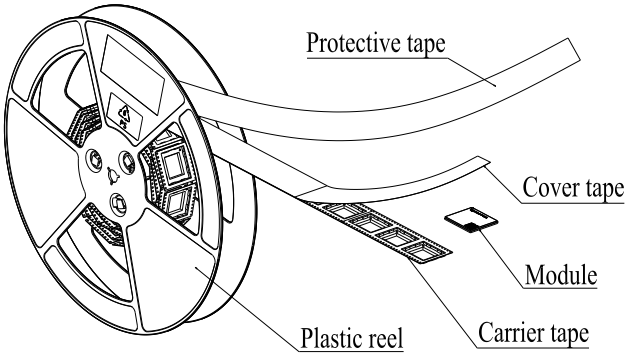


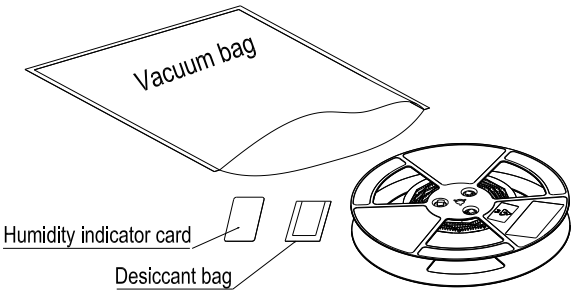
Figure 23: Mounting Direction

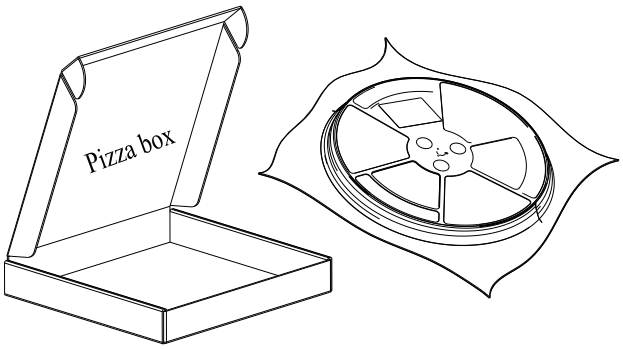
8.1.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

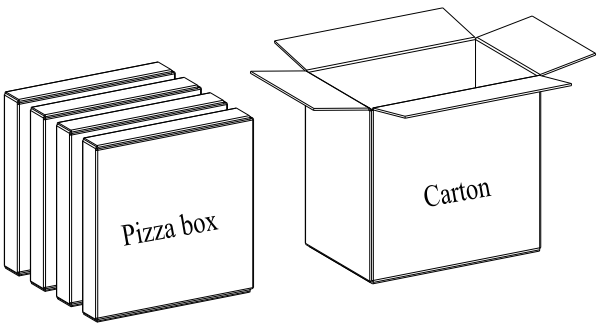
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.



Pizza box size (mm): 363 × 343 × 55
Carton size (mm): 380 × 250 × 365

Figure 24: Packaging Process

8.2. Storage

The module is provided in a vacuum-sealed packaging. MSL of the module is rated at 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [9] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should meet the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the module.

[9] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

8.3. Manufacturing and Soldering

Push the squeegee to apply solder paste on the stencil surface, thus making the paste fill the stencil openings and then penetrate the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. For more information about the stencil thickness for the module, see *document [6] module SMT application note*.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid module damage caused by repeated heating, it is recommended to that the module should be mounted only after reflow soldering of the other side of the PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown in the figure and table below.

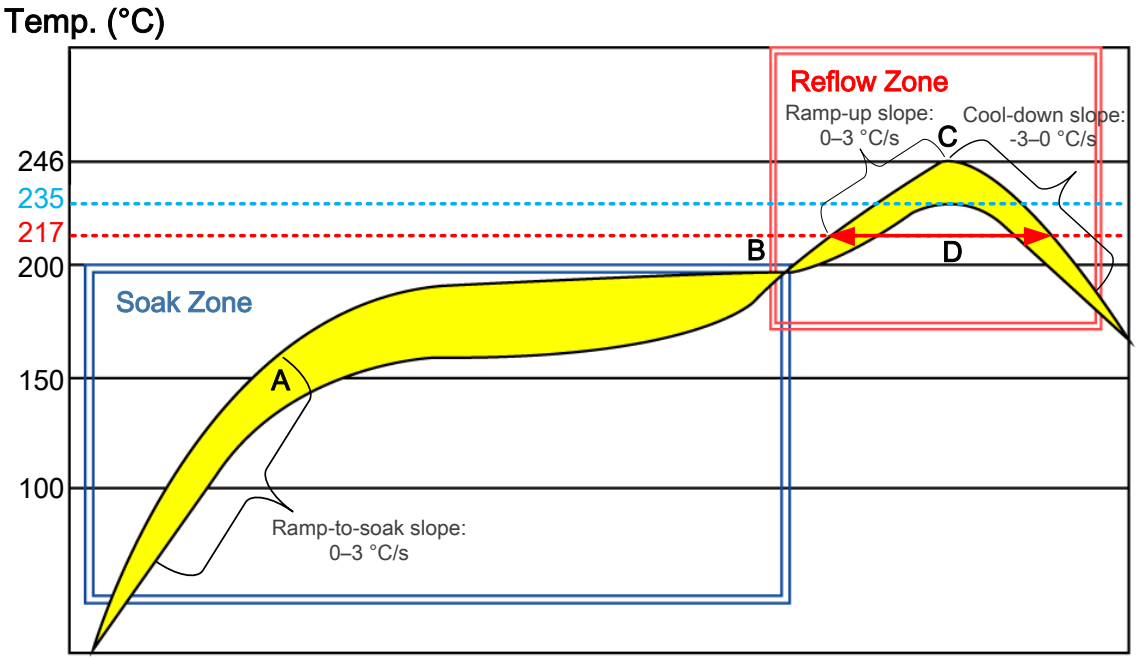


Figure 25: Recommended Reflow Soldering Thermal Profile

Table 16: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max. Temperature	235–246 °C
Cool Down slope	-3–0 °C/s
Reflow Cycle	
Max. Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may require direct contact with the module, **NEVER** wipe the module shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, and trichloroethylene. Otherwise, the shielding can may become rusty.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, **DO NOT** use any coating material that may chemically react with the PCB or shielding cover. Prevent the coating material from penetrating the module shield.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to SMT process complexity, contact Quectel Technical Support in advance regarding any ambiguous situation, or any process (e.g., selective soldering, ultrasonic soldering) that is not addressed in *document [6] module SMT application note*.

9 Labelling Information

The label of the Quectel GNSS modules contains important product information. The location of the product type number is shown in the figure below.

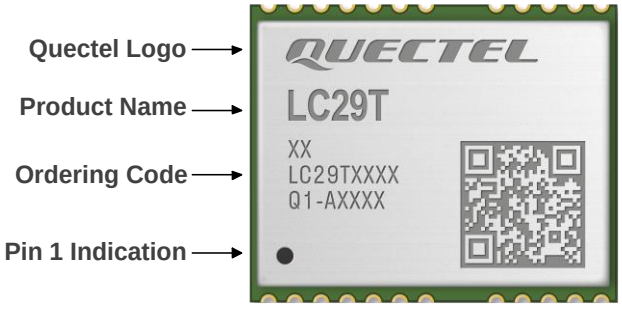


Figure 26: Labelling Information

The image above is for illustrative purposes only and may differ from the actual module. For authentic appearance and label, see the module received from Quectel.

10 Appendix References

Table 17: Related Documents

Document Name	
[1]	Quectel_LC29T(AA)&LC99T(IA)_GNSS_Protocol_Specification
[2]	Quectel_LG69T(AA,AD,AF,AI,AJ,AR)&LC29T(AA)&LC99T(IA)_Firmware_Upgrade_Guide
[3]	Quectel_LC29T(AA)_Reference_Design
[4]	Quectel_GNSS_Antenna_Application_Note
[5]	Quectel_RF_Layout_Application_Note
[6]	Quectel_Module_SMT_Application_Note

Table 18: Terms and Abbreviations

Abbreviation	Description
1PPS	One Pulse Per Second
3GPP	3rd Generation Partnership Project
AGNSS	Assisted GNSS (Global Navigation Satellite System)
BDS	BeiDou Satellite Navigation System
bps	bit(s) per second
CEP	Circular Error Probable
C/N_0	Carrier-to-noise Ratio
CPU	Central Processing Unit
DR	Dead Reckoning
EGNOS	European Geostationary Navigation Overlay Service

Abbreviation	Description
ESD	Electrostatic Discharge
GAGAN	GPS Aided Geo Augmented Navigation
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
I/O	Input/Output
IC	Integrated Circuit
IMU	Inertial Measurement Unit
I_{PEAK}	Peak Current
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LNA	Low-noise Amplifier
MCU	Microcontroller Unit/Microprogrammed Control Unit
MSAS	Multi-functional Satellite Augmentation System (Japan)
MSL	Moisture Sensitivity Levels
NavIC	Navigation with Indian Constellation
NMEA	National Marine Electronics Association 0183 Interface Standard
OC	Open Collector
PCB	Printed Circuit Board
PI	Power Input
PMU	Power Management Unit
ppm	parts per million
PSRR	Power Supply Rejection Ratio
QZSS	Quasi-zenith Satellite System

Abbreviation	Description
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RoHS	Restriction of Hazardous Substances
RTC	Real-time Clock
RTK	Real-time Kinematic
RXD	Receive Data (Pin)
SAW	Surface Acoustic Wave
SBAS	Satellite-based Augmentation System
SMD	Surface Mount Device
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Crystal Oscillator
T_operating	Operating Temperature
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
TXD	Transmit Data (Pin)
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCC	Supply Voltage
$V_I$max	Maximum Input Voltage
$V_I$min	Minimum Input Voltage
$V_I$nom	Normal Input Voltage
V_{IH}max	High-level Maximum Input Voltage
V_{IH}min	High-level Minimum Input Voltage

Abbreviation	Description
V_{IH}nom	High-level Normal Input Voltage
V_{IL}max	Low-level Maximum Input Voltage
V_{IL}min	Low-level Minimum Input Voltage
V_{O}nom	Normal Output Voltage
V_{OL}max	Low-level Maximum Output Voltage
V_{OH}min	High-level Minimum Output Voltage
VSWR	Voltage Standing Wave Ratio
WAAS	Wide Area Augmentation System
XTAL	External Crystal Oscillator