AN4043
Application note

SLLIMM™-nano
small low-loss intelligent molded module

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Introduction

In recent years the variable speed motor control market has required high performance solutions able to satisfy the increasing energy saving requirements, compactness, reliability, and system costs in home appliances, such as dish washers, refrigerator compressors, air conditioning fans, draining and recirculation pumps, and in low power industrial applications, such as small fans, pumps and tools, etc. To meet these market needs, STMicroelectronics has developed a new family of very compact, high efficiency, dual-in-line intelligent power modules, with optional extra features, called small low-loss intelligent molded module nano (SLLIMM™-nano).

The SLLIMM-nano product family combines optimized silicon chips, integrated in three main inverter blocks:

- power stage
  - six very fast IGBTs
  - six freewheeling diodes
- driving network
  - three high voltage gate drivers
  - three gate resistors
  - three bootstrap diodes
- protection and optional features
  - op amp for advanced current sensing
  - comparator for fault protection against overcurrent and short-circuit
  - smart shutdown function
  - dead time, interlocking function and undervoltage lockout.

Thanks to its very good compactness, the fully isolated SLLIMM-nano package (NDIP) is the ideal solution for applications requiring reduced assembly space, without sacrificing thermal performance and reliability.

Compared to discrete-based inverters, including power devices, and driver and protection circuits, the SLLIMM-nano family provides a high integrated level that means simplified circuit design, reduced component count, lower weight, and high reliability.

The aim of this application note is to provide a detailed description of SLLIMM-nano products, providing guidelines to motor drive designers for an efficient, reliable, and fast design when using the new ST SLLIMM-nano family.

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1 Inverter design concept and SLLIMM-nano solution

Motor drive applications, ranging from a few tens of watts to mega watts, are mainly based on the inverter concept thanks to the fact that this solution can meet efficiency, reliability, size, and cost constraints required in a number of markets.

As shown in *Figure 1*, an inverter for motor drive applications is basically composed of a power stage, mainly based on IGBTs and freewheeling diodes; a driving stage, based on high voltage gate drivers; a control unit, based on microcontrollers or DSPs; some optional sensors for protection and feedback signals for controls.
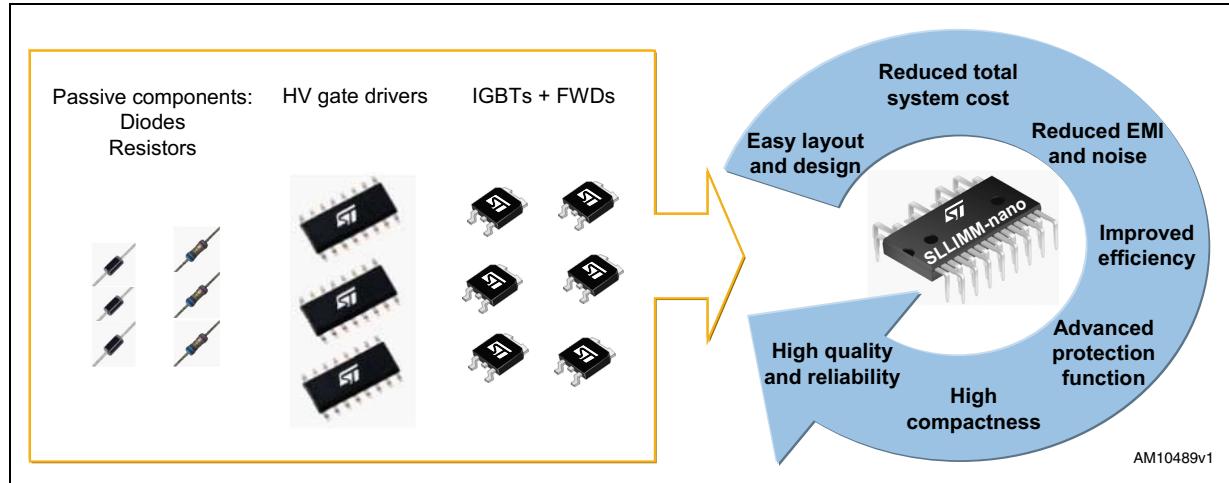
The approach of this solution with discrete devices produces high manufacturing costs associated with high reliability risks, bigger size and higher weight, a considerable number of components and the significant stray inductances and dispersions in the board layout.

Figure 1.   Inverter motor drive block diagram

In recent years, the use of intelligent power modules has rapidly increased thanks to the benefits of greater integration levels. The new ST SLLIMM-nano family is able to replace more than 20 discrete devices in a single package. *Figure 2* shows a comparison between a discrete-based inverter and the SLLIMM-nano solution, the advantages of SLLIMM-nano can be easily understood and can be summarized in a significantly improved design time, reduced manufacturing efforts, higher flexibility in a wide range of applications, and increased reliability and quality level.

In addition, the optimized silicon chips in both control and power stages and the optimized board layout provide maximized efficiency, reduced EMI and noise generation, higher levels of protection, and lower propagation delay time.

Figure 2.   Discrete-based inverter vs. SLLIMM-nano solution comparison

1.1   Product synopsis

The SLLIMM-nano family has been designed to satisfy the requirements of a wide range of final applications up to 100 W (in free air), such as:
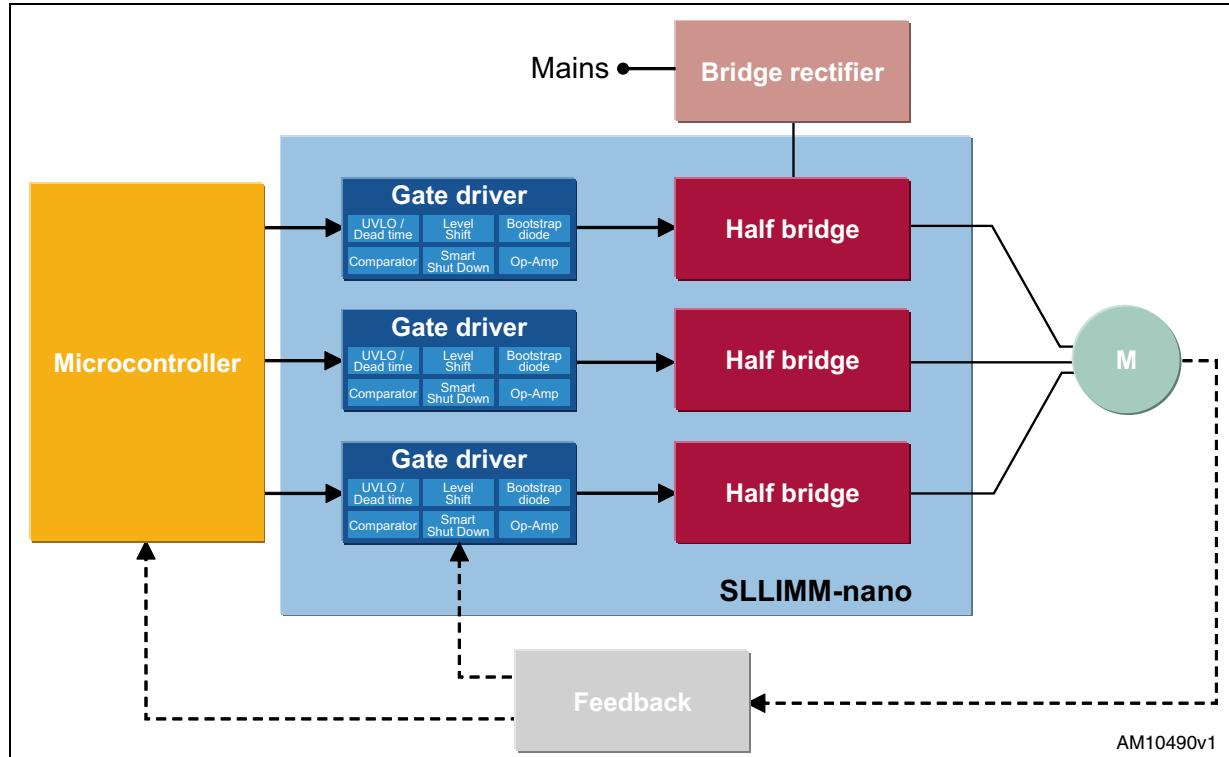
● dish washers

● refrigerator compressors

● air conditioning fans

● draining and recirculation pumps

● low power industrial applications

● small fans, pumps and tools.

The main features and integrated functions can be summarized as follows:

● 600 V, 3 A ratings

● 3-phase IGBT inverter bridge including:

 – six low-loss IGBTs

 – six low forward voltage drop and soft recovery freewheeling diodes

● three control ICs for gate driving and protection including:

 – smart shutdown function

 – comparator for fault protection against overcurrent and short-circuit

 – op amp for advanced current sensing

 – three integrated bootstrap diodes

 – interlocking function

 – undervoltage lockout

● open emitter configuration for individual phase current sensing

● very compact and fully isolated package

● integrated gate resistors for IGBT switching speed optimum setting

● gate driver proper biasing.

Figure 3 shows the block diagram of the SLLIMM-nano included in the inverter solution.

Figure 3.   SLLIMM block diagram

The power devices (IGBTs and freewheeling diodes), incorporated in the half bridge block, are tailored for a motor drive application delivering the greatest overall efficiency, thanks to the optimized trade-off between conduction and switching power losses and very low EMI generation, as a result of reduced dV/dt and di/dt.

The IC gate drivers have been selected in order to meet two levels of functionality, giving users more freedom to choose: a basic version which includes the essential features for a cost-effective solution and a fully featured version which provides advanced options for a sophisticated control method.
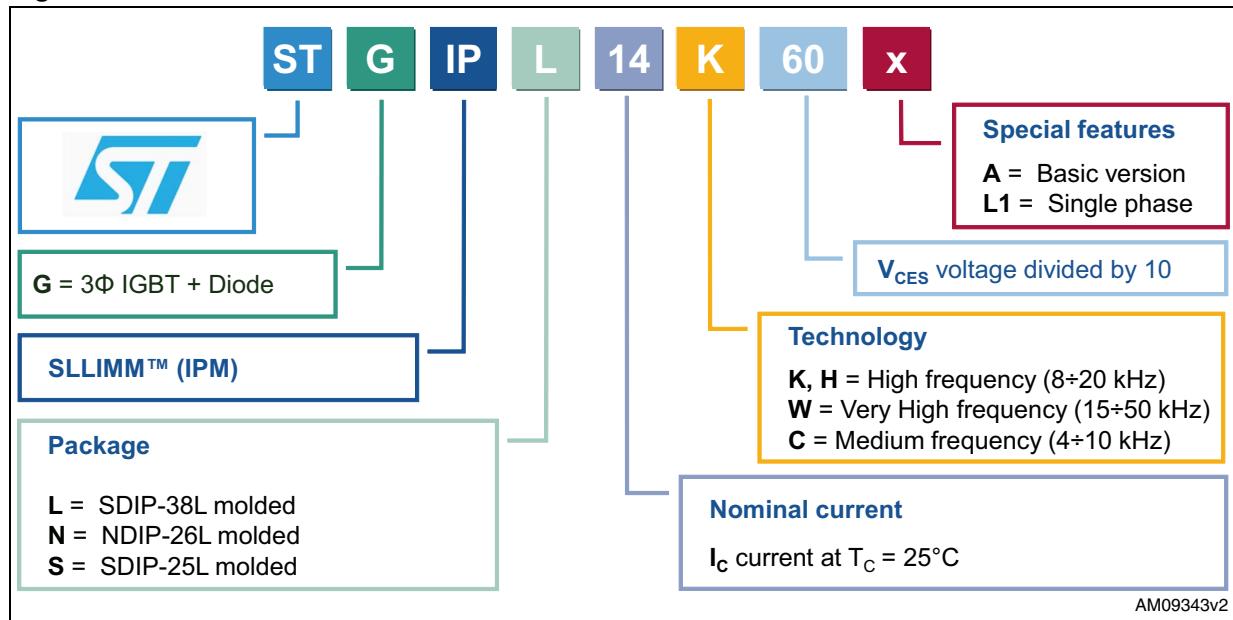
The fully isolated NDIP package offers a high compactness level, very useful in those applications with reduced space, ensuring at the same time, high thermal performance and reliability levels.

1.2 Product line-up and nomenclature

Table 1.   SLLIMM-nano line-up

Features	Basic version	Fully featured version
	STGIPN3H60A	STGIPN3H60
Voltage (V)	600	600
Current @ T_C = 25 °C (A)	3	3
R_{thJA} max. (°C/W)	50	50
Package type	NDIP-26L	NDIP-26L
Package size (mm) X, Y, Z	29.5x12.5x3.1	29.5x12.5x3.1
Integrated bootstrap diode	Yes	Yes
SD function	No	Yes
Comparator for fault protection	No	Yes (1 pin)
Smart shutdown function	No	Yes
Op amps for advanced current sensing	No	Yes
Interlocking function	Yes	Yes
Undervoltage lockout	Yes	Yes
Open emitter configuration	Yes (3 pins)	Yes (3 pins)
3.3 / 5 V input interface compatibility	Yes	Yes
High-side IGBT input signal	Active high	Active high
Low-side IGBT input signal	Active high	Active low

Figure 4.   SLLIMM-nano nomenclature

1.3 Internal circuit

Figure 5.   Internal circuit of the STGIPN3H60A
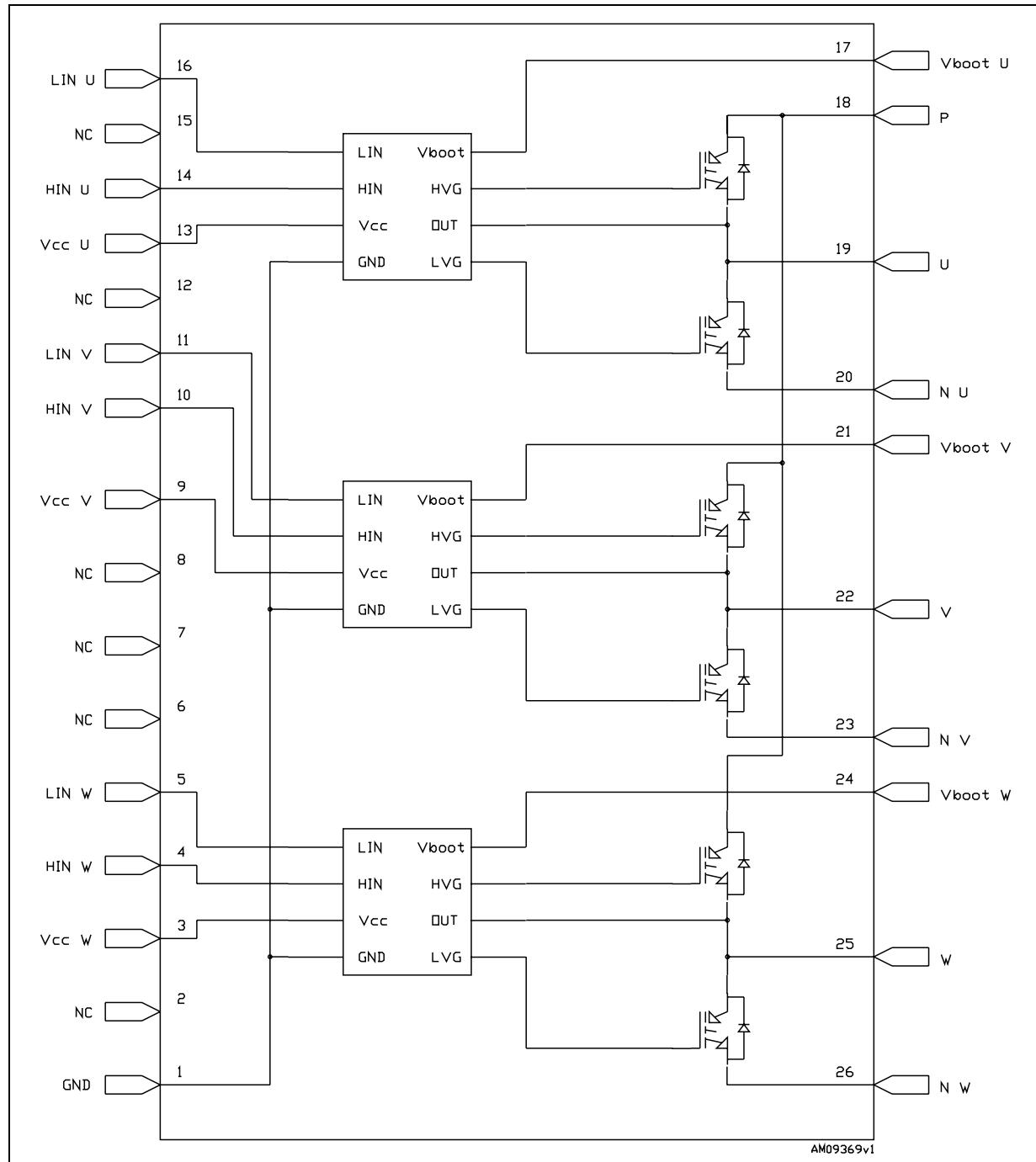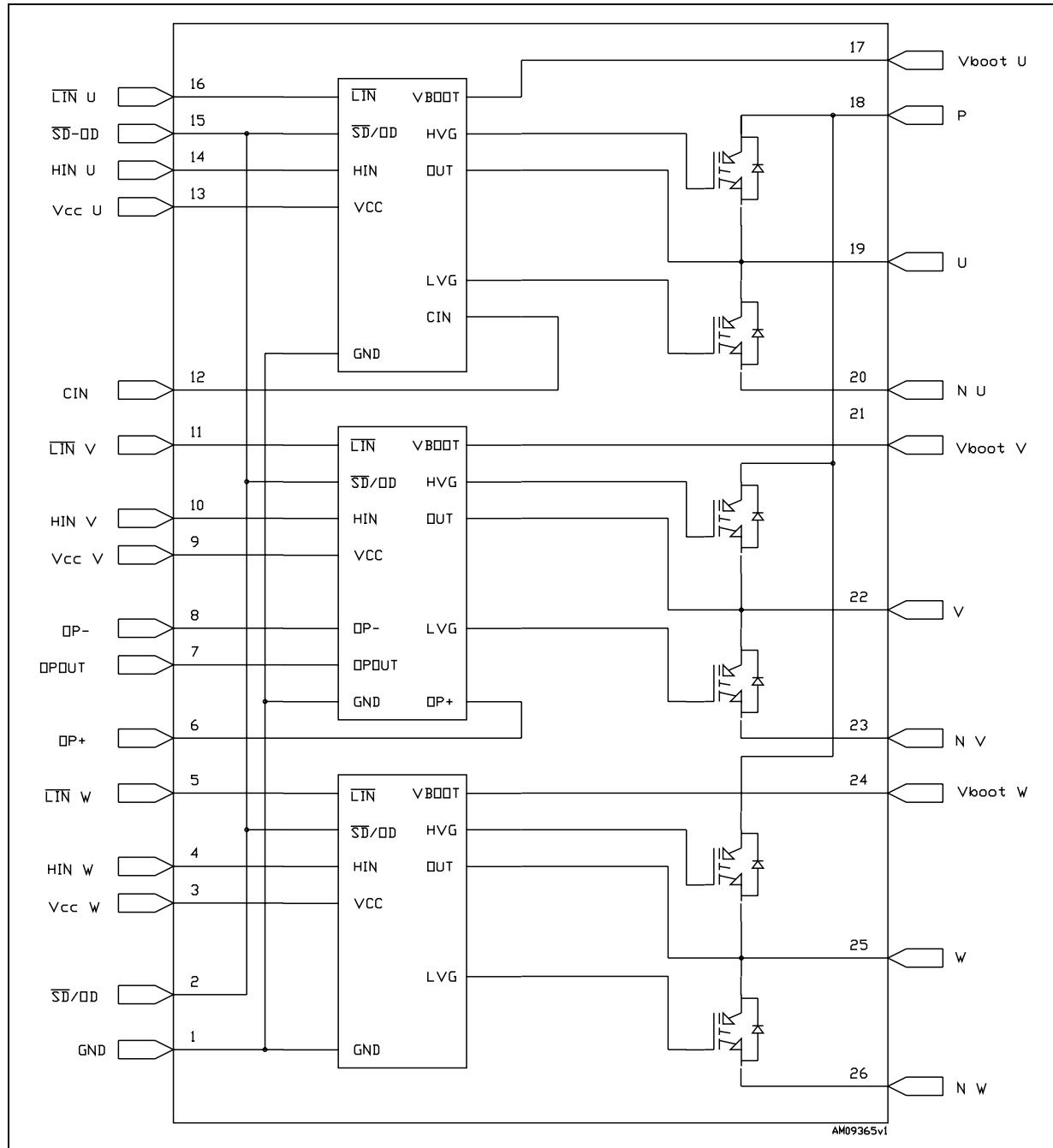
Figure 6.   Internal circuit of the STGIPN3H60

1.4   Absolute maximum ratings

The absolute maximum ratings represent the extreme capability of the device and they can be normally used as a worst limit design condition. It is important to note that the absolute maximum value is given according to a set of testing conditions such us temperature, frequency, voltage, and so on. Device performance can change according to the applied condition.

The SLLIMM-nano specifications are described below using the STGIPN3H60 datasheet as an example. Please refer to the respective product datasheets for a detailed description of all possible types.

Table 2. **Inverter part**

Symbol	Parameter	Value	Unit
V_{CES}	Collector emitter voltage (V_{IN}[(1)] = 0)	600	V
$\pm I_C$[(2)]	Each IGBT continuous collector current at T_C = 25 °C	3	A
$\pm I_C$[(3)]	Each IGBT pulsed collector current	18	A
P_{TOT}	Each IGBT total dissipation at T_C = 25 °C	8	W
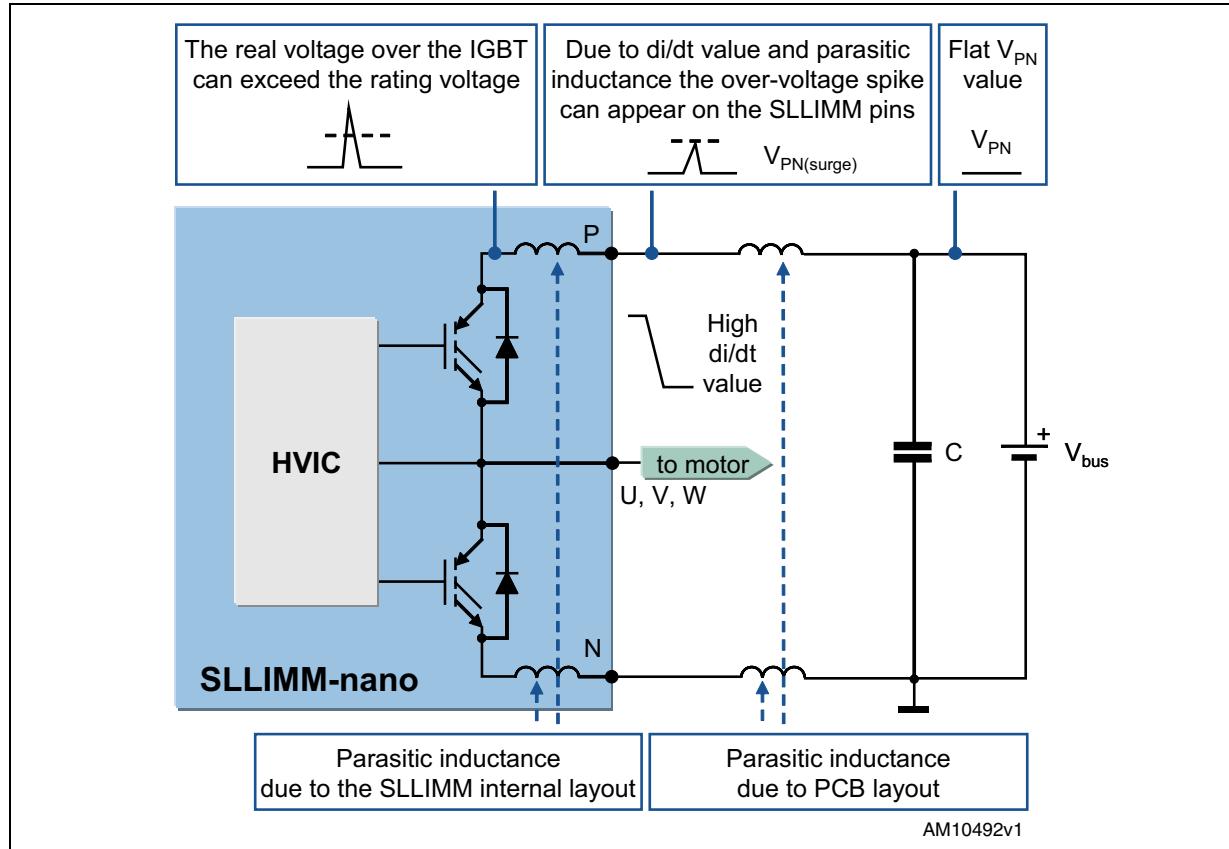
1. Applied between HIN_U, HIN_V, HIN_W; $\overline{LIN}_U$, $\overline{LIN}_V$, $\overline{LIN}_W$ and GND.

2. Calculated according to the iterative *Equation 1*.

3. Pulse width limited by max. junction temperature.

Equation 1

$$I_C(T_C) = \frac{T_{jmax} - T_C}{R_{th(j-c)} \cdot V_{CE(sat)(max)}(@T_{jmax}, I_C(T_C))}$$

● V_{CES}: collector emitter voltage

The power stage of the SLLIMM-nano is based on IGBTs (and freewheeling diodes) having 600 V V_{CES} rating. Generally, considering the intelligent power module internal stray inductances during the commutations, which can generate some surge voltages, the maximum surge voltage between P-N ($V_{PN(surge)}$) allowed is lower than V_{CES}, as shown in *Figure 7*. At the same time, considering also the surge voltage generated by the stray inductance between the device and the DC-link capacitor, the maximum supply voltage (in steady-state) applied between P-N (V_{PN}) must be even lower than $V_{PN(surge)}$. Thanks to the small package size and the lower working current, this phenomenon is less marked in the SLLIMM-nano than in a big intelligent power module.

Figure 7. Stray inductance components of output stage

- $\pm I_C$: each IGBT continuous collector current

The allowable DC current continuously flowing at the collector electrode ($T_C = 25\ °C$). The I_C parameter is calculated according to *Equation 1*.

Table 3. Control part of the STGIPN3H60

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W, and GND (V_{CC} =15 V)	V_{boot} -21 to V_{boot} +0.3	V
V_{CC}	Low voltage power supply	-0.3 to 21	V
V_{CIN}	Comparator input voltage	-0.3 to V_{CC} +0.3	V
V_{OP+}	Op amp non-inverting input	-0.3 to V_{CC} +0.3	V
V_{OP}	Op amp inverting input	-0.3 to V_{CC} +0.3	V
V_{boot}	Bootstrap voltage	-0.3 to 620	V
V_{IN}	Logic input voltage applied between HIN, $\overline{LIN}$ and GND	-0.3 to 15	V
$V_{\overline{SD}/OD}$	Open drain voltage	-0.3 to 15	V
dV_{OUT}/dt	Allowed output slew rate	50	V/ns

- V_{CC}: low voltage power supply

V_{CC} represents the supply voltage of the control part. A local filtering is recommended to enhance the SLLIMM-nano noise immunity. Generally, the use of one electrolytic capacitor (with greater value but not negligible ESR) and one smaller ceramic capacitor (hundreds of nF), faster than the electrolytic one to provide current, is suggested.

Please refer to *Table 4* in order to properly drive the SLLIMM-nano.

Table 4.   Supply voltage and operation behavior

V_{CC} voltage (typ. value)		Operating behavior
STGIPN3H60A	STGIPN3H60	
< 10 V	< 12 V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12 V – 17 V	13.5 V – 18 V	Typical operating conditions
> 18 V	> 21 V	Control circuit is destroyed

Table 5.   Total system

Symbol	Parameter	Value	Unit
T_J	Operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

2 Electrical characteristics and functions

In this section the main electrical characteristics of the power stage are discussed, together with a detailed description of all the SLLIMM-nano functions.

2.1 IGBTs

The SLLIMM-nano achieves power savings in the inverter stage thanks to the use of IGBTs manufactured with the proprietary advanced PowerMESH™ process.
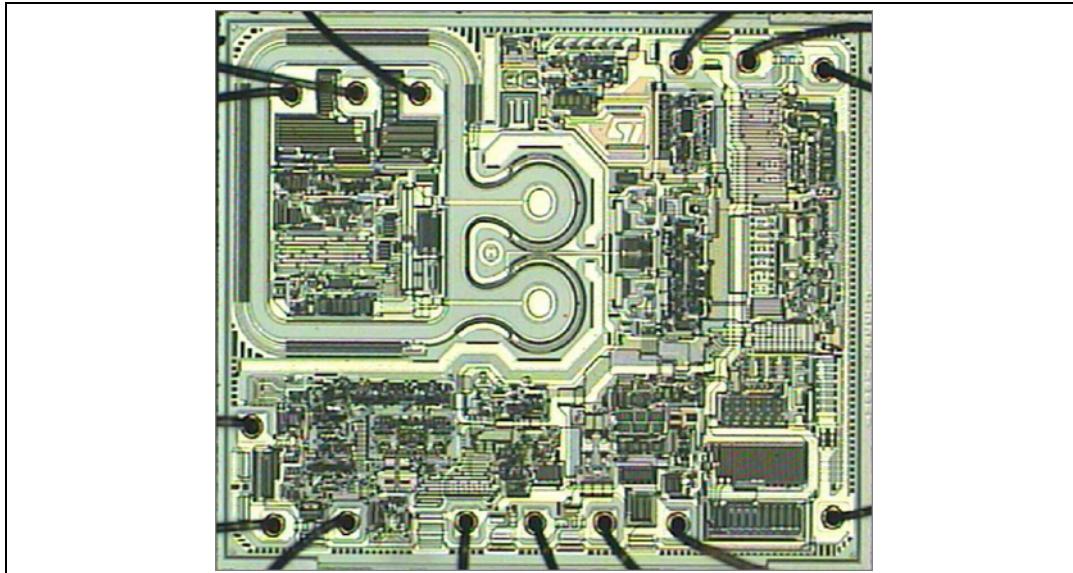
These power devices, optimized for the typical motor control switching frequency, offer an excellent trade-off between voltage drop ($V_{CE(sat)}$) and switching speed (t_{fall}), and therefore minimize the two major sources of energy loss, conduction and switching, reducing the environmental impact of daily-use equipment. A full analysis on the power losses of the complete system in reported in *Section 4: Power losses and dissipation*.

2.2 Freewheeling diodes

Turbo 2 ultrafast high voltage diodes have been adequately selected for the SLLIMM-nano family and carefully tuned to achieve the best t_{rr}/VF trade-off and softness as freewheeling diodes in order to further improve the total performance of the inverter and significantly reduce the electromagnetic interference (EMI) in the motor control applications which are quite sensitive to this phenomena.
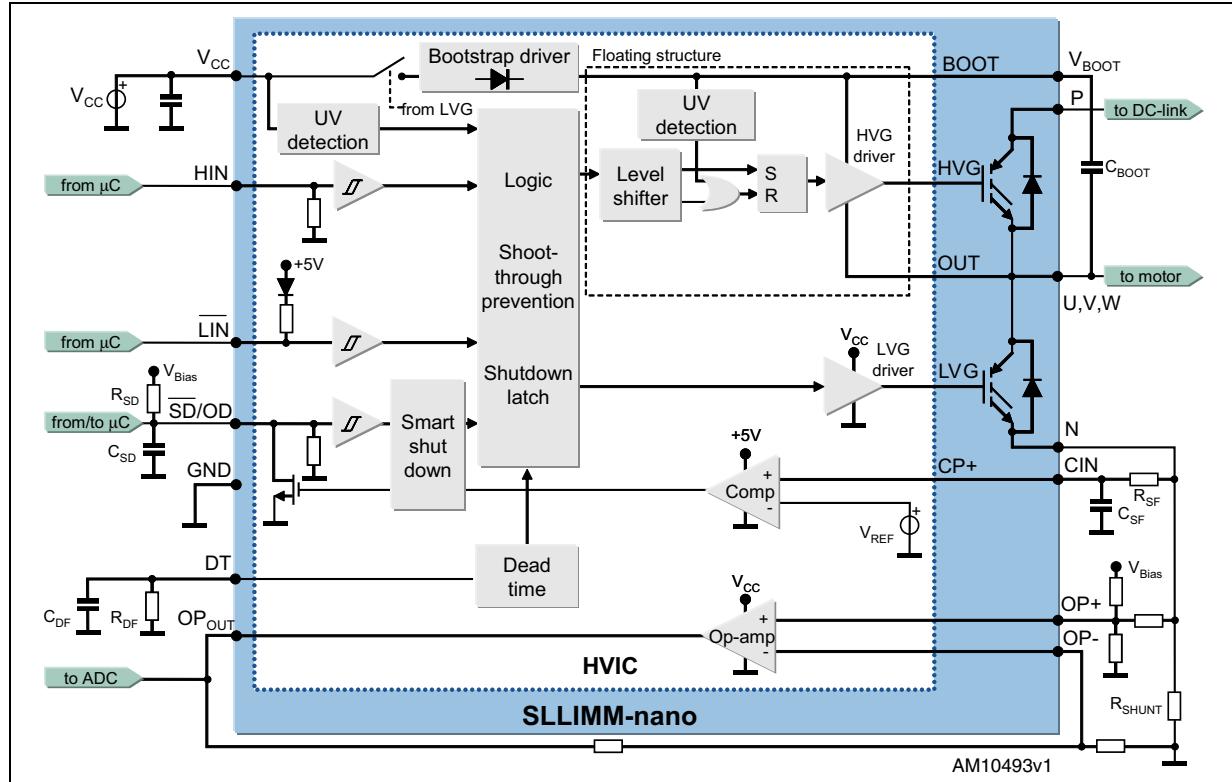
2.3 High voltage gate drivers

The SLLIMM-nano is equipped with a versatile high voltage gate driver IC (HVIC), designed using BCD offline (Bipolar, CMOS, and DMOS) technology (see *Figure 8*) and particularly suited to field oriented control (FOC) motor driving applications, able to provide all the functions and current capability necessary for high-side and low-side IGBT driving. This driver can be used in all applications where high voltage shifted control is necessary and it includes a patented internal circuitry which replaces the external bootstrap diode.

Figure 8.   High voltage gate drive die image

Each high voltage gate driver chip controls two IGBTs in half bridge topology, offering basic functions such as dead time, interlocking, integrated bootstrap diode, and also advanced features such as smart shutdown (patented), fault comparator, and a dedicated high performance op amp for advanced current sensing. A schematic summary of the features by device are listed in *Table 1*.

In this application note the main characteristics of a high voltage gate drive related to the SLLIMM-nano are discussed. For a greater understanding, please refer to the AN2738 application note.

Figure 9.   **High voltage gate driver block diagram**

2.3.1 Logic inputs

The high voltage gate driver IC has two logic inputs, HIN and LIN, to separately control the high-side and low-side outputs, HVG and LVG. Please refer to *Table 1* for the input signal logics by device.

In order to prevent any cross conduction between high-side and low-side IGBT, a safety time (dead time) is introduced (see *Section 2.3.4: Dead time and interlocking function management* for further details).

All the logic inputs are provided with hysteresis (~1 V) for low noise sensitivity and are TTL/CMOS 3.3 V compatible. Thanks to this low voltage interface logic compatibility, the SLLIMM-nano can be used with any kind of high performance controller, such as microcontrollers, DSPs or FPGAs.

As shown in the block diagrams of *Figure 10* and *Figure 11*, the logic inputs have internal pull-down (or pull-up) resistors in order to set a proper logic level in the case of interruption in the logic lines. If logic inputs are left floating, the gate driver outputs LVG and HVG are set to low level. This simplifies the interface circuit by eliminating the six external resistors, therefore, saving cost, board space and number of components.

Figure 10. Logic input configuration for the STGIPN3H60A

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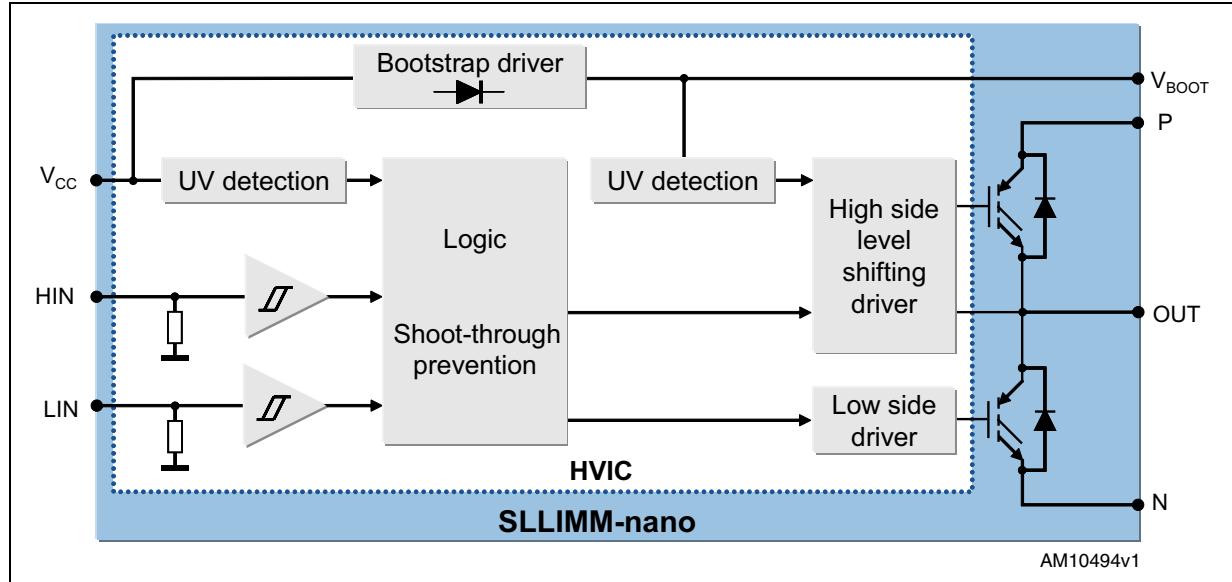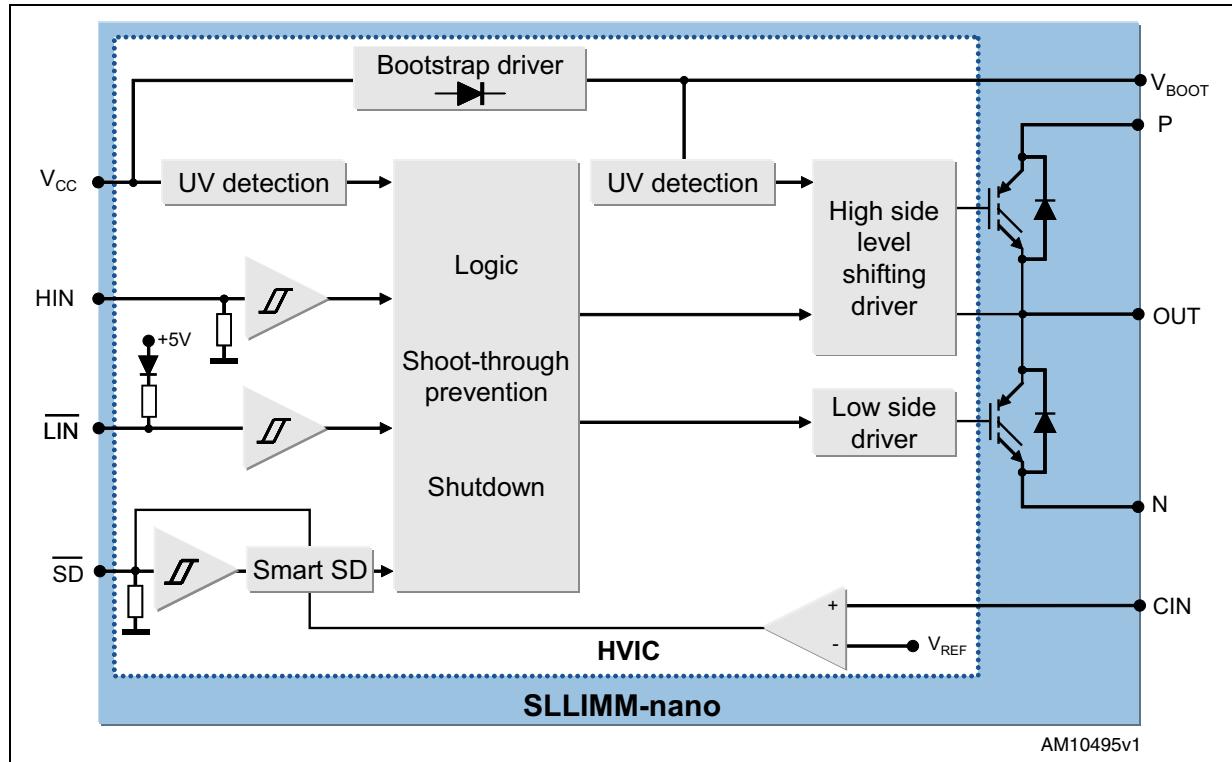
Figure 11. Logic input configuration for the STGIPN3H60

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The typical values of the integrated pull-up/down resistors are shown in *Table 6*:

Table 6.   Integrated pull-up/down resistor values

Input pin	PN	Input pin logic	Internal pull-up	Internal pull-down
High-side gate driving HIN_U, HIN_V, HIN_W	STGIPN3H60A	Active high		500 kΩ
Low-side gate driving LIN_U, LIN_V, LIN_W	STGIPN3H60A	Active high		500 kΩ
High-side gate driving HIN_U, HIN_V, HIN_W	STGIPN3H60	Active high		85 kΩ
Low-side gate driving $\overline{LIN}_U$, $\overline{LIN}_V$, $\overline{LIN}_W$	STGIPN3H60	Active low	720 kΩ	
$\overline{SD}$ / OD shutdown	STGIPN3H60	Active low		125 kΩ

2.3.2   High voltage level shift

The built-in high voltage level shift allows direct connection between the low voltage control inputs and the high voltage power half bridge in any power application up to 600 V. It is obtained thanks to the BCD offline technology which integrates, in the same die bipolar devices, low and medium voltage CMOS for analog and logic circuitry and high voltage DMOS transistors with a breakdown voltage in excess of 600 V. This key feature eliminates the need for external optocouplers, resulting in significant savings regarding component count and power losses. Other advantages are high-frequency operation and short input-to-output delays.
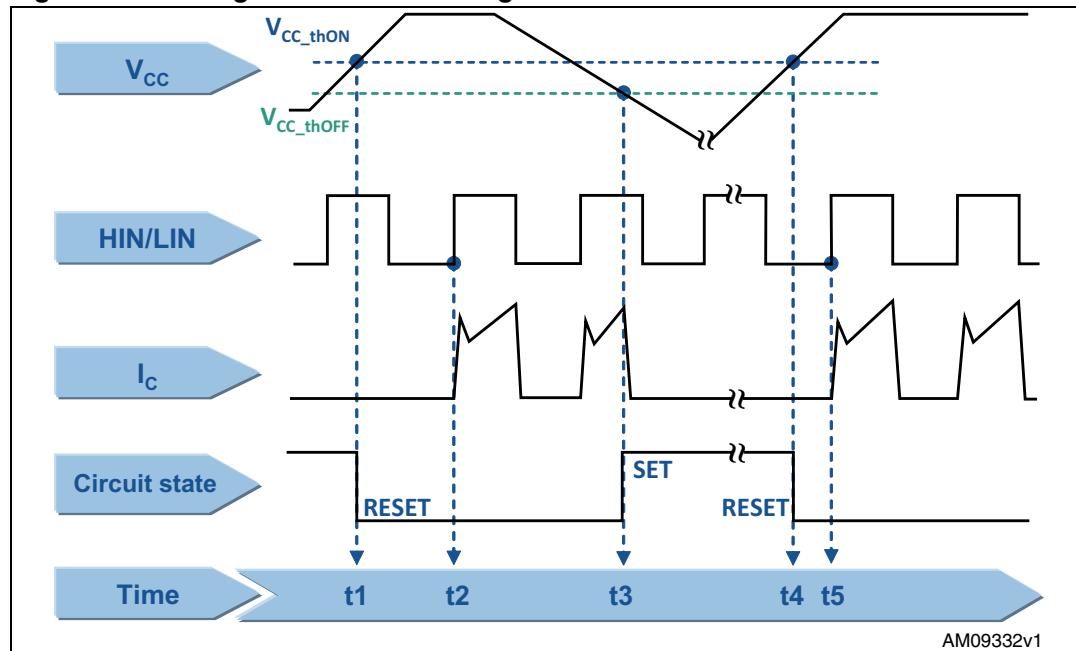
2.3.3   Undervoltage lockout

The SLLIMM-nano supply voltage V_{CC} is continuously monitored by an undervoltage lockout (UVLO) circuitry which turns off the gate driver outputs when the supply voltage goes below the V_{CC_thOFF} threshold specified on the datasheet, and turns on the IC when the supply voltage goes above the V_{CC_thON} voltage. A hysteresis of about 1.5 V is provided for noise rejection purposes. The high voltage floating supply Vboot is also provided with a similar undervoltage lockout circuitry. When the driver is in UVLO condition, both gate driver outputs are set to low level, setting the half bridge power stage output to high impedance.

The timing chart of undervoltage lockout, plotted in *Figure 12*, is based on the following steps:

● t1: when the V_{CC} supply voltage raises the V_{CC_thON} threshold, the gate driver starts to work after the next input signal HIN/LIN is on. The circuit state becomes RESET

● t2: input signal HIN/LIN is on and the IGBT is turned on

● t3: when the V_{CC} supply voltage goes below the V_{CC_thOFF} threshold, the UVLO event is detected. The IGBT is turned off in spite of input signal HIN/LIN. The state of the circuit is now SET

● t4: the gate driver re-starts once the V_{CC} supply voltage again raises the V_{CC_thON} threshold

● t5: input signal HIN/LIN is on and the IGBT is turned on again.

Figure 12. Timing chart of undervoltage lockout function

2.3.4 Dead time and interlocking function management

In order to prevent any possible cross-conduction between high-side and low-side IGBTs, the SLLIMM-nano provides both the dead time and the interlocking function. The interlocking function is a logic operation which sets both the outputs to low level when the inputs are simultaneously active. The dead time function is a safety time introduced by the device between the falling edge transition of one driver output and the rising edge of the other output. If the rising edge set externally by the user occurs before the end of this dead time, it is ignored and results as delayed until the end of the dead time.

Table 7. Interlocking function truth table of the STGIPN3H60A

Condition	Logic input (V_I)		Outputs	
	LIN	HIN	LVG	HVG
Interlocking half bridge tri-state	H	H	L	L
0 "logic state" half bridge tri-state	L	L	L	L
1 "logic state" low-side direct driving	H	L	H	L
1 "logic state" high-side direct driving	L	H	L	H
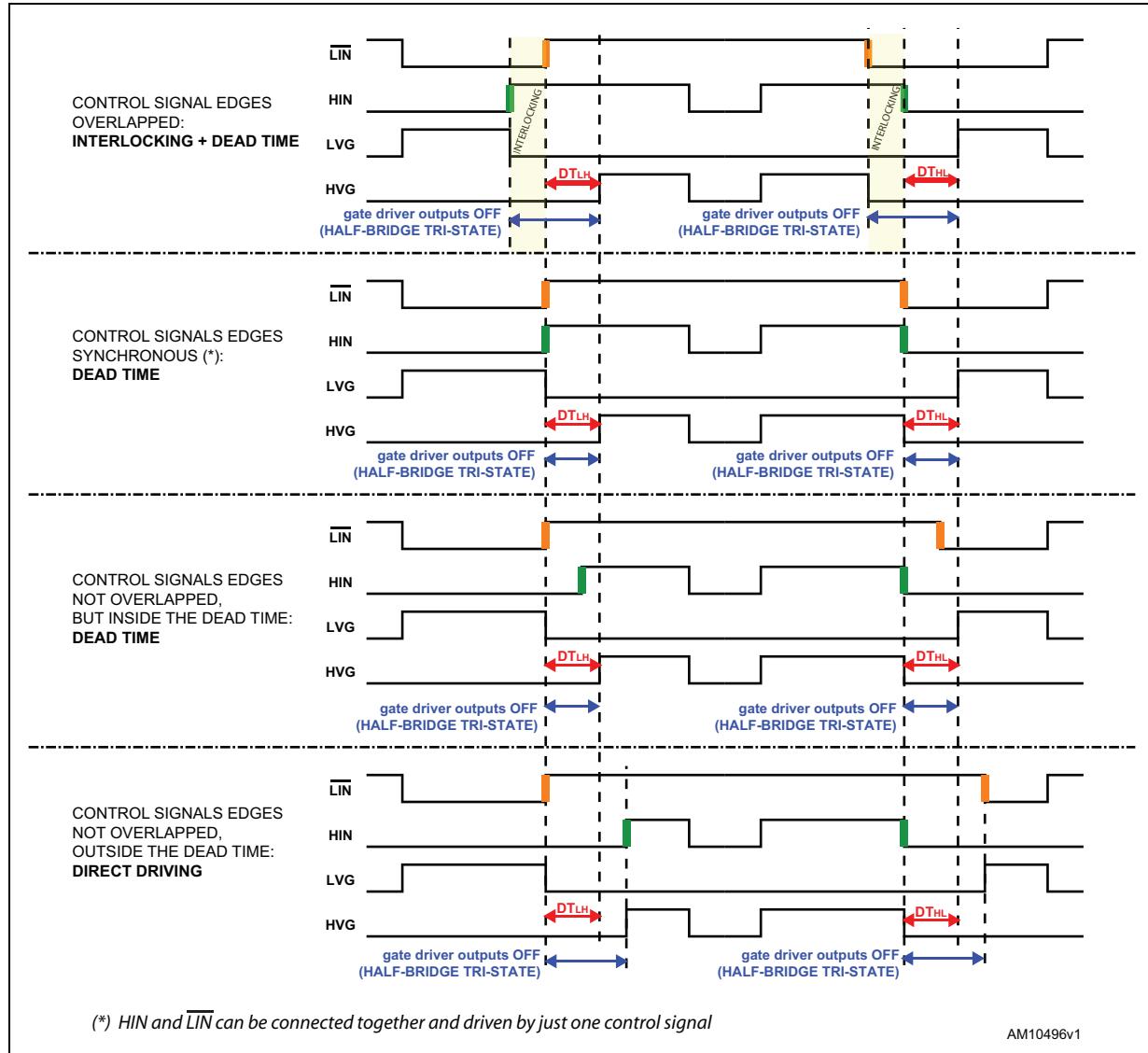
The dead time is internally set at 320 ns as the typical value of the STGIPN3H60A.

Table 8.   Interlocking function truth table of the STGIPN3H60

Condition	Logic input (V_I)			Outputs	
	$\overline{SD}$	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half bridge tri-state	L	X	X	L	L
Interlocking half bridge tri-state	H	L	H	L	L
0 "logic state" half bridge tri-state	H	H	L	L	L
1 "logic state" low-side direct driving	H	L	L	H	L
1 "logic state" high-side direct driving	H	H	H	L	H

Note: *X: not important.*

The dead time is internally set at 180 ns as typical value. In *Figure 13* the details of dead time and interlocking function management of the STGIPN3H60 is described.

Figure 13. Timing chart of dead time function

(*) HIN and $\overline{\text{LIN}}$ can be connected together and driven by just one control signal

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2.3.5 Comparators for fault sensing

The SLLIMM-nano STGIPN3H60 integrates one comparator intended for advanced fault protection, such as overcurrent, overtemperature or any other type of fault measurable via a voltage signal. The comparator has an internal reference voltage V_{REF}, specified in the datasheet, on its inverting input (see *Figure 9*), while the non-inverting input is available on the C_{IN} pin. The comparator input can be connected to an external shunt resistor, in order to implement a simple overcurrent or short-circuit detection function, as discussed in detail in *Section 2.3.6: Short-circuit protection and smart shutdown function*.

2.3.6 Short-circuit protection and smart shutdown function

The fully featured version of the SLLIMM-nano (STGIPN3H60) is able to monitor the output current and provide protection against overcurrent and short-circuit conditions in a very short time (comparator triggering to high/low-side driver turn-off propagation delay t_{isd} = 200 ns), thanks to the smart shutdown function. This feature is based on an innovative patented circuitry which provides an intelligent fault management operation and greatly reduces the protection intervention delay independently on the protection time duration which can be set as desired by the device user.
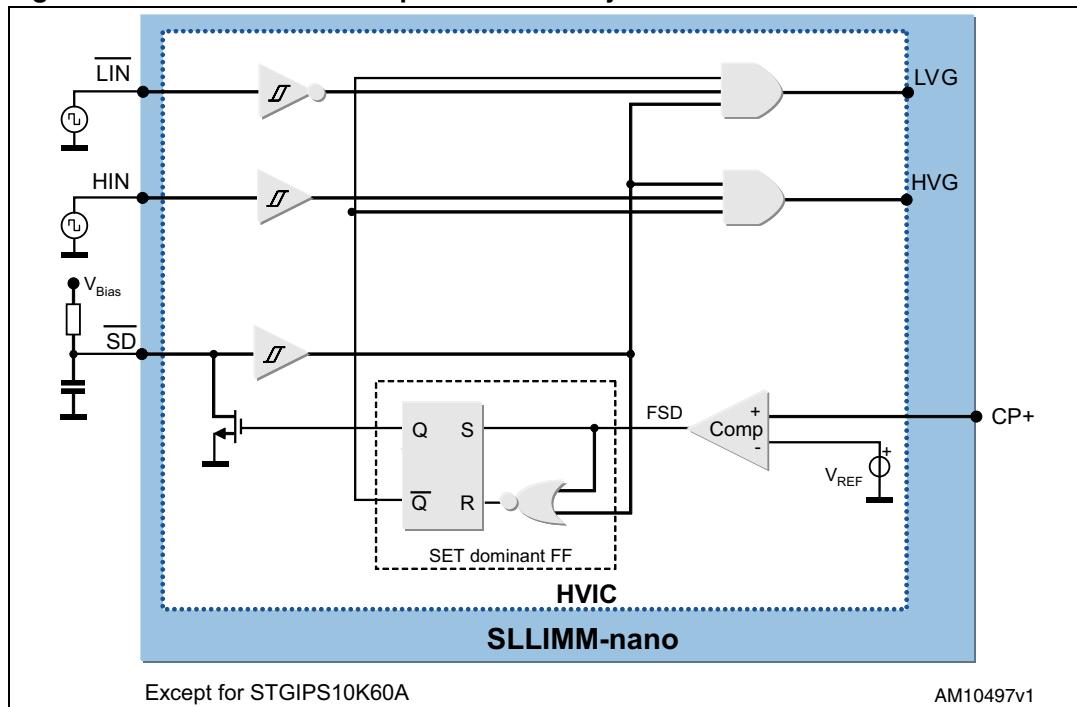
As already mentioned in *Section 2.3.5: Comparators for fault sensing* and as shown in *Figure 9*, the comparator input can be connected to an external shunt resistor, R_{SHUNT}, in order to implement a simple overcurrent detection function. An RC filter network (R_{SF} and C_{SF}) is necessary to prevent erroneous operation of the protection. The output signal of the comparator is fed to an integrated MOSFET with the open drain available on the $\overline{SD}$ / OD pin, shared with the $\overline{SD}$ input. When the comparator triggers, the device is set in shutdown state and all its outputs are set to low level, leaving the half bridge in tri-state. In common overcurrent protection architectures, the comparator output is usually connected to the SD input and an external RC network (R_{SD} and C_{SD}) is connected to this $\overline{SD}$ / OD line in order to provide a mono-stable circuit which implements a protection time when a fault condition occurs.

Contrary to common fault detection systems, the new smart shutdown structure allows an immediate turn-off of the output gate driver in the case of fault, without waiting for the external capacitor to be discharged. This strategy minimizes the propagation delay between the fault detection event and the actual outputs switch-off. In fact, the time delay between the fault and outputs disabling is not dependent on the RC value of the external SD circuitry but, thanks to the new architecture, has a preferential path internally in the driver. Then the device immediately turns off the driver outputs and latches the turn-on of the open drain switch, until the SD signal has reached its lower threshold. After the SD signal goes below the lower threshold, the open drain is switched off (see *Figure 15*).

The smart shutdown system provides the possibility to increase the value of the external RC network across the SD pin (sized to fix the disable time generated after the fault event) as much as desired by the user without compromising the intervention time delay of the SLLIMM-nano protection.

A block diagram of the smart shutdown architecture is depicted in *Figure 14*.

Figure 14. Smart shutdown equivalent circuitry

In normal operation the outputs follow the commands received from the respective input signals.

When a fault detection event occurs, the fault signal (FSD) is set to HIGH by the fault detection circuit output and the FF receives a SET input signal. Consequently, the FF outputs set the SLLIMM-nano output signals to low level and, at the same time, turn on the open drain MOSFET which works as active pull-down for the $\overline{SD}$ signal. Note that the gate driver outputs stay at low level until the $\overline{SD}$ pin has experienced both a falling edge and a rising edge, although the fault signal may be returned to low level immediately after the fault sensing. In fact, even if the FF is reset by the falling edge of the $\overline{SD}$ input, the $\overline{SD}$ signal also works as enable for the outputs, thanks to the two AND ports. Moreover, once the internal open drain transistor has been activated, due to the latch, it cannot be turned off until the $\overline{SD}$ pin voltage reaches the low logic level. Note that, since the FF is SET dominant, oscillations of the $\overline{SD}$ pin are avoided if the fault signal remains steady at a high level.

2.3.7 Timing chart of short-circuit protection and smart shutdown function

With reference to *Figure 15*, the short-circuit protection is based on the following steps:

● t1: when the output current is lower than the max. allowed level, the SLLIMM-nano is working in normal operation

● t2: when the output current reaches the max. allowed level (I_{SC}), the overcurrent/short-circuit event is detected and the protection is activated.
The voltage across the shunt resistor, and then on the C_{IN} pin, exceeds the V_{REF} value, the comparator triggers, setting the device in shutdown state and both its outputs are set to low level leading the half bridge in tri-state.
The smart shutdown switches off the IGBT gate (HVG, LVG) through a preferential path (200 ns as typical internal delay time) and, at the same time, it switches on the M1 internal MOSFET. The SD signal starts the discharge phase and its value drops with a time constant τ_A. The time constant τ_A value is given by:

Equation 2
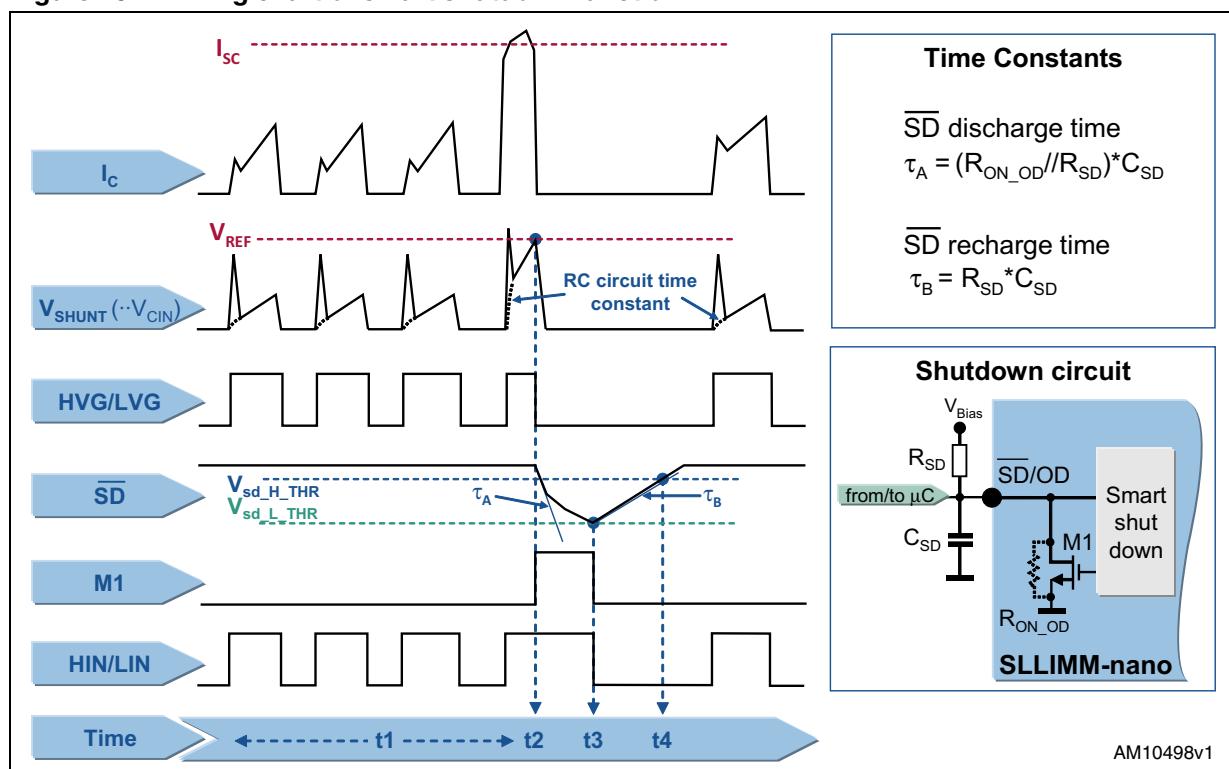
$$\tau_A = (R_{ON\_OD} // R_{SD}) \cdot C_{SD}$$

● t3: the SD signal reaches the lower threshold $V_{sd\_L\_THR}$ and the control unit switches off the input HIN and LIN. The smart shutdown is disabled (M1 off) and SD can rise up with a time constant τ_B, given by:

Equation 3

$$\tau_B = R_{SD} \cdot C_{SD}$$

● t4: when the SD signal reaches the upper threshold $V_{sd\_H\_THR}$, the system is re-enabled.

Figure 15.   Timing chart of smart shutdown function

2.3.8   Current sensing shunt resistor selection

As previously discussed, the shunt resistors R_{SHUNT} externally connected between the N pin and ground (see *Figure 9*) are used to realize the overcurrent detection.

When the output current exceeds the short-circuit reference level (I_{SC}), the C_{IN} signal overtakes the V_{REF} value and the short-circuit protection is active. For a reliable and stable operation the current sensing resistor should be a high quality, low tolerance non-inductive type. In fact, stray inductance in the circuit, which includes the layout, the RC filter, and also the shunt resistor, must be minimized in order to avoid undesired short-circuit detection.

For these reasons, the shunt resistor and the filtering components must be placed as close as possible to the SLLIMM-nano pins, for additional suggestions refer to *Section 5.1: Layout suggestions*.

The value of the current sense resistor can be calculated by following different guidelines, functions of the design specifications, or requirements. A common criterion is presented here based on the following steps:

● Defining of the overcurrent threshold value (I_{OC_th}). For example, it can be fixed considering the IGBT typical working current in the application and adding 20-30% as overcurrent.

● Calculation of the shunt resistor value according to the conditioning network. An example of the conditioning network is shown in *Figure 19*. Further details can be found in the user manuals listed (see *References* 5 and *References* 6).

● Selection of the closest shunt resistor commercial value.

● Calculation of the power rating of the shunt resistor, taking into account that this parameter is strongly temperature dependent. Therefore, the power derating ratio of the shunt resistor, $\Delta P(T)\%$, shown in the manufacturer's datasheet, must be considered in the calculation as follows:

Equation 4

$$P_{SHUNT}(T) = \frac{R_{SHUNT} \cdot I_{RMS}^2}{\Delta P(T)\%}$$
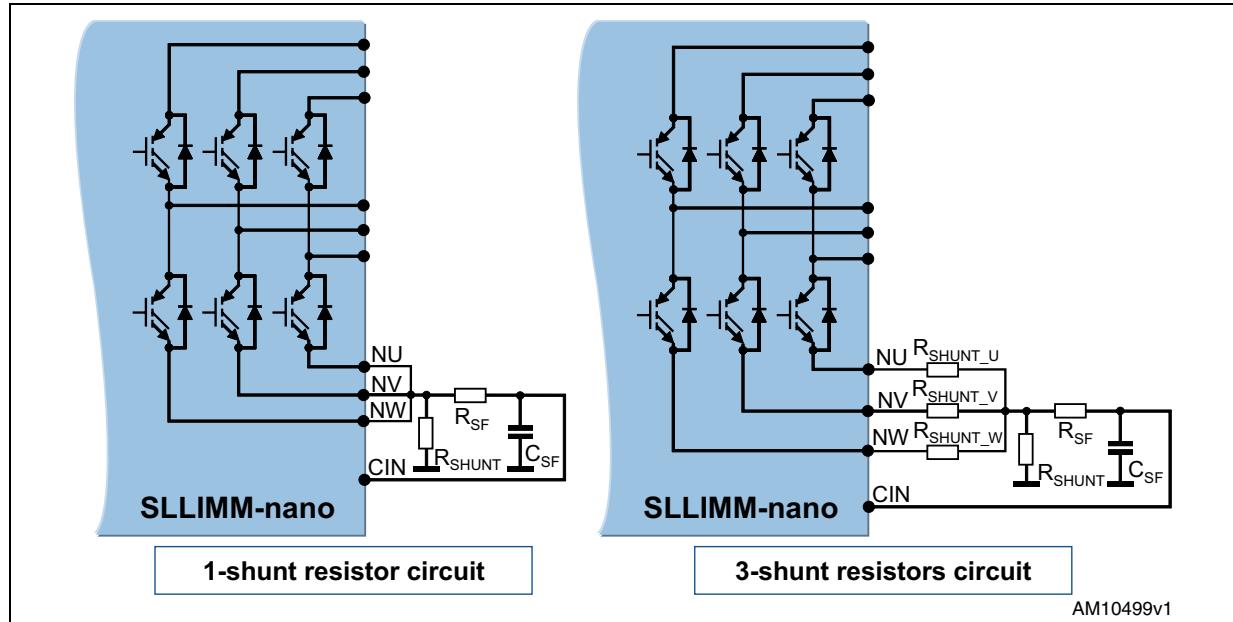
where I_{RMS} is the IGBT RMS working current.

For a proper selection of the shunt resistor, a safety margin of at least 30% is recommended on the calculated power rating.

2.3.9 RC filter network selection

Two options of shunt (1- or 3-shunt) resistor circuit can be adopted in order to implement different control techniques and short-circuit protection, as shown in *Figure 16*.

Figure 16. Examples of SC protection circuit

An RC filter network is required to prevent undesired short-circuit operation due to the noise on the shunt resistor.

Both solutions allow to detect the total current in all three phases of the inverter. The filter is based on the R_{SF} and C_{SF} network and its time constant is given by:

Equation 5

$$t_{SF} = R_{SF} \cdot C_{SF}$$

In addition to the RC time constant, the turn-off propagation delay of the gate driver, t_{isd} (specified in the datasheet) and the IGBT turn-off time (in the range of tens of ns), must be considered in the total delay time (t_{Total}), which is the time necessary to completely switch off the IGBT once the short-circuit event is detected. Therefore, the t_{Total} is calculated as follows:

Equation 6

$$t_{Total} = t_{SF} + t_{isd} + t_{off}$$
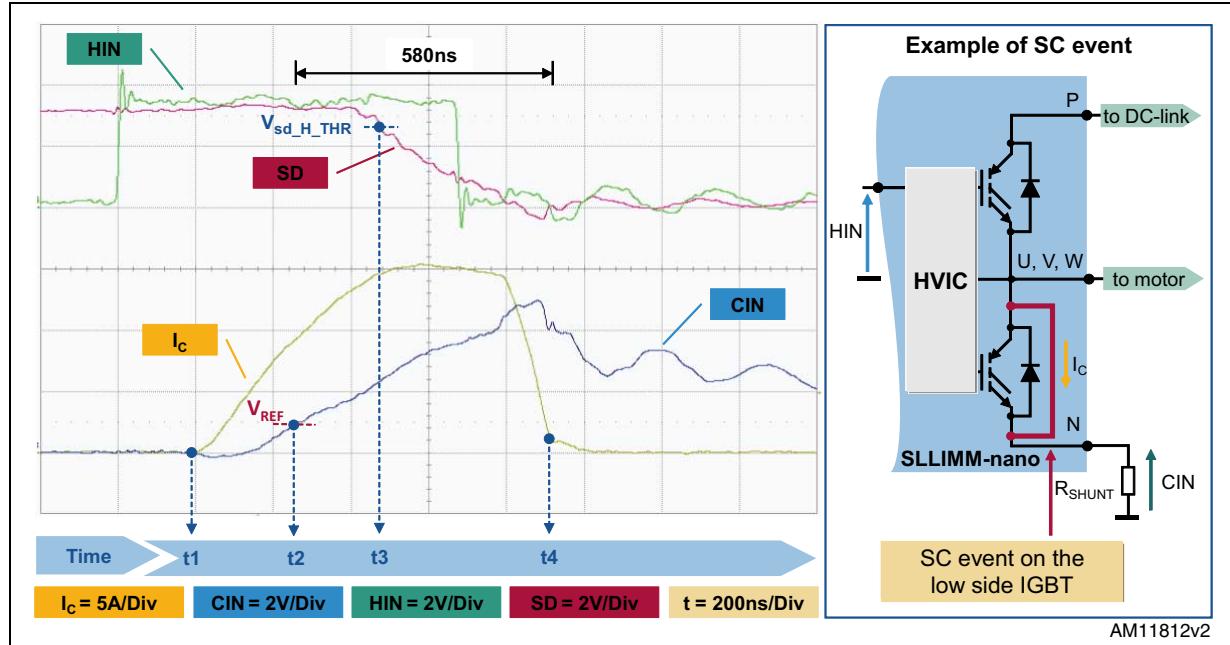
and the t_{SF} is recommended to be set in the range of 1~2 µs.

In the case of a 3-shunt resistor circuit, a specific control technique can be implemented by using the three shunt resistors (R_{SHUNT_U}, R_{SHUNT_V} and R_{SHUNT_W}) able to monitor each phase current.

An example of a short-circuit event is shown in *Figure 17*, where it is possible to note the very fast protection, thanks to the smart shutdown function, against fault events. The main steps are:

● t1: collector current IC starts to rise. SC event is not detected yet due to the RC network on the C_{IN} pin.

● t2: voltage on V_{CIN} reaches the V_{REF}. SC event is detected and the smart shutdown starts to turn off the SLLIMM-nano.

● t3: the SD in activated.

● t4: the SLLIMM-nano is definitively turned off in 580 ns (including the $t_{d(off)}$ time of IGBT) from SC detection.
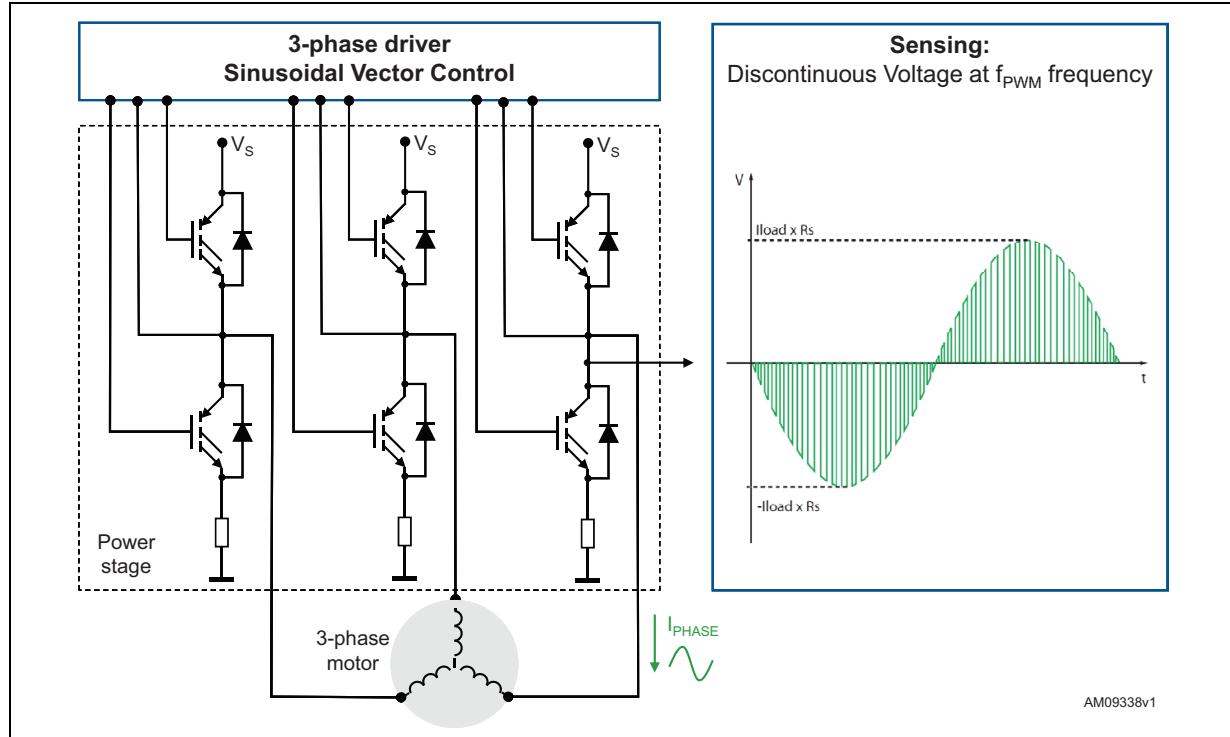
Finally, the total disable time is t4-t2 and the total SC action time is t4-t1.

Figure 17. Example of SC event

2.3.10 Op amps for advanced current sensing

The fully featured version of the SLLIMM-nano (STGIPN3H60) integrates also one operational amplifier optimized for field oriented control (FOC) applications. In a typical FOC application the currents in the three half bridges are sensed using a shunt resistor. The analog current information is transformed into a discontinuous sense voltage signal, having the same frequency as the PWM signal driving the bridge. The sense voltage is a bipolar analog signal, whose sign depends on the direction of the current (see *Figure 18*):
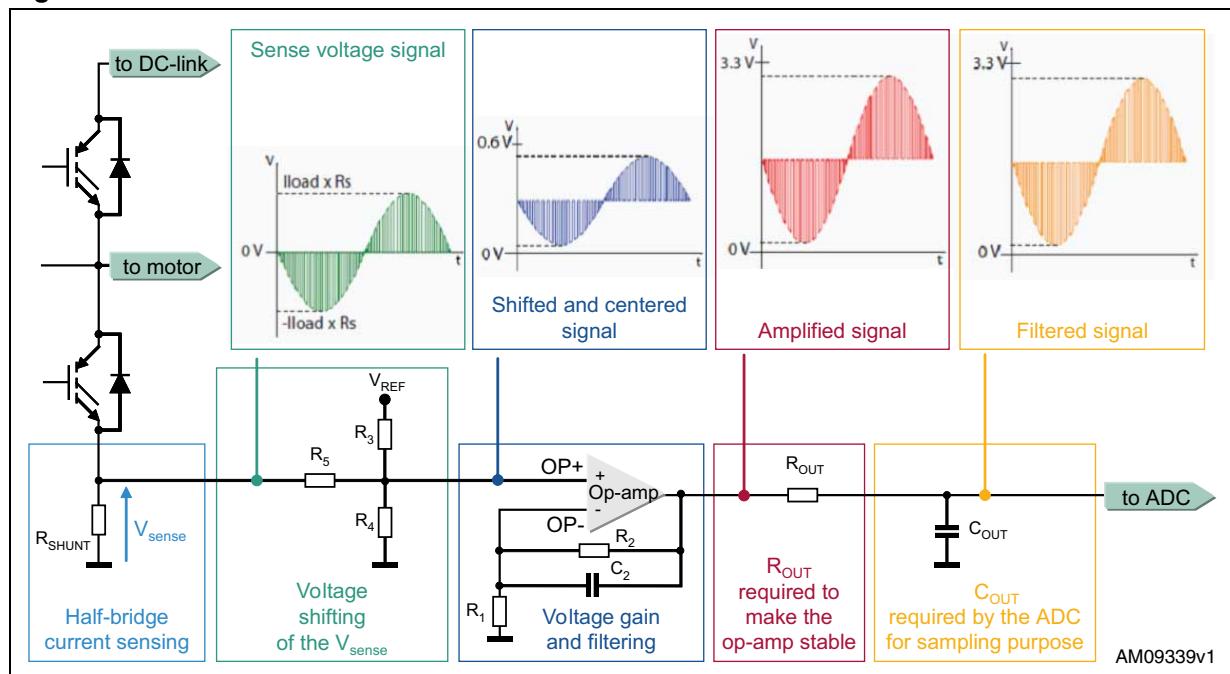
Figure 18. 3-phase system

The sense voltage signals must be provided to an A-D converter. They are usually shifted and amplified by dedicated op amps in order to exploit the full range of the A-D converter. The typical scheme and principle waveforms are shown in *Figure 19*:

Figure 19. General advanced current sense scheme and waveforms

ADCs used in vector control applications have a typical full scale range (FSR) of about 3.3 V. The sense signals must be shifted and centered on FSR/2 voltage (about 1.65 V) and amplified with a gain which provides the matching between the maximum value of the sensed signal and the FSR of the ADC. Some typical examples of sense network sizing can be found in the user manuals listed (see *References* 5 and *References* 6).
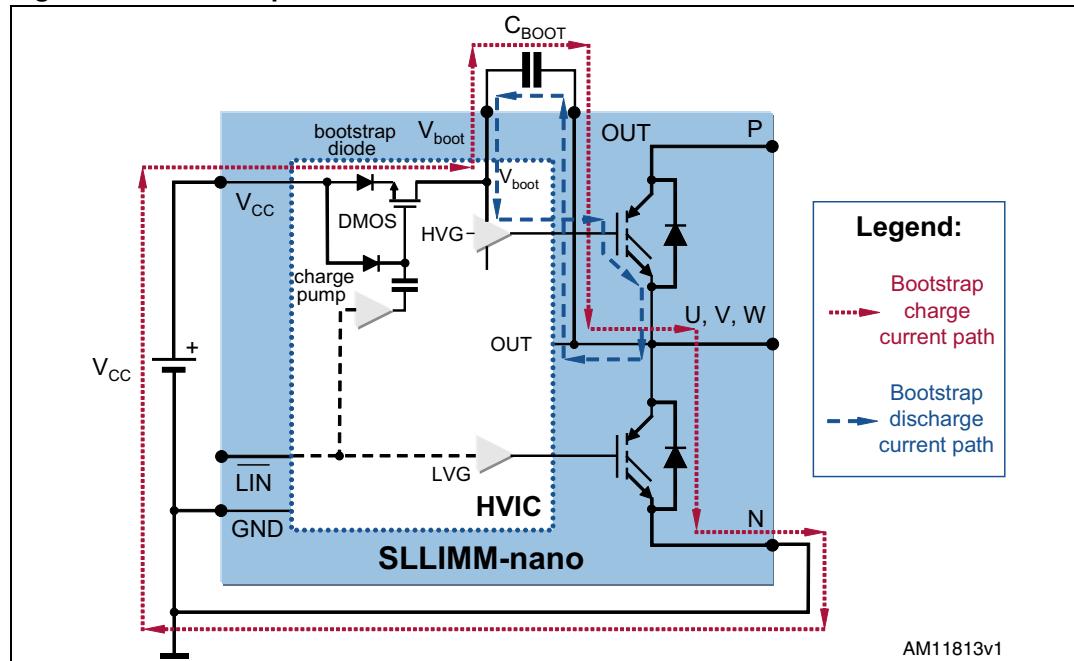
2.3.11 Bootstrap circuit

In the 3-phase inverter the emitters of the low-side IGBTs are connected to the negative DC bus (V_{DC-}) as common reference ground, which allows all low-side gate drivers to share the same power supply, while, the emitter of high-side IGBTs is alternately connected to the positive (V_{DC+}) and negative (V_{DC-}) DC bus during the running conditions.

A bootstrap method is a simple and cheap solution to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode. The SLLIMM-nano family includes a patented integrated structure that replaces the external diode. It is realized with a high voltage DMOS driven synchronously with the low-side driver (LVG) and a diode in series. An internal charge pump provides the DMOS driving voltage.

The operation of the bootstrap circuit is shown in *Figure 20*. The floating supply capacitor C_{BOOT} is charged, from the V_{CC} supply, when the V_{OUT} voltage is lower than the V_{CC} voltage (e.g. low-side IGBT is on), through the bootstrap diode and the DMOS path with reference to the "bootstrap charge current path". During the high-side IGBT ON phase, the bootstrap circuit provides the right gate voltage to properly drive the IGBT (see "bootstrap discharge current path"). This circuit is iterated for all the three half bridges.

Figure 20. Bootstrap circuit

The value of the C_{BOOT} capacitor should be calculated according to the application condition and must take the following into account:

● voltage across C_{BOOT} must be maintained at a value higher than the undervoltage lockout level for the IC driver. This enables the high-side IGBT to work with a correct gate voltage (lower dissipation and better overall performances). Please consider that if

a voltage below the UVLO threshold is applied on the bootstrap channel, the IC disables itself (no output) without any fault signal.

● the voltage across C_{BOOT} is affected by different components such as drop across the integrated bootstrap structure, drop across the low-side IGBT, and others.

● when the high-side IGBT is on, the C_{BOOT} capacitor discharges mainly to provide the right IGBT gate charge but other phenomena must be considered such as leakage currents, quiescent current, etc.

2.3.12 Bootstrap capacitor selection

A simple method to properly size the bootstrap capacitor considers only the amount of charge that is needed when the high voltage side of the driver is floating and the IGBT gate is driven once. This approach does not take into account either the duty cycle of the PWM, or the fundamental frequency of the current. Observations on PWM duty cycle, the kind of modulation (6-step, 12-step and sine-wave) must be considered with their own peculiarity to achieve the best bootstrap circuit sizing.

During the bootstrap capacitor charging phase, the low-side IGBT is on and the voltage across C_{BOOT} (V_{CBOOT}) can be calculated as follows:

Equation 7

$$V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{CE(sat)max}$$

where:

V_{CC}: supply voltage of gate driver.

V_F: bootstrap diode forward voltage drop.

$V_{CE(sat)max}$: maximum emitter collector voltage drop of low-side IGBT.

$V_{RDS(on)}$: DMOS voltage drop.

The dimension of the bootstrap capacitance C_{BOOT} value is based on the minimum voltage drop (ΔV_{CBOOT}) to guarantee when the high-side IGBT is on, and must be:

Equation 8

$$\Delta V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{GE(min)} - V_{CE(sat)max}$$

under the condition:

Equation 9

$$V_{CBOOT(min)} > V_{BS\_thON}$$

where:

$V_{GE(min)}$: minimum gate emitter voltage of high-side IGBT.

V_{BS_thON}: bootstrap turn-on undervoltage threshold (maximum value, see datasheet).

Considering the factors contributing to V_{CBOOT} decreasing, the total charge supplied by the bootstrap capacitor (during high-side ON phase) is:

Equation 10

$$Q_{TOT} = Q_{GATE} + \left(I_{LKGE} + I_{QBO} + I_{LK} + I_{LKDiode} + I_{LKCap}\right) \cdot t_{Hon} + Q_{LS}$$

where:

Q_{GATE}: total IGBT gate charge.

I_{LKGE}: IGBT gate emitter leakage current.

I_{QBO}: bootstrap circuit quiescent current.

I_{LK}: bootstrap circuit leakage current.

$I_{LKDiode}$: bootstrap diode leakage current.

I_{LKCap}: bootstrap capacitor leakage current (relevant when using an electrolytic capacitor but can be ignored if other types of capacitors are used).

t_{Hon}: high-side ON time.

Q_{LS}: charge required by the internal level shifters.
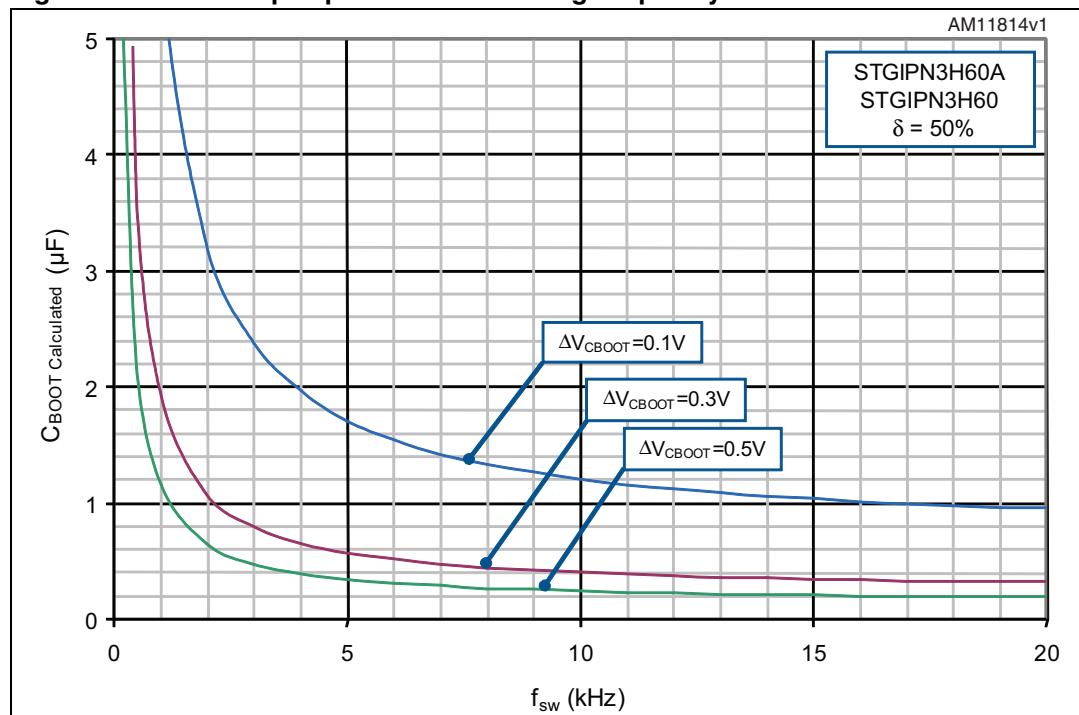
Finally, the minimum size of the bootstrap capacitor is:

Equation 11

$$C_{BOOT} = \frac{Q_{TOT}}{\Delta V_{CBOOT}}$$

For an easier selection of bootstrap capacitor, *Figure 21* shows the behavior of C_{BOOT} (calculated) versus switching frequency (f_{sw}), with different values of ΔV_{CBOOT}, corresponding to *Equation 11 Equation 11* for a continuous sinusoidal modulation and a duty cycle δ = 50%.

Figure 21. Bootstrap capacitor vs. switching frequency
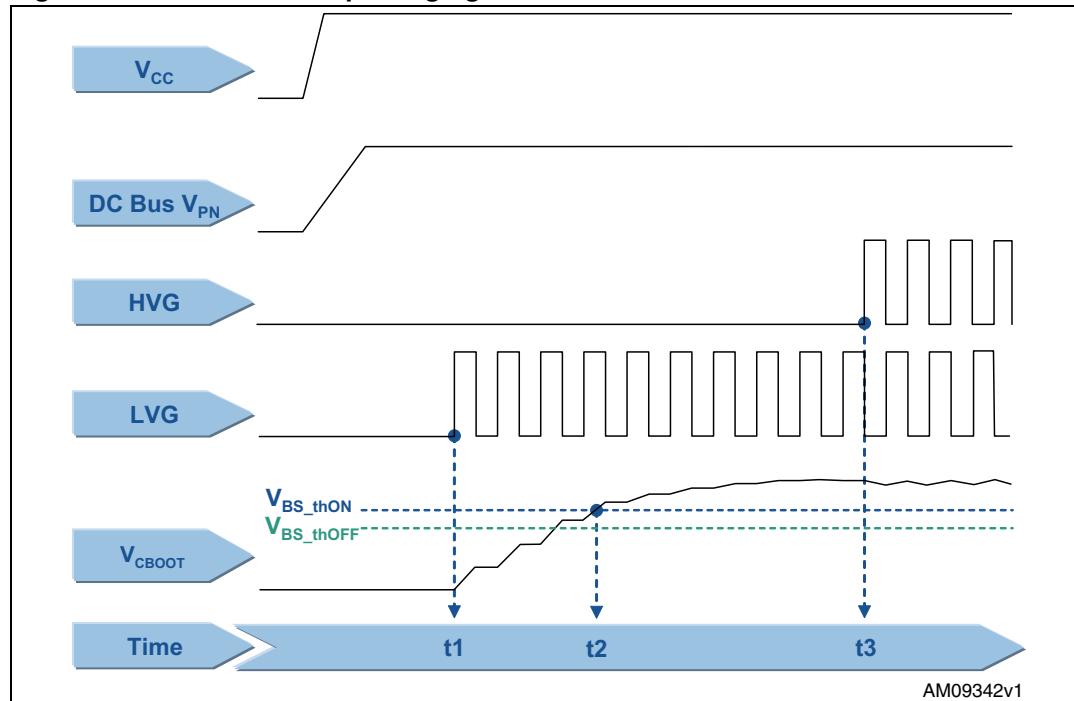
Considering the limit cases during the PWM control and further leakages and dispersions in the board layout, the capacitance value to use in the bootstrap circuit must be selected two or three times higher than the C_{BOOT} calculated in the graph of *Figure 21*. The bootstrap capacitor should be with a low ESR value for a good local decoupling, therefore, in case an electrolytic capacitor is used, one parallel ceramic capacitor placed directly on the SLLIMM-nano pins is strictly recommended.

2.3.13 Initial bootstrap capacitor charging

During the startup phase, the bootstrap capacitor must be charged for a suitable time to complete the initial charging time (t_{CHARGE}), which is, at least, the time V_{CBOOT} needs to exceed the turn-on undervoltage threshold V_{BS_thON}, as already stated in *Equation 9Equation 9*. For a normal operation, the voltage across the bootstrap capacitor must never drop down to the turn-off undervoltage threshold V_{BS_thOFF} throughout the working conditions. For the period of startup, only the low-side IGBT is switched on and, just after this phase, the PWM is run, as shown in the following steps of *Figure 22*:

- t1: the bootstrap capacitor starts to charge through the low-side IGBT (LVG)
- t2: the voltage across the bootstrap capacitor (V_{CBOOT}) reaches its turn-on undervoltage threshold V_{BS_thON}
- t3: the bootstrap capacitor is fully charged; this enables the high-side IGBT and the C_{BOOT} capacitor starts to discharge in order to provide the right IGBT gate charge. The bootstrap capacitor recharges during the on-state of the low-side IGBT (LVG).

Figure 22. Initial bootstrap charging time

The initial charging time is given by*Equation 12 Equation 12* and must be, for safety reasons, at least three times longer than the calculated value.

Equation 12

$$t_{CHARGE} \geq \frac{C_{BOOT} \cdot R_{DS(on)}}{\delta} * \ln\left(\frac{V_{CC}}{\Delta V_{CBOOT}}\right)$$

where δ is the duty cycle of the PWM signal and $R_{DS(on)}$ is 120 Ω typical value, as shown in the datasheet.

A practical example can be done by considering a motor drive application where the PWM switching frequency is 16 kHz, with a duty cycle of 50%, and ΔV_{CBOOT} = 0.1 V (that means, a gate driver supply voltage V_{CC} = 17.5 V). From the graph in *Figure 21* the bootstrap capacitance is 1.0 µF, therefore the C_{BOOT} can be selected by using a value between 2.0 and 3.0 µF. According to the commercial value the bootstrap capacitor can be 2.2 µF. From *Equation 12Equation 12*, the initial charging time is:

Equation 13

$$t_{CHARGE} \geq \frac{2.2 \cdot 10^{-6} \cdot 120}{0.5} \cdot \ln\left(\frac{17.5}{0.1}\right) = 2.7 ms$$

For safety reasons, the initial charging time must be at least 8.1 ms.

3 Package

The NDIP is a dual-in-line transfer mold package available in 26-lead version (NDIP-26L) able to meet demanding cost and size requirements of consumer appliance inverters. It consists of a copper lead frame with power stage and control stage soldered on it and housed using the transfer molding process. The excellent thermal properties of the copper allows good heat spread and heat transfer, furthermore, the thickness and the layout of the lead frames has been optimized in order to further reduce the thermal resistance.
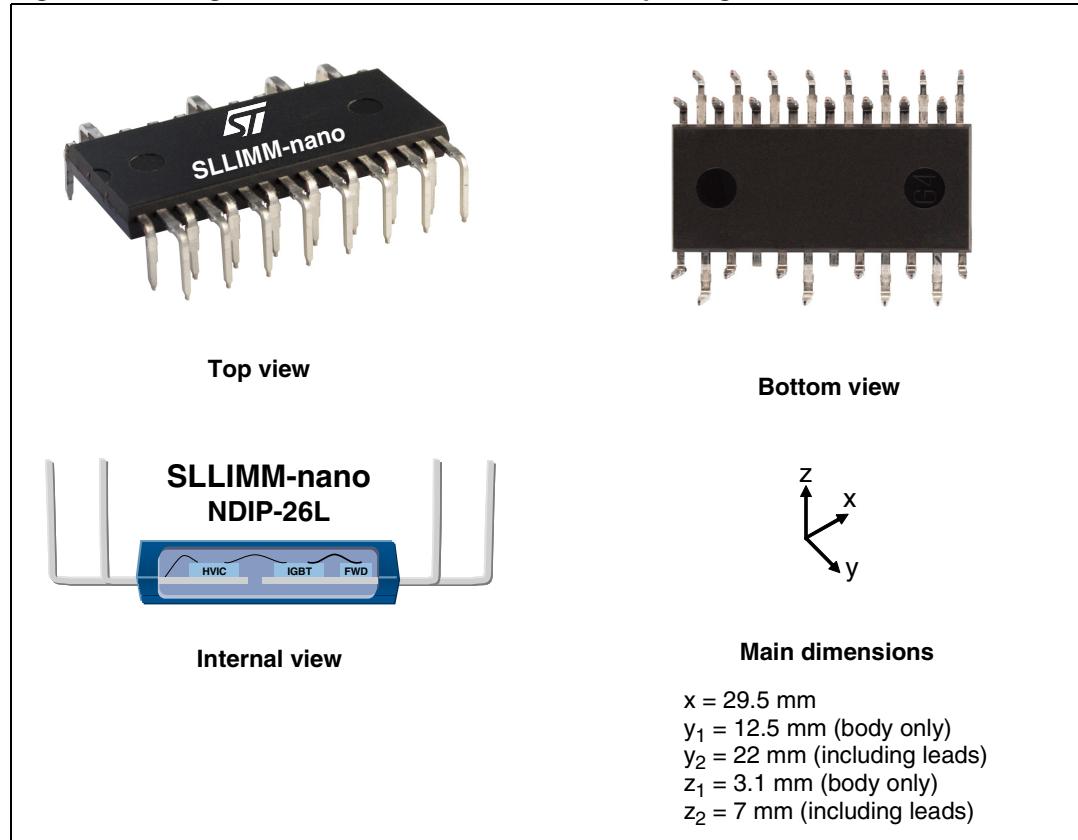
The package pinout has been designed in order to maximize the distance between the high voltage and low voltage pins, by placing the relevant pins on the opposite side of the package. This is mainly useful to keep a safe distance between high voltage and low voltage pins and for an easy PCB layout.

Finally, thanks to the transfer molding technology and design optimization, the SLLIMM-nano offers a high power density level in a very compact package while providing good thermal propriety, electrical isolation and overall reliable performance.

3.1 Package structure

Figure 23 contains the images and an internal structure illustration of the NDIP-26L package.

Figure 23. Images and internal view of NDIP-26L package

Top view

Bottom view

SLLIMM-nano
NDIP-26L

Internal view

Main dimensions

$x = 29.5$ mm
$y_1 = 12.5$ mm (body only)
$y_2 = 22$ mm (including leads)
$z_1 = 3.1$ mm (body only)
$z_2 = 7$ mm (including leads)

3.2 Package outline and dimensions

Figure 24.   Outline drawing of NDIP-26L package
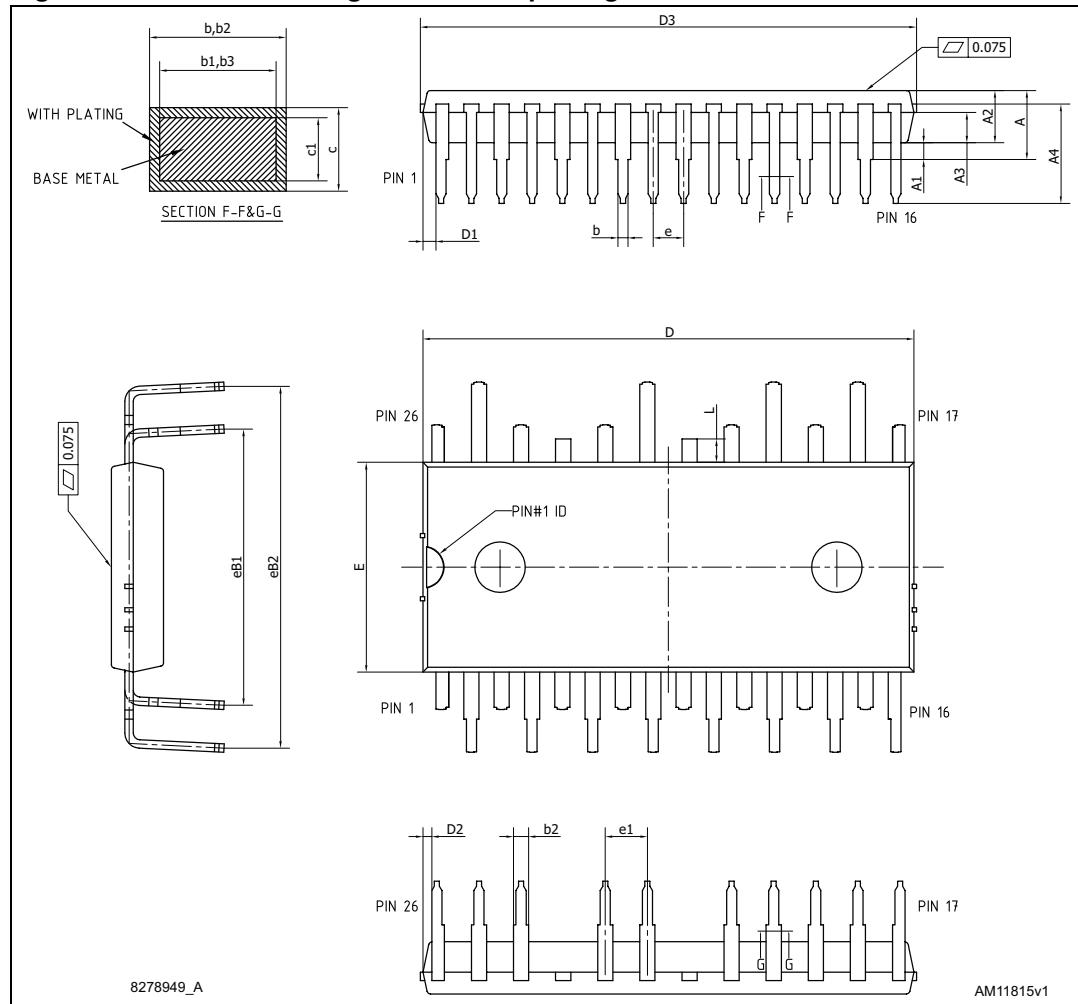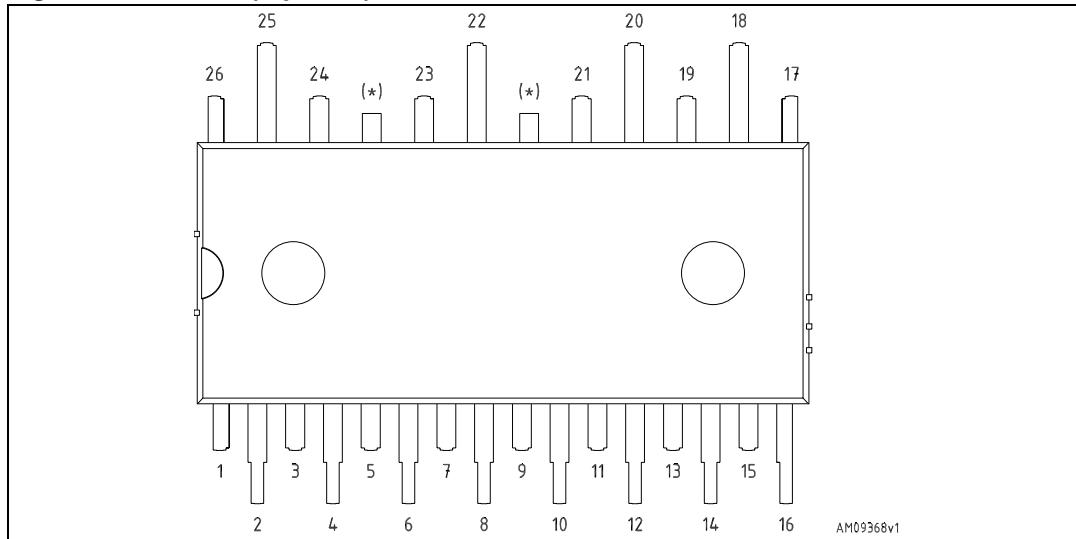
Table 9.   Outline drawing of NDIP-26L package

Dimension	(mm)		
	Min.	**Typ.**	**Max.**
A			4.4
A1	0.8	1	1.2
A2	3	3.1	3.2
A3	1.7	1.8	1.9
A4	5.7	5.9	6.1
b	0.53		0.72
b1	0.52	0.6	0.68
b2	0.83		1.02
b3	0.82	0.9	0.98
c	0.46		0.59
c1	0.45	0.5	0.55
D	29.05	29.15	29.25
D1	0.5		
D2	0.35		
D3			29.55
E	12.35	12.45	12.55
e	1.7	1.8	1.9
e1	2.4	2.5	2.6
eB1	16.1	16.4	16.7
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

3.3   Input and output pins description

This paragraph defines the input and output pins of the SLLIMM-nano. For a more accurate description and layout suggestions, please consult the relevant sections.


Figure 25. Pinout (top view)

Table 10. Input and output pins

Pin #	Name		Description	
	STGIPN3H60A	STGIPN3H60	STGIPN3H60A	STGIPN3H60
1	GND		Ground	
2	NC	$\overline{SD}$ / OD	Not connected	Shutdown logic input (active low) / open drain (comparator output)
3	$V_{CC\ W}$		Low voltage power supply W phase	
4	HIN_W		High-side logic input for W phase	
5	LIN_W	$\overline{LIN_{\overline{W}}}$	Low-side logic input for W phase (active high)	Low-side logic input for W phase (active low)
6	NC	OP_+	Not connected	Op amp non inverting input
7	NC	OP_{OUT}	Not connected	Op amp output
8	NC	OP_-	Not connected	Op amp inverting input
9	$V_{CC\ V}$		Low voltage power supply V phase	
10	HIN_V		High-side logic input for V phase	
11	LIN_V	$\overline{LIN_{\overline{V}}}$	Low-side logic input for V phase (active high)	Low-side logic input for V phase (active low)
12	NC	CIN	Not connected	Comparator input
13	$V_{CC\ U}$		Low voltage power supply U phase	
14	HIN_U		High-side logic input for U phase	
15	NC	$\overline{SD}$ / OD	Not connected	Shutdown logic input (active low) / open drain (comparator output)
16	LIN_U	$\overline{LIN_{\overline{U}}}$	Low-side logic input for U phase (active high)	Low-side logic input for U phase (active low)
17	V_{bootU}		Bootstrap voltage for U phase	

Table 10.   Input and output pins (continued)

Pin #	Name		Description	
	STGIPN3H60A	**STGIPN3H60**	**STGIPN3H60A**	**STGIPN3H60**
18	P		Positive DC input	
19	U		U phase output	
20	N_U		Negative DC input for U phase	
21	V_{bootV}		Bootstrap voltage for V phase	
22	V		V phase output	
23	N_V		Negative DC input for V phase	
24	V_{bootW}		Bootstrap voltage for W phase	
25	W		W phase output	
26	N_W		Negative DC input for W phase	

High-side bias voltage pins /high-side bias voltage reference

Pins: V_{bootU}-U, V_{bootV}-V, V_{bootW}-W

● The bootstrap section is designed to realize a simple and efficient floating power supply, in order to provide the gate voltage signal to the high-side IGBTs

● The SLLIMM-nano family integrates the bootstrap diodes. This helps users to save costs, board space, and number of components

● The advantage of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs

● Each bootstrap capacitor is charged from the VCC supply during the on-state of the corresponding low-side IGBT

● To prevent malfunction caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins

● The value of bootstrap capacitors is strictly related to the application conditions. Please consult *Section 2.3.11: Bootstrap circuit* for more information.

Gate driver bias voltage

Pins: $V_{CC\ U}$, $V_{CC\ V}$, $V_{CC\ W}$

● Control supply pins for the built-in ICs

● To prevent malfunction caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.

Gate drive supply ground

Pin: GND

● Ground reference pin for the built-in ICs

● To avoid noise influence, the main power circuit current should not be allowed to flow through this pin (see *Section 5.1: Layout suggestions*).

Signal input

Pins: HIN_U, HIN_V, HIN_W; LIN_U, LIN_V, LIN_W; $\overline{LIN_U}$, $\overline{LIN_V}$, $\overline{LIN_W}$

● These pins control the operation of the built-in IGBTs.

● The signal logic of HIN_U, HIN_V, HIN_W, LIN_U, LIN_V, and LIN_W pins is active high. The IGBT associated with each of these pins is turned on when a sufficient logic (higher than a specific threshold) voltage is applied to these pins.

● The signal logic of LIN_U, LIN_V, LIN_W pins is active low. The IGBT associated with each of these pins is turned on when a logic voltage (lower than a specific threshold voltage) is applied to these pins.

● The wiring of each input should be as short as possible to protect the SLLIMM-nano against noise influence. RC coupling circuits should be adopted for the prevention of input signal oscillation. Suggested values are R=100Ω and C=1nF.

Internal comparator non-inverting (only for the STGIPN3H60)

Pin: CIN

● The current sensing shunt resistor, connected on each phase leg, may be used by the internal comparator (pin CIN) to detect short-circuit current

● The shunt resistor should be selected to meet the detection levels matched for the specific application

● An RC filter (typically ~1 μs) should be connected to the CIN pin to eliminate noise

● The connection length between the shunt resistor and CIN pin should be minimized

● If a voltage signal, higher than the specified V_{REF} (see datasheet), is applied to this pin, the SLLIMM-nano automatically shuts down and the $\overline{SD}$ / OD pin is pulled down (to inform the microcontroller).

Shutdown / open drain (only for the STGIPN3H60)

Pins: $\overline{SD}$ / OD

● There are two available pins of $\overline{SD}$ / OD which are exactly the same. They are placed on the opposite ends of the package in order to offer higher flexibility to the PCB layout. It is sufficient to use only one of the two pins for the proper functioning of the device.

● The $\overline{SD}$ / OD pins work as enable/disable pins.

● The signal logic of $\overline{SD}$ / OD pins are active low. The SLLIMM-nano shuts down if a voltage lower than a specific threshold is applied to these pins, leading each half bridge in tri-state.

● The $\overline{SD}$ / OD status is connected also to the internal comparator status (*Section 2.3.6: Short-circuit protection and smart shutdown function*). When the comparator triggers, the $\overline{SD}$ / OD pin is pulled down acting as a FAULT pin.

● The $\overline{SD}$ / OD, when pulled down by the comparator, are open drain configured. The $\overline{SD}$ / OD voltage should be pulled up to the 3.3 V or 5 V logic power supply through a pull-up resistor.

Integrated operational amplifier (only for the STGIPN3H60)

Pins: OP+, OP-, OP_{OUT}

● The op amp is completely uncommitted

● The op amp performance is optimized for advanced control technique (FOC)

● Thanks to the integrated op amp, it is possible to realize a compact and efficient board layout, minimizing the required BOM list.

Positive DC-link

Pin: P

● This is a DC-link positive power supply pin of the inverter and it is internally connected to the collectors of the high-side IGBTs

● To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to the P pin. Generally a 0.1 or 0.22 µF high frequency, high voltage non-inductive capacitor is recommended.

Negative DC-link

Pins: N_U, N_V, N_W

● These are the DC-link negative power supply pins (power ground) of the inverter

● These pins are connected to the low-side IGBT emitters of each phase

● The power ground of the application should be separated from the logic ground of the system and they should be reconnected at one specific point (star connection).

Inverter power output

Pins: U, V, W

● Inverter output pins for connecting to the inverter load (e.g. motor).

4 Power losses and dissipation

The total power losses in an inverter are comprised of conduction losses, switching losses, and off-state losses and they are essentially generated by the power devices of the inverter stage, such as the IGBTs and the freewheeling diodes. The conduction losses (P_{COND}) are the on-state losses during the conduction phase. The switching losses (P_{SW}) are the dynamic losses encountered during turn-on and turn-off. The off-state losses, due to the blocking voltage and leakage current, can be neglected.
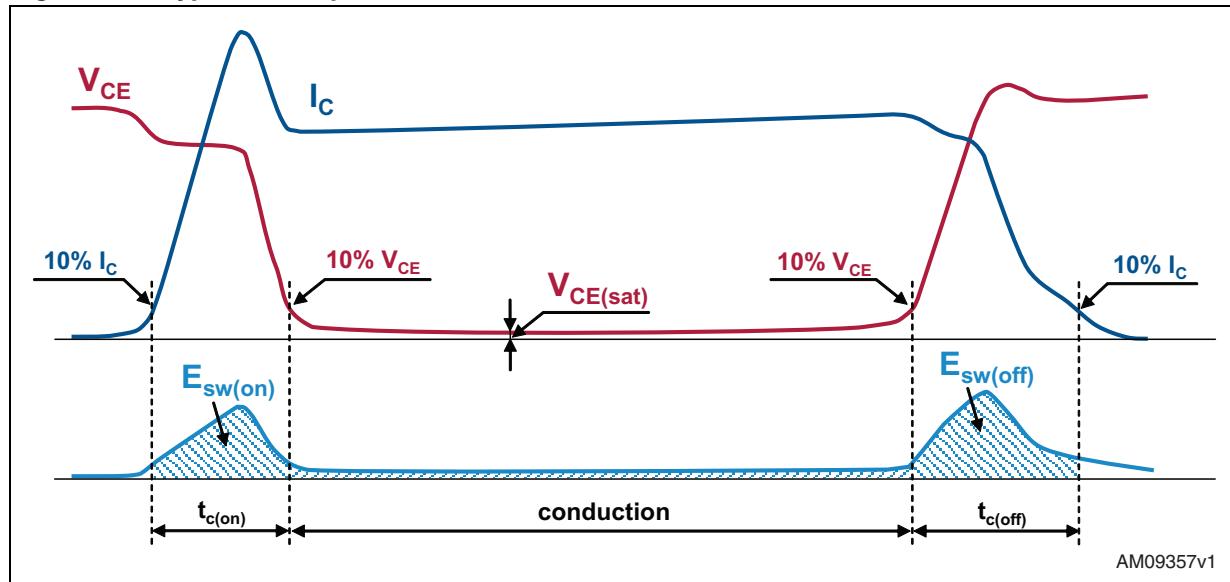
Finally, the total power losses are given by:

Equation 14

$$P_{tot} \approx P_{cond} + P_{sw}$$
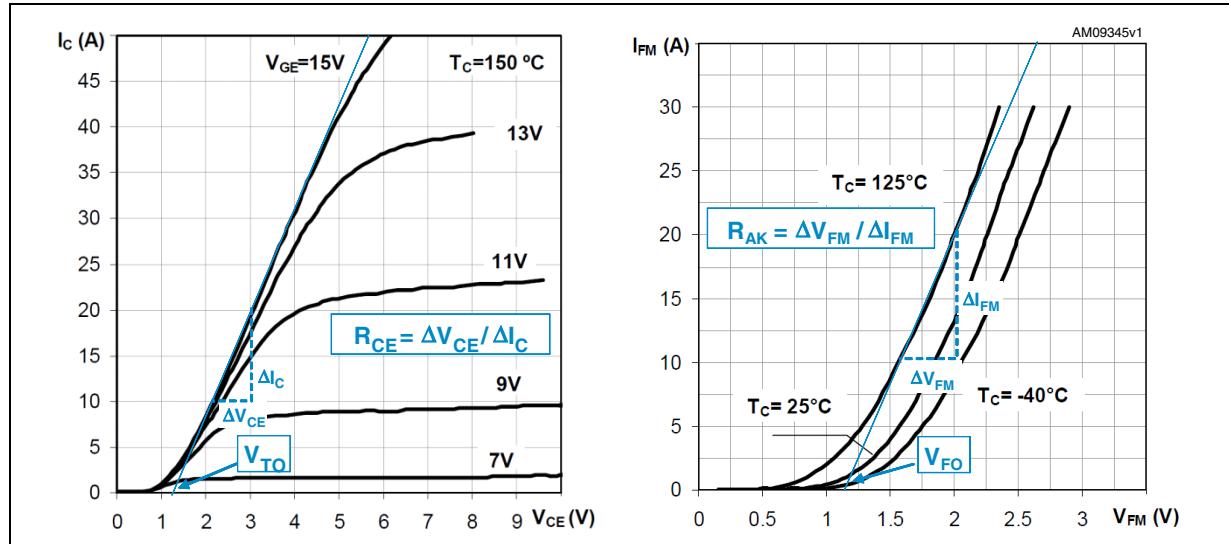
Figure 26 shows a typical waveform of an inductive hard switching application such as a motor drive, where the major sources of power losses are specified.

Figure 26. Typical IGBT power losses

4.1 Conduction power losses

The conduction losses are caused by IGBT and freewheeling diode forward voltage drop at rated current. They can be calculated using a linear approximation of the forward characteristics for both the IGBT and diode, having a series connection of DC voltage source representing the threshold voltage, V_{TO} for IGBT, (and V_{FO} for diode) and a collector emitter on-state resistance, R_{CE}, (and anode cathode on-state resistance, R_{AK}), as shown in *Figure 27*.

Figure 27.   IGBT and diode approximation of the output characteristics

Both forward characteristics are temperature dependent, and so must be considered under a specified temperature.

The linear approximations can be translated for IGBT in the following equation:

Equation 15

$$v_{ce}(i_c) = V_{TO} + R_{CE} \cdot i_c$$

and, for freewheeling diode:

Equation 16

$$v_{fm}(i_{fm}) = V_{FO} + R_{AK} \cdot i_{fm}$$

The conduction losses of IGBT and diode can be derived as the time integral of the product of conduction current and voltage across the devices, as follows:

Equation 17

$$P_{cond\_IGBT} = \frac{1}{T}\int_0^T v_{ce} \cdot i_c(t)dt = \frac{1}{T}\int_0^T \left(V_{TO} \cdot i_c(t) + R_{ce} \cdot i_c^2(t) \right)dt$$

Equation 18

$$P_{cond\_Diode} = \frac{1}{T}\int_0^T v_f \cdot i_f(t)dt = \frac{1}{T}\int_0^T \left(V_{FO} \cdot i_f(t) + R_{AK} \cdot i_f^2(t) \right)dt$$

where T is the fundamental period.

The different utilization mode of the SLLIMM-nano, modulation technique, and working conditions make the power losses very difficult to estimate, it is therefore necessary to fix some starting points.

Assuming that:

1. The application is a variable voltage variable frequency (VVVF) inverter based on sinusoidal PWM technique.
2. The switching frequency is high and therefore the output currents are sinusoidal.
3. The load is ideal inductive.

Under these conditions, the output inverter current is given by:

Equation 19

$$i = \hat{I}\cos(\theta - \phi)$$

where $\hat{I}$ is the current peak, θ stands for ωt and ϕ is the phase angle between output voltage and current.

The conduction power losses can be obtained as:

Equation 20

$$P_{cond\_IGBT} = \frac{V_{TO} \cdot \hat{I}}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi \cos(\theta - \phi)d\theta + \frac{R_{CE} \cdot \hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi \cos^2(\theta - \phi)d\theta$$

Equation 21

$$P_{cond\_Diode} = \frac{V_{FO}\hat{I}}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\xi)\cos(\theta - \phi)d\theta + \frac{R_{AK}\hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\xi)\cos^2(\theta - \phi)d\theta$$

where ξ is the duty cycle for this PWM technique and is given by:

Equation 22

$$\xi = \frac{1 + m_a \cdot \cos\theta}{2}$$

and m_a is the PWM amplitude modulation index.

Finally, solving *Equation 20Equation 20* and *Equation 21Equation 21*, we have:

Equation 23

$$P_{cond\_IGBT} = V_{TO} \cdot \hat{I}\left(\frac{1}{2\pi} + \frac{m_a \cdot \cos\phi}{8}\right) + \frac{R_{CE} \cdot \hat{I}^2}{2\pi}\left(\frac{1}{8} + \frac{m_a \cdot \cos\phi}{3\pi}\right)$$

Equation 24

$$P_{cond\_Diode} = V_{FO} \cdot \hat{I}\left(\frac{1}{2\pi} - \frac{m_a \cdot \cos\phi}{8}\right) + \frac{R_{AK} \cdot \hat{I}^2}{2\pi}\left(\frac{1}{8} - \frac{m_a \cdot \cos\phi}{3\pi}\right)$$

and therefore, the conduction power losses of one device (IGBT and diode) are:

Equation 25

$$P_{cond} = P_{cond\_IGBT} + P_{cond\_Diode}$$

Of course, the total conduction losses per inverter are six times this value.

4.2 Switching power losses

The switching loss is the power consumption during the turn-on and turn-off transients. As already shown in *Figure 26*, it is given by the pulse of power dissipated during the turn-on (t_{on}) and turn-off (t_{off}). Experimentally, it can be calculated by the time integral of product of the collector current and collector-emitter voltage for the switching period. However, the dynamic performance is strictly related to many parameters such as voltage, current and temperature, so it is necessary to use the same assumptions of conduction power losses (*Section 4.1: Conduction power losses*) to simplify the calculations.

Under these conditions, the switching energy losses are given by:

Equation 26

$$E_{on}(\theta) = \hat{E}_{on}\, \cos(\theta - \phi)$$

Equation 27

$$E_{off}(\theta) = \hat{E}_{off}\, \cos(\theta - \phi)$$

where $\hat{E}_{on}$ and $\hat{E}_{off}$ are the maximum values taken at T_{jmax} and $\hat{I}_c$, θ stands for ωt and ϕ is the phase angle between output voltage and current.

Finally, the switching power losses per device depend on the switching frequency (f_{sw}) and they are calculated as follows:

Equation 28
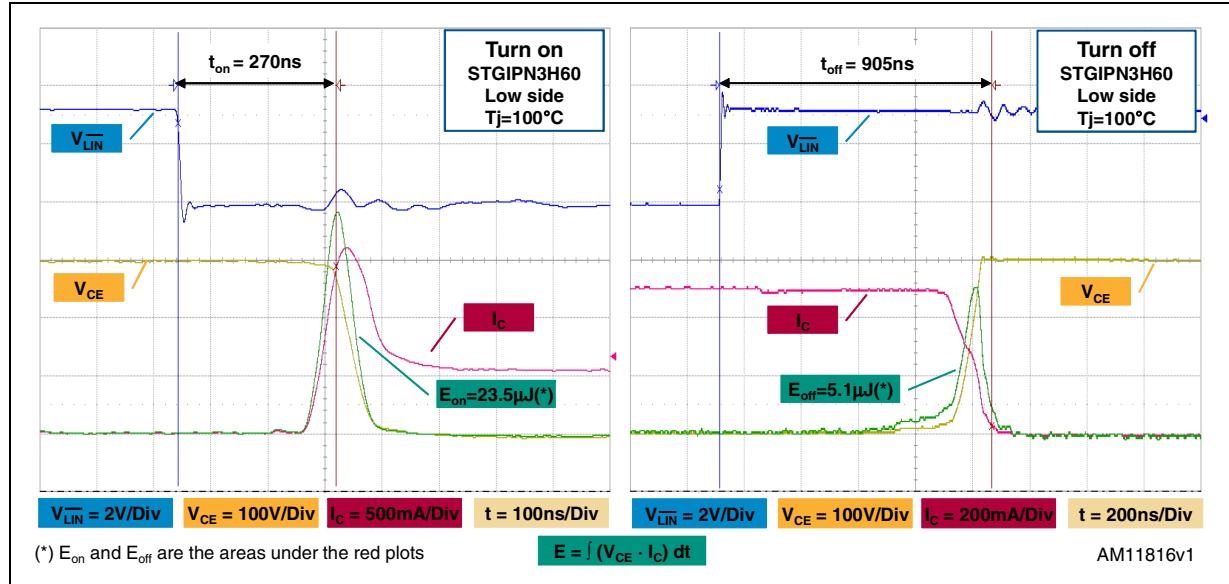
$$P_{sw} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (E_{IGBT} + E_{Diode}) \cdot f_{sw} d\theta = \frac{(E_{IGBT} + E_{Diode}) \cdot f_{sw}}{\pi}$$

where E_{IGBT} and E_{Diode} are the total switching energy for the IGBT and the freewheeling diode, respectively. Also in this case, the total switching losses per inverter are six times this value.

Figure 28 shows the real turn-on and turn-off waveforms of the STGIPN3H60 under the following conditions:

● V_{PN} = 300 V, I_C = 0.5 A, T_j = 100 °C with inductive load on full bridge topology, taken on the low-side IGBT.

The green plots represent instantaneous power as a result of IC (in red) and V_{CE} (in yellow) waveforms multiplication, during the switching transitions. The areas under these plots are the switching energies computed by graphic integration thanks to the digital oscilloscope.

Figure 28. Typical switching waveforms of the STGIPN3H60

| $V_{\overline{LIN}}$ = 2V/Div | V_{CE} = 100V/Div | I_C = 500mA/Div | t = 100ns/Div | $V_{\overline{LIN}}$ = 2V/Div | V_{CE} = 100V/Div | I_C = 200mA/Div | t = 200ns/Div |

(*) E_{on} and E_{off} are the areas under the red plots $\quad$ **E = ∫ (V_{CE} · I_C) dt** $\quad\quad$ AM11816v1

4.3 Thermal impedance overview

During operation, power losses generate heat which elevates the temperature in the semiconductor junctions contained in the SLLIMM-nano, limiting its performance and lifetime. To ensure safe and reliable operation, the junction temperature of power devices must be kept below the limits defined in the datasheet, therefore, the generated heat must be conducted away from the power chips and into the environment using an adequate cooling system.

The SLLIMM-nano was designed to drive electric motors up to 100 W without any heatsink. Therefore, the thermal aspect of the system is one of the key factors in designing high efficiency and high reliability equipment. In this environment the package and its thermal resistance play a fundamental role.

Thermal resistance quantifies the capability of a given thermal path to transfer heat in steady-state and it is generically given as the ratio between the temperature increase above the reference and the relevant power flow:

Equation 29

$$R_{th} = \frac{\Delta T}{\Delta P}$$
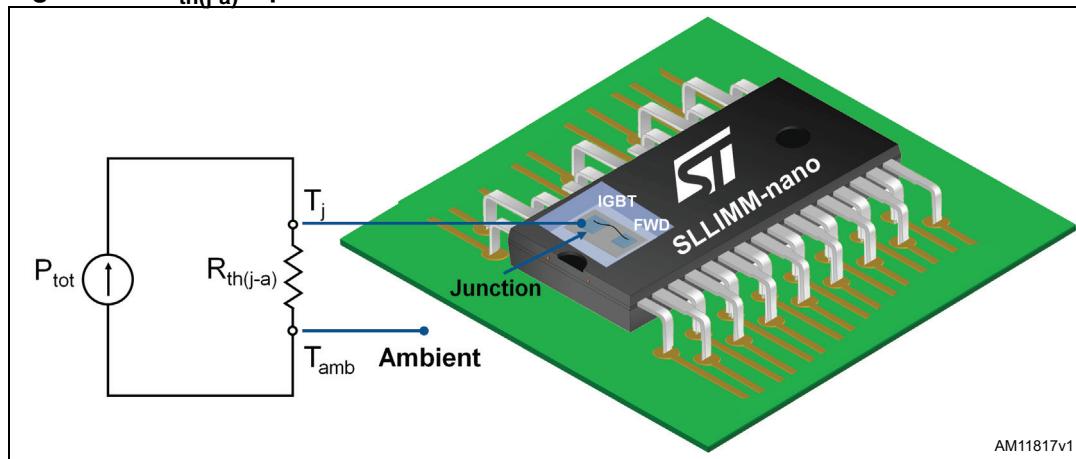
The thermal resistance specified in the datasheet is the junction-ambient $R_{th(j-a)}$ which is commonly used with natural and forced convection air cooled systems and it is defined as the difference in temperature between junction and ambient reference divided by the power dissipation per device:

Equation 30

$$R_{th(j-a)} = \frac{T_j - T_{amb}}{P_D}$$

Figure 29 shows an equivalent circuit of the thermal resistance between junction and ambient $R_{th(j-a)}$.

Figure 29. $R_{th(j-a)}$ equivalent thermal circuit

As the power loss P_{tot} is cyclic, also the transient thermal impedance must be considered. It is defined as the ratio between the time dependent temperature increase above the reference, $\Delta T(t)$, and the relevant heat flow:
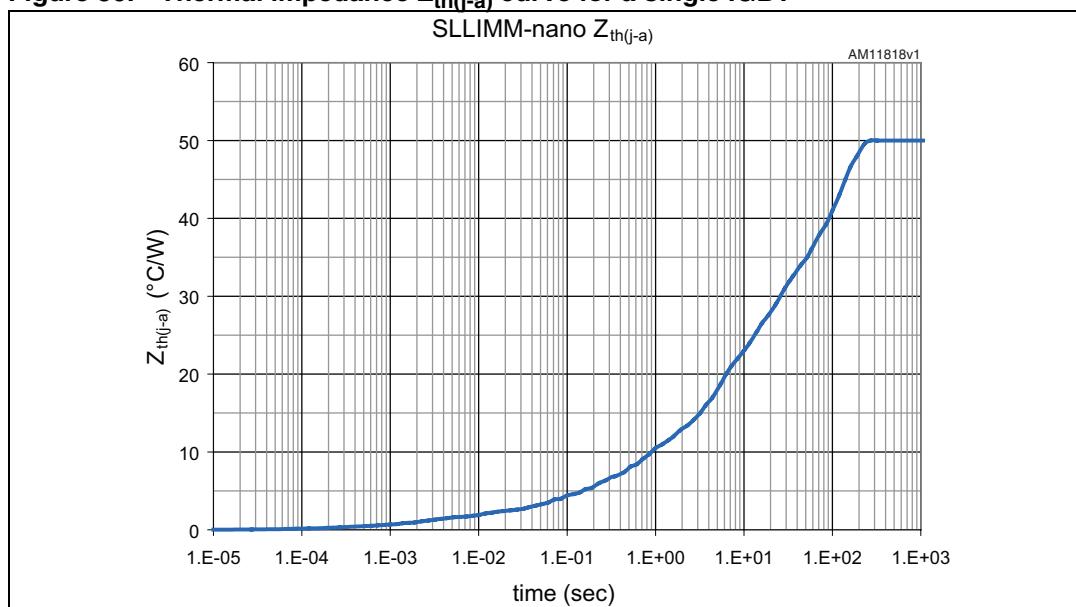
Equation 31

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P}$$

Contrary to that already seen regarding the thermal resistance, the thermal impedance is typically represented by an RC equivalent circuit. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature and therefore the advantage of this behavior is the short-term overload capability of the SLLIMM-nano.
For example, *Figure 30* shows thermal impedance from a junction to ambient curve for a single IGBT of the SLLIMM-nano.

Figure 30.   Thermal impedance $Z_{th(j-a)}$ curve for a single IGBT

More generally, in the case of the device, power is time dependent too. The device temperature can be calculated by using the convolution integral method applied to *Equation 31Equation 31*, as follows:
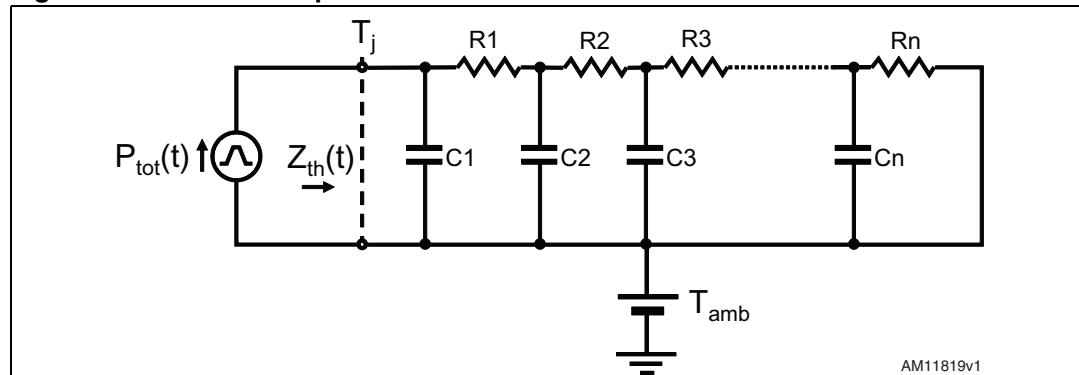
Equation 32

$$\Delta T(t) = \int_0^t Z_{th}(t - \tau) \cdot P(\tau) d\tau$$
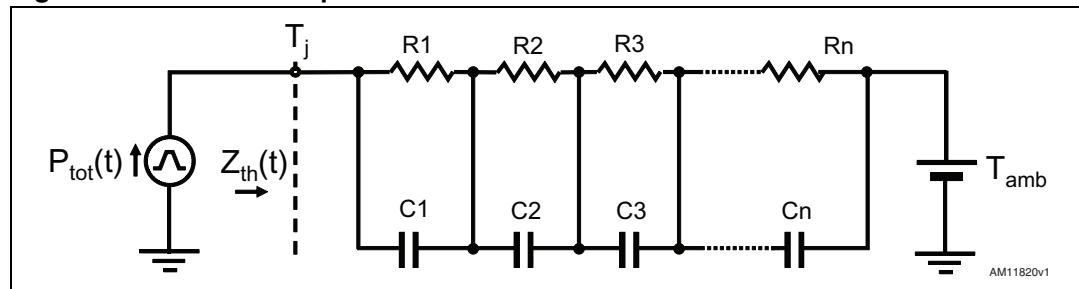
An alternative method, very useful for the simulator tools, is the transient thermal impedance model, which provides a simple method to estimate the junction temperature rise under a transient condition.

By using the thermo-electrical analogy, the transient thermal impedance $Z_{th(t)}$ can be transformed into an electrical equivalent RC network. The number of RC sections increases the model details, therefore a twelfth order model, for $Z_{th(j-a)}$, based on the Cauer and Foster networks, has been used in order to improve the accuracy of both models.

Figure 31 and *Figure 32* show the general Cauer and Foster RC equivalent circuit used for the thermal impedance model.

Figure 31.   Cauer RC equivalent circuit

Figure 32.   Foster RC equivalent circuit

Temperatures inside the electrical RC network represent voltages, power flows represent currents, electrical resistances and capacitances represent thermal resistances and capacitances respectively. The case temperature is represented with a DC voltage source and it can be interpreted as the initial junction temperature.

Transient thermal impedance models are derived by curve fitting an equation to the measured data. Values for the individual resistors and capacitors are the variables from that equation and are defined in *Table 11*, for both $Z_{th(j-a)}$ Cauer and Foster thermal impedance models.

Table 11.   Cauer and Foster RC thermal network elements
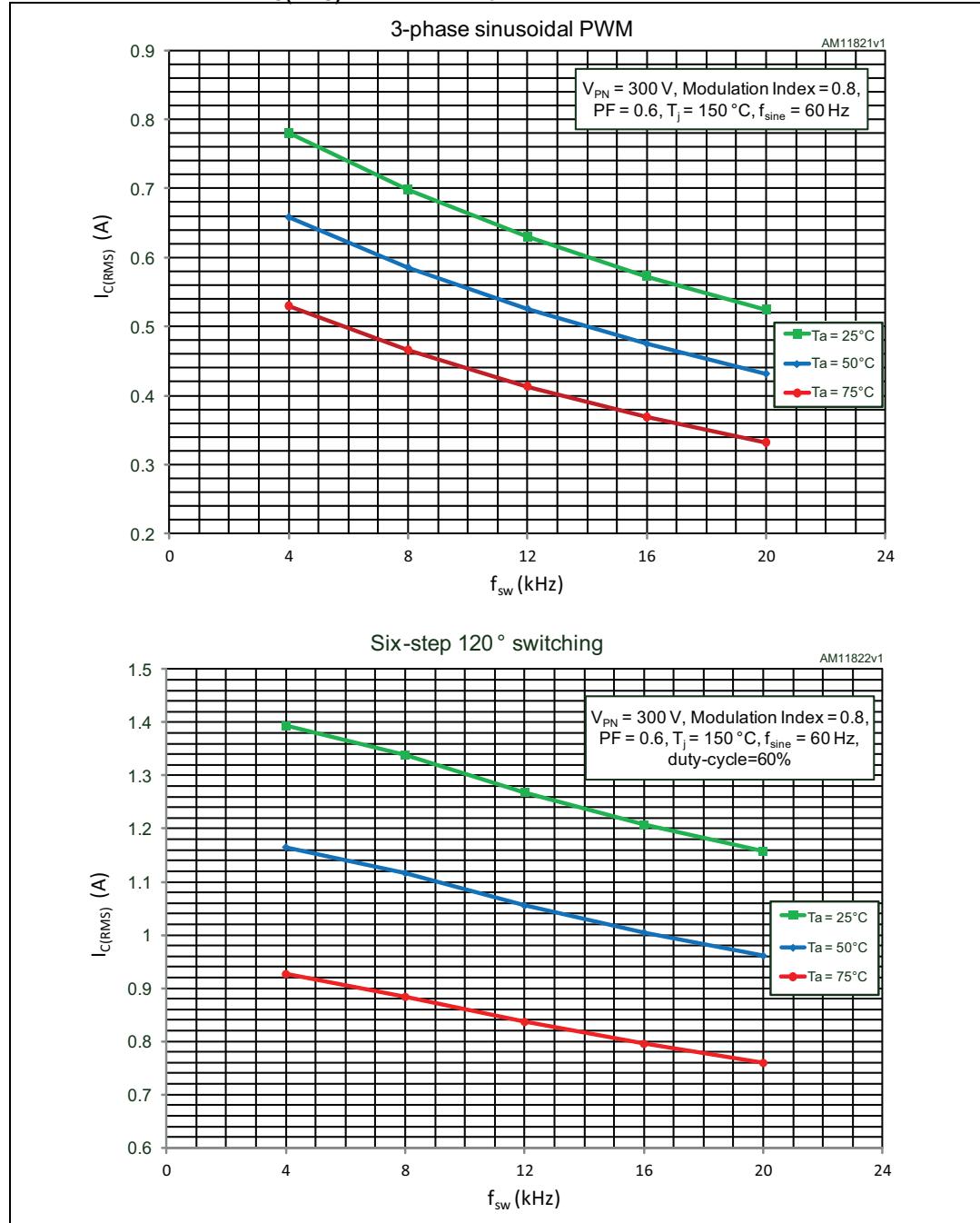
Element	$Z_{th(j-a)}$ Cauer Network	$Z_{th(j-a)}$ Foster Network
R1 (°C/W)	8.96E-01	1.81E-01
R2 (°C/W)	9.37E-01	1.71E-01
R3 (°C/W)	5.92E-01	8.12E-02
R4 (°C/W)	1.37E-02	5.11E-02
R5 (°C/W)	2.11E-02	1.86E-01
R6 (°C/W)	2.84E+00	6.58E-01
R7 (°C/W)	1.26E-01	5.00E-04
R8 (°C/W)	4.48E-02	6.95E-02
R9 (°C/W)	4.06E-01	5.14E-01
R10 (°C/W)	4.93E+00	4.43E+00
R11 (°C/W)	9.38E+00	7.90E+00
R12 (°C/W)	2.99E+01	3.58E+01
C1 (W·sec/°C)	6.25E-04	1.55E-01
C2 (W·sec/°C)	3.81E-03	1.67E-01
C3 (W·sec/°C)	4.69E-03	1.19E+00
C4 (W·sec/°C)	2.41E-03	9.09E-01
C5 (W·sec/°C)	4.39E-03	1.84E-02
C6 (W·sec/°C)	3.27E-03	1.07E-03
C7 (W·sec/°C)	1.82E-02	1.77E-03
C8 (W·sec/°C)	1.32E-02	8.80E-02
C9 (W·sec/°C)	3.63E-03	1.19E-02
C10 (W·sec/°C)	6.72E-02	4.74E-02
C11 (W·sec/°C)	2.75E-02	2.35E-01
C12 (W·sec/°C)	2.22E+00	1.75E+00

4.4   Power loss calculation example

As a result of power loss calculation and thermal aspects, fully treated in the previous sections, it is possible to simulate the maximum $I_{C(RMS)}$ current versus switching frequency curves for a VVVF inverter using a 3-phase sinusoidal PWM and a six-step 120° switching modulation to synthesize sinusoidal output currents.

The curves graphed in *Figure 33* represent the maximum current managed by the SLLIMM-nano in safety conditions, when the junction temperature rises to the maximum junction temperature of 150 °C for three ambient temperatures (25, 50 and 75 °C), which is a typical operating condition to guarantee the reliability of the system. These curves, functions of the motor drive typology and control scheme, are simulated under the following conditions:

● V_{PN} = 300 V, m_a = 0.8, cos = 0.6, T_j = 150 °C, T_c = 100 °C, f_{SINE} = 60 Hz, max. value of $R_{th(j-c)}$, typical $V_{CE(sat)}$ and E_{tot} values.

Figure 33. Maximum I$_{C(RMS)}$ current vs. f$_{sw}$ simulated curves

5 Design and mounting guidelines

This section introduces the main layout suggestions for an optimized design and major mounting recommendations, to appropriately handle and assemble the SLLIMM-nano family.

5.1 Layout suggestions

Optimization of PCB layout for high voltage and high switching frequency applications is a critical point. PCB layout is a complex matter as it includes several aspects, such as length and width of track and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application to properly function and achieve the expected performance. On the other hand, a PCB without a careful layout can generate EMI issues (both induced and perceived by the application), can provide overvoltage spikes due to parasitic inductances along the PCB traces, and can produce higher power loss and even malfunction in the control and sensing stages.
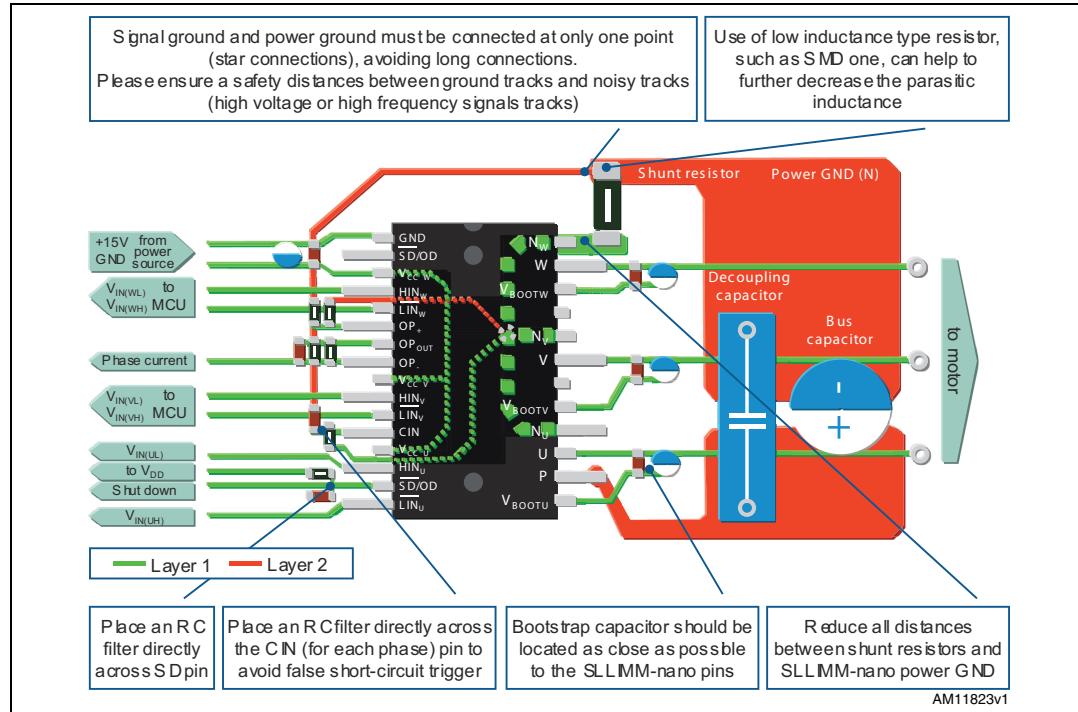
The compactness of the SLLIMM-nano solution, which offers an optimized gate driving network and reduced parasitic elements, allows users to focus only on certain issues, such as the ground issue or noise filter. Therefore, in order to avoid all the aforementioned conditions, the following general guidelines and suggestions must be followed in PCB layout for 3-phase applications.

5.1.1 General suggestions

- PCB traces should be designed to be as short as possible and the area of the circuit (power or signal) should be minimized to avoid the sensitivity of such structures to surrounding noise.

- Ensure a good distance between switching lines with high voltage transitions and the signal line sensitive to electrical noise. Specifically, the tracks of each OUT phase, bringing significant currents and high voltages, should be separated from the logic lines and analog sensing circuit of the op amp and comparator.

- Place the R_{SENSE} resistors as close as possible to the low-side pins of the SLLIMM-nano (N_U, N_V and N_W). Parasitic inductance can be minimized by connecting the ground line (also called driver ground) of the SLLIMM-nano directly to the cold terminal of sense resistors. Use of a low inductance type resistor, such as an SMD resistor instead of long-lead type resistors, can help to further decrease the parasitic inductance.

- Avoid any ground loop. Only a single path must connect two different ground nodes.

- Place each RC filter as close as possible to the SLLIMM-nano pins in order to increase their efficiency.

- In order to prevent surge destruction, the wiring between the smoothing capacitor and the P and N pins should be as short as possible. The use of a high frequency, high voltage non-inductive capacitor about 0.1 or 0.22 µF between the P and N pins is recommended.

- Fixed voltage tracks, such as GND or HV lines, can be used to shield the logic and analog lines from the electrical noise produced by the switching lines (e.g. U, V and W).

- Generally it is recommended to connect each half bridge ground in a star configuration and the three R_{SENSE} very close to each other and to the power ground.

In *Figure 34*, general suggestions for all SLLIMM-nano products are summarized.

Figure 34. General suggestions

Special attention must be paid to wrong layouts. In *Figure 35* and *Figure 36* some common PCB mistakes are shown.

Figure 35. Example 1 on a possible wrong layout
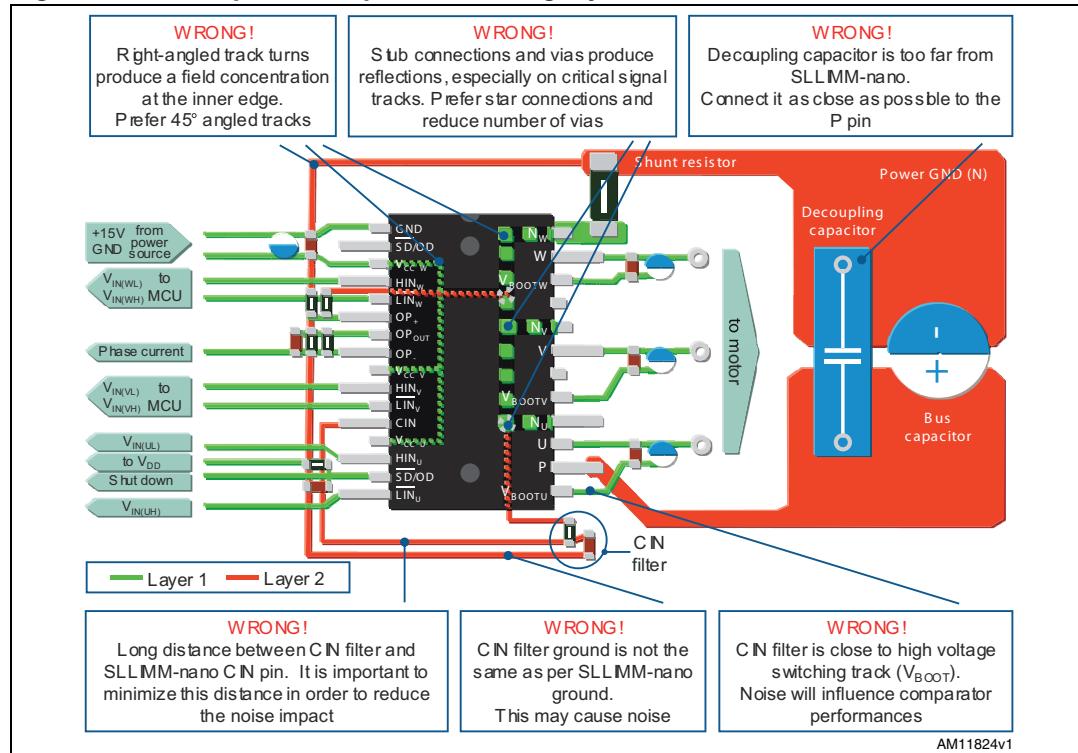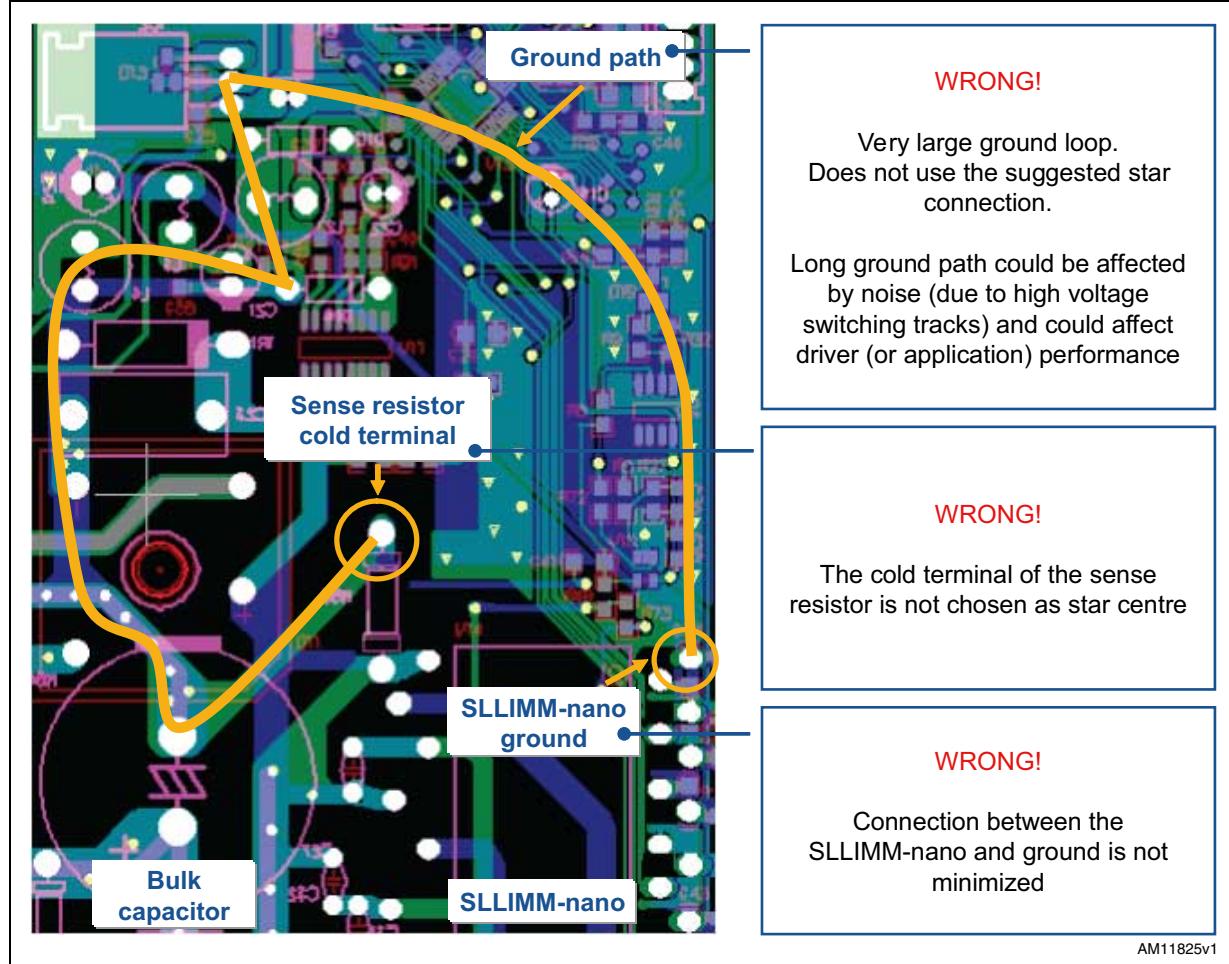
Figure 36. Example 2 on a possible wrong layout

Labels in figure:
- Ground path
- Sense resistor cold terminal
- SLLIMM-nano ground
- SLLIMM-nano
- Bulk capacitor

WRONG!

Very large ground loop. Does not use the suggested star connection.

Long ground path could be affected by noise (due to high voltage switching tracks) and could affect driver (or application) performance

WRONG!

The cold terminal of the sense resistor is not chosen as star centre

WRONG!

Connection between the SLLIMM-nano and ground is not minimized

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5.2 Mounting instructions and cooling techniques

The SLLIMM-nano is a very compact intelligent power module able to drive electric motors up to 100 W without any heatsink or cooling system installed on the board. The NDIP is a transfer mold package with no screw holes, therefore some dedicated cooling techniques must be adopted if a higher power level is targeted.
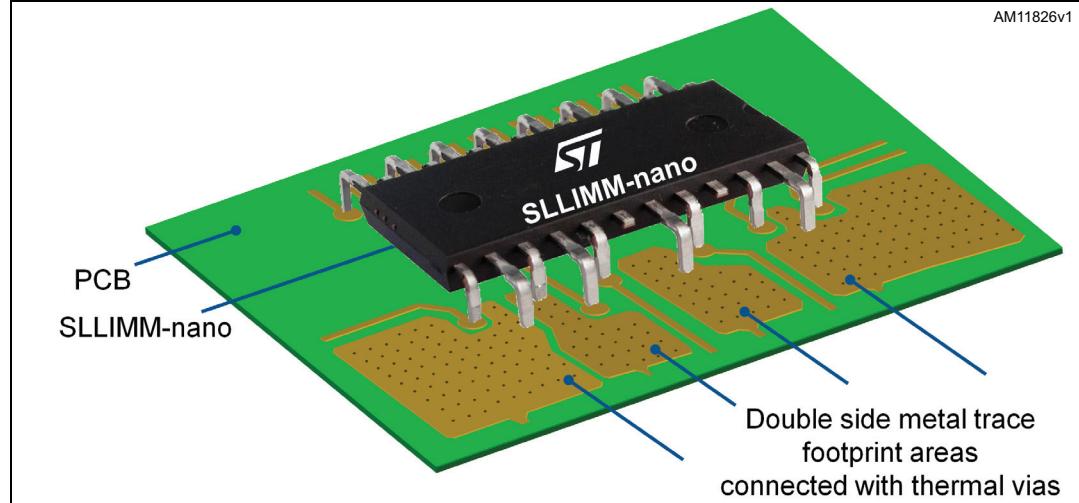
One of the easiest methods is based on a natural cooling system and a proper design of the PCB layout. In this case, the PCB, along with the pads, acts as a heatsink providing paths for individual packages to effectively transfer heat to the board and the adjacent environment. Therefore, maximizing the area of the metal traces where the power and ground pins of the package are located is a valuable method for reducing the thermal resistance and for leading to an improved power performance.

The pins mainly involved in this phenomenon are the positive DC pin (P) and the phase output pins (U, V, W), since they are directly connected to the copper lead frame where the power devices are mounted and IGBTs and diodes are the major source of heat, as already treated in *Section 4: Power losses and dissipation*. Several aspects impact on the total thermal performance, such as the area of metal traces, the thickness of the copper plate, their placement on the board and the distance between the SLLIMM-nano and other heat

sources. Both sides of the PCB can be used and thermally connected through direct copper connections or thermal vias in order to increase the heat dissipation and reduce the layout complexity.

Figure 37 shows an example of a metal trace layout used to dissipate heat on the PCB.
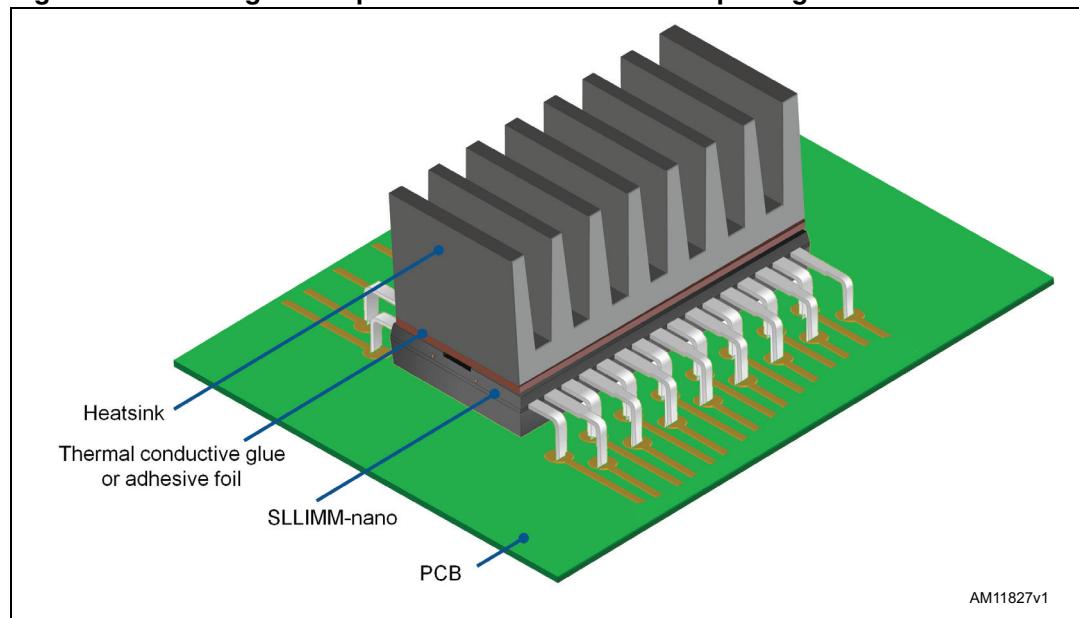
**Figure 37. Cooling technique: copper plate on the PCB**
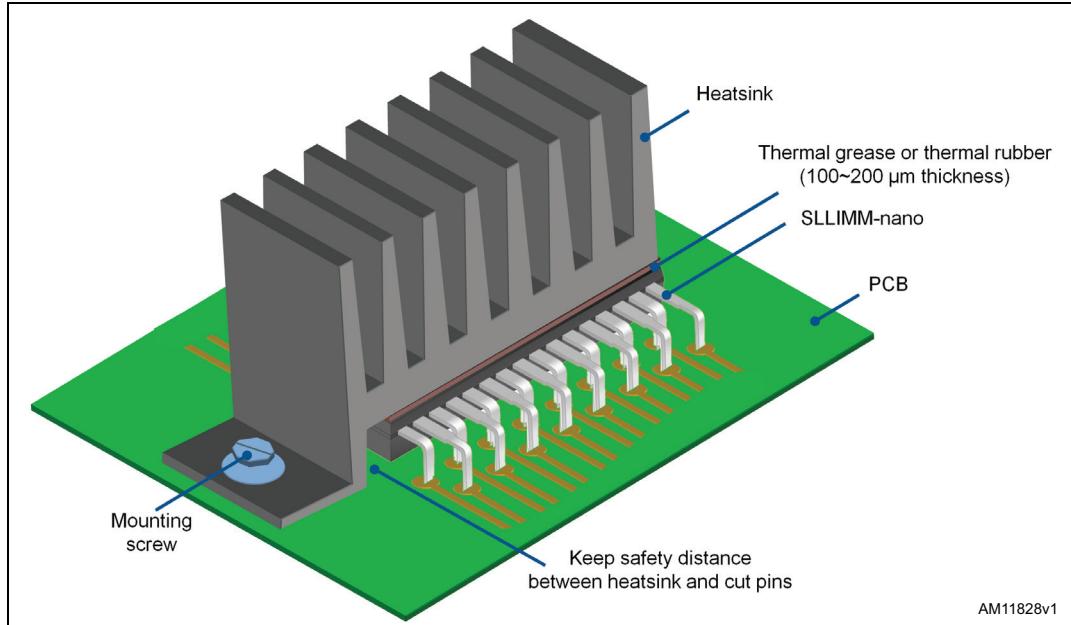
Higher thermal performance can be achieved by using a large and compact external heatsink, in close contact with the SLLIMM-nano.

The heatsink can be directly fixed on the package thanks to thermal conductive glue or adhesive foil between the heatsink and the backside of the package, as shown in *Figure 38*.

Figure 38. Cooling technique: heatsink bonded on the package

An alternative method provides a heatsink (or plate) bonded on the package and fixed on the PCB through a mounting screw, giving higher mechanical stability, as shown in *Figure 39*. This heatsink installation method requires a uniform layer of thermal grease or thermal rubber layer and needs a safety distance between the heatsink and the lateral side of the SLLIMM-nano, where some cut pins appear.

Figure 39.   Cooling technique: heatsink bonded on the PCB

Finally, a large variety of solutions may exist which take advantage of the metal box in which the board can eventually be housed.

Nevertheless, whatever the heatsink installation method may be, some precautions should be observed to maximize the effect of the heatsink. Smoothen the surface by removing burrs and protrusions; it is essential to ensure an optimal contact between the SLLIMM-nano and the heatsink. Apply a uniform layer of silicon grease (or thermal conductive glue), from 100 μm up to 200 μm of thickness, between the device and the heatsink to reduce the contact thermal resistance. Be sure to apply the coating thinly and evenly, taking care to not have any voids remaining on the contact surface between the SLLIMM-nano and the heatsink. We recommend using high quality grease with stable performance within the operating temperature range of the SLLIMM-nano.

6 General handling precaution and storage notices

The incidence of thermal and/or mechanical stress to the semiconductor devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

The SLLIMM-nano is an ESD sensitive device and it may be damaged in the case of ESD shocks. All equipment used to handle power modules must comply with ESD standards including transportation, storage, and assembly.

Transportation

Be careful when handling the SLLIMM-nano and packaging material. Ensure that the module is not subjected to mechanical vibration or shock during transport. Do not throw or drop in order to ensure that the SLLIMM-nano is correctly functioning before boarding. Wet conditions are dangerous and moisture can also adversely affect the packaging. Hold the package in such a way as to avoid touching the leads during mounting. Putting package boxes upside down, leaning them at an angle, or giving them uneven stress may cause the terminals to be deformed or the resin to be damaged.

Throwing or dropping the packaging boxes may cause the modules to be damaged. Wetting the packaging boxes may cause the malfunction of modules when operating. Pay attention when transporting in wet conditions.

Storage
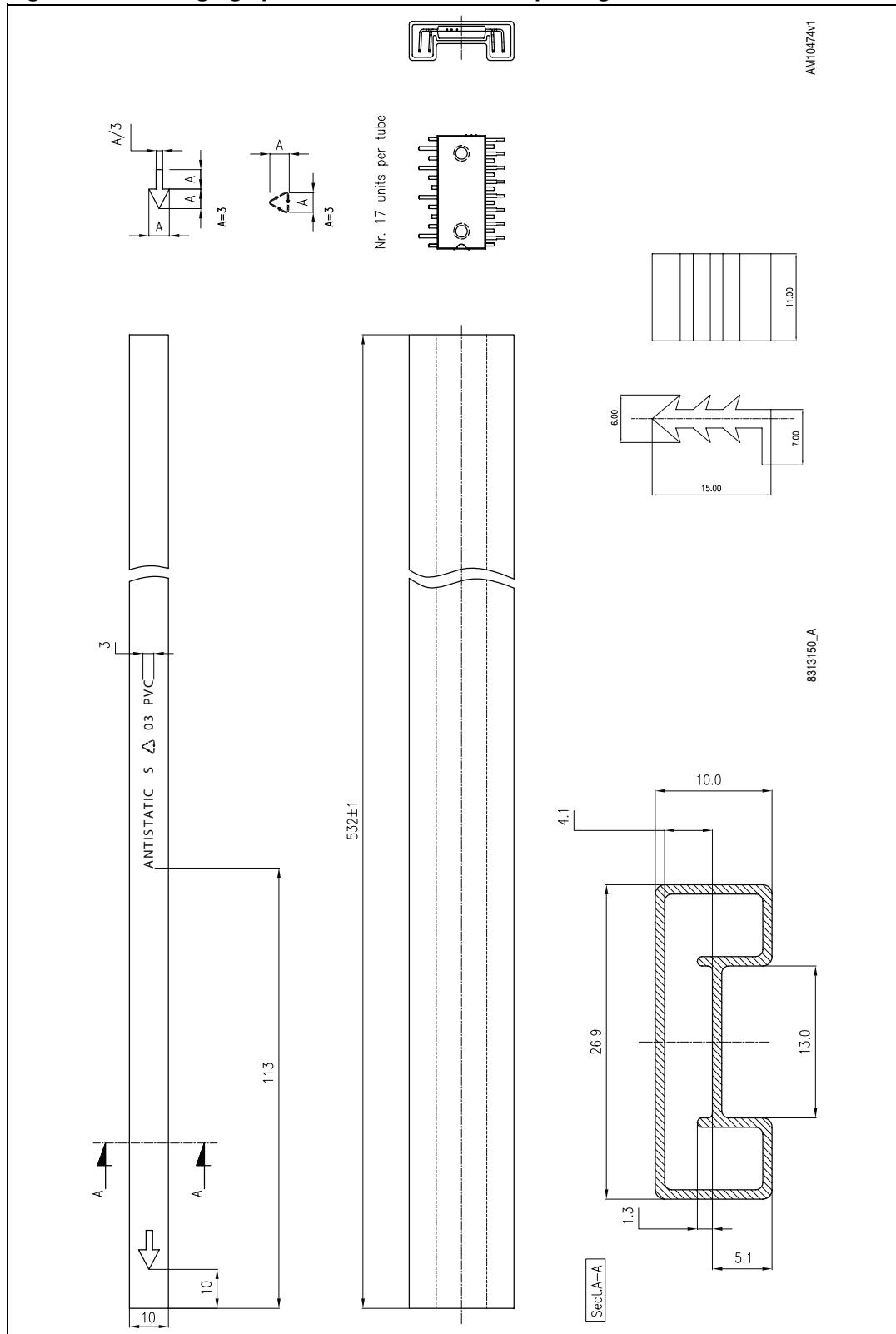
● Do not force or load external pressure on the modules while they are in storage

● Humidity should be kept within the range of 40% to 75%, the temperature should not go over 35 °C or below 5 °C

● Lead solder ability is degraded by lead oxidation or corrosion. So using storage areas where there is minimal temperature fluctuation is highly recommended

● The presence of harmful gases or dusty conditions is not acceptable for storage

● Use antistatic containers.

Electrical shock and thermal injury

● Do not touch either module or heatsink when the SLLIMM-nano is operating to avoid sustaining an electrical shock and/or a burn injury.

6.1 Packaging specifications

Figure 40. Packaging specifications of NDIP-26L package

7 References

1. AN3338 application note
2. STGIPN3H60A datasheet
3. STGIPN3H60 datasheet
4. AN2738 application note
5. UM1483 user manual
6. UM1517 user manual
7. Minimum-Loss Strategy for Three-Phase PWM Rectifier, IEEE, JUNE 1999

Note: *SLLIMM™ and PowerMESH™ are trademarks of STMicroelectronics.*

8 Revision history

Table 12.   Document revision history

Date	Revision	Changes
05-Apr-2012	1	Initial release.
17-Sep-2012	2	Updated: *Figure 4 on page 9*, *Figure 17 on page 28*, *Figure 34* and *Figure 35 on page 52*.

Please Read Carefully: